module top(clk,reset,a1,a2,a3,b1,b2,b3,c1,c2,c3,c4,c5,c6,c7,c8,c9);

parameter data\_size=8;

input wire clk,reset;

input wire [data\_size-1:0] a1,a2,a3,b1,b2,b3;

output wire [2\*data\_size:0] c1,c2,c3,c4,c5,c6,c7,c8,c9;

wire [data\_size-1:0] a12,a23,a45,a56,a78,a89,b14,b25,b36,b47,b58,b69;

pe P1 (.clk(clk), .reset(reset), .in\_a(a1), .in\_b(b1), .out\_a(a12), .out\_b(b14), .out\_c(c1));

pe P2 (.clk(clk), .reset(reset), .in\_a(a12), .in\_b(b2), .out\_a(a23), .out\_b(b25), .out\_c(c2));

pe P3 (.clk(clk), .reset(reset), .in\_a(a23), .in\_b(b3), .out\_a(), .out\_b(b36), .out\_c(c3));

pe P4 (.clk(clk), .reset(reset), .in\_a(a2), .in\_b(b14), .out\_a(a45), .out\_b(b47), .out\_c(c4));

pe P5 (.clk(clk), .reset(reset), .in\_a(a45), .in\_b(b25), .out\_a(a56), .out\_b(b58), .out\_c(c5));

pe P6 (.clk(clk), .reset(reset), .in\_a(a56), .in\_b(b36), .out\_a(), .out\_b(b69), .out\_c(c6));

pe P7 (.clk(clk), .reset(reset), .in\_a(a3), .in\_b(b47), .out\_a(a78), .out\_b(), .out\_c(c7));

pe P8 (.clk(clk), .reset(reset), .in\_a(a78), .in\_b(b58), .out\_a(a89), .out\_b(), .out\_c(c8));

pe P9 (.clk(clk), .reset(reset), .in\_a(a89), .in\_b(b69), .out\_a(), .out\_b(), .out\_c(c9));

endmodule

module pe(clk,reset,in\_a,in\_b,out\_a,out\_b,out\_c);

parameter data\_size=8;

input wire reset,clk;

input wire [data\_size-1:0] in\_a,in\_b;

output reg [2\*data\_size:0] out\_c;

output reg [data\_size-1:0] out\_a,out\_b;

always @(posedge clk)begin

if(reset) begin

out\_a=0;

out\_b=0;

out\_c=0;

end

else begin

out\_c<=out\_c+in\_a\*in\_b;

out\_a<=in\_a;

out\_b<=in\_b;

end

end

endmodule

module test;

reg clk;

reg reset;

reg [7:0] a1,a2,a3,b1,b2,b3;

wire [16:0] c1,c2,c3,c4,c5,c6,c7,c8,c9;

top uut (

.clk(clk), .reset(reset), .a1(a1), .a2(a2), .a3(a3), .b1(b1), .b2(b2), .b3(b3), .c1(c1), .c2(c2), .c3(c3), .c4(c4), .c5(c5), .c6(c6), .c7(c7), .c8(c8), .c9(c9) );

initial

begin

clk = 0; reset = 0; a1 = 0; a2 = 0; a3 = 0; b1 = 0; b2 = 0; b3 = 0;

#5 reset = 1; #5 reset = 0;

#5; a1 = 1; a2 = 0; a3 = 0; b1 = 2; b2 = 0; b3 = 0;

#10; a1 = 2; a2 = 4; a3 = 0; b1 = 4; b2 = 1; b3 = 0;

#10; a1 = 3; a2 = 5; a3 = 7; b1 = 6; b2 = 5; b3 = 3;

#10; a1 = 0; a2 = 6; a3 = 8; b1 = 0; b2 = 9; b3 = 7;

#10; a1 = 0; a2 = 0; a3 = 9; b1 = 0; b2 = 0; b3 = 8;

#10; a1 = 0; a2 = 0; a3 = 0; b1 = 0; b2 = 0; b3 = 0;

#100;

$monitor("%d %d %d\n%d %d %d\n%d %d %d",c1,c2,c3,c4,c5,c6,c7,c8,c9);

end

initial begin

forever #5 clk = ~clk;

end

endmodule