Validation Plan and Report: Payload Interface Unit (PIU) – 8U CubeSat

### Scoping and Objectives

This validation document is intended to verify the functional performance and robustness of the Payload Interface Unit (PIU), which is designed to manage data transfer between the payload and the On-Board Computer (OBC) of an 8U CubeSat. The scope includes independent characterization of the PIU in absence of a payload, subsystem validation, and test automation framework development.

### Key Risks & Features

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| **#** | **Risk Description** | **Risk Score** | **Validation Plan** |
| 1 | Payload unavailable for early testing |  | Develop and integrate a payload simulator for interface emulation |
| 2 | LVDS bit errors during data transmission |  | Perform bit error rate testing with variable patterns, implement hardware signal integrity checks |
| 3 | Failure during thermovac conditions |  | Conduct thermal vacuum tests with full instrumentation, isolate failure causes, apply design mitigation |
| 4 | Memory failure or data corruption in 128GB NV memory |  | Full write-read memory validation with CRC checks under temperature cycling |

## Validation Test Plan

### Mechanical Validation

* Visual and optical inspection of:
  + PCB integrity (cracks, delamination)
  + Connector alignment and solder joint quality
  + Component orientation (ICs, passives)
  + External dimensions and mass (compliance with CubeSat specs)

### **Electrical Tests**

* **Power Consumption:**
  + Measure current draw at 5V input during:
    - Startup (inrush current)
    - Idle vs. active modes (LVDS/RS-422 data transfer)
  + Validate rail stability (3V3, 5V, VBAT) under load
* **Signal Integrity:**
  + LVDS Interface:
    - Verify ~100Ω termination resistance (power-off)
    - Eye diagram analysis (jitter, skew, amplitude)
    - Measure skew using differential probe
  + RS-422 Interface:
    - Loopback test with framed data
    - Check for parity/framing errors

### **Functional Tests**

* **Payload-PIU Interface:**
  + Emulate payload data streams (50 Mbps LVDS)
  + Validate CRC and buffer handling
* **PIU-OBC Interface:**
  + Test 150 Mbps link to OBC
  + Verify throughput and error-free operation
* **Non-Volatile Memory:**
  + Write/read 1GB test patterns
  + Validate data retention after power cycles

### **Environmental Tests**

* **TVAC Testing:**
  + Operate at -40°C to +85°C
  + Monitor LVDS/OBC link stability
* **Post-Thermal Checks:**
  + Re-run power consumption tests
  + Verify memory integrity

### **EMC Tests**

* Radiated/conducted emissions (LVDS, RS-422)
* Susceptibility to burst/continuous-wave interference

## **Test Resources**

### **Firmware/Software:**

* Payload Emulator software (FPGA bitstream + config scripts)
* OBC Simulator Tools
* Automated Test Controller Scripts

### **Hardware:**

* PIU EM Unit + 5V power supply
* Payload Emulator
* OBC Test Sled (minimum viable setup for OBC power/comms)
* Digital Oscilloscope (eye diagram capture)
* TDR Tester (impedance verification)
* LVDS Logic Analyzer
* Thermal Chamber
* RS-422 Loopback Test Harness
* SpaceWire Interface Node (Test Router)