FRENZY SALARY CALCULATOR
CONSILIUM PS1

-BY TEAM SSS

- COMPONENTS USED:
  - COMPARATOR
  - ADDER
  - UNIVERSAL SHIFT REGISTER
  - LOGIC STATES
  - SYNCHRONOUS COUNTER
  - LOGIC PROBE

- APPROACH:
  - PROTEUS
    - THE INPUT FROM **LOGIC STATES** INCLUDES LEVEL. FOR EX, IF THE SALARY FOR THE 5^{TH} LEVEL IS TO BE FOUND THEN THE INPUT NEEDS TO BE 5 THROUGH THE LOGIC STATES.THE MAXIMUM INPUT WHICH CAN BE TAKEN IS 15.

    - THE **COUNTER** OVER HERE JUST BEHAVES LIKE LOOP COUNTER IN FOR LOOP WHICH COUNTS THE ITERATIONS THAT HAVE OCCURRED. IT HAS AN INITIAL STATE ONE HERE. SO EVEN IF THE INPUT IS 0, THEN IT DISPLAYS THE SALARY OF THE 1^{ST} LEVEL.

    - ONE SET OF **SHIFT REGISTERS** STORES THE PRESENT STATE AND THE OTHER SET STORES THE NEXT STATE JUST LIKE, TWO VARIABLES OF TYPE REG GIVEN AN INITIAL STATE OF 5 AND 7 RESPECTIVELY.

      - HERE, ONLY LOADING AND RETAINING PROPERTIES OF REGISTER IS USED BY CONNECTING THE SELECTING LINES TO COMPARATOR.

    - **ADDER** CONTINUOUSLY SUMS UP THE PRSENT STATE AND NEXT STATE VALUES AND FEEDS IT TO THE SECOND SET OF REGISTERS.

    - **CLOCK** SIGNAL HELPS IN INCREMENTING THE COUNTER. IT IS USED AT HIGH FREQUENCY HERE IN ORDER TO SHOW OUTPUT QUICKLY.

- **COMPARATOR** HELPS IN STOPPING THE PROCESS OF CALCULATION ONCE THE REQUIRED LEVEL IS REACHED.

- **LOGIC PROBES** ARE USED TO SHOW THE OUTPUT SALARY.

➢ VERILOG

- THERE IS A SLIGHT DIFFERENCE IN BETWEEN PROTEUS AND VERILOG IMPLEMENTATIONS.

- HERE THE INSTANCES SR1 AND SR2 ARE GIVEN THE INITIAL STATE WITH HELP OF A **RESET PIN**.

- IN THE TESTBENCH RESET IS GIVEN A VALUE 0 SO THAT THE REGISTERS GET THEIR INITIAL VALUES AT FIRST POSEDGE OF CLOCK.

- FOR LATER POSEDGE OF CLOCK, THE RESET HAS BEEN INITIALIZED TO 1 WHICH LETS THE REGISTER DO ITS NORMAL FUNCTIONING OF LOADING AND RETAINING.

- FOR FINDING THE SALARY OF THE NTH LEVEL UPTO 15^{TH} VALUE OF t_a IN THE TESTBENCH MUST BE UPDATED TO REQUIRED VALUE.

- t_a IS A 5 BIT NUMBER TAKING THE HIGHEST POSITIVE NUMBER AS 15. VALUE GREATER THAN THATIF STORED IN t_a GIVES ERRONEOUS RESULTS.

- FOR INPUT AS 0 THE OUTPUT IS Z AS 0 LEVEL IS INVALID.

NOTE

- **THE VERILOG CODE, TESTBENCH, PROTEUS FILE, EXPLNATION AND VIDEO ARE ALL ALSO PRESENT IN THE LINK SHARED IN THE GOOGLE FORM.**

THANK YOU

ANIRUDH & SAHIT