week 2 problem

Monday, November 21, 2022 8:44 AM

Computer Organization and Architecture 10th - William Stallings.pdf

refresh operation requires 150 ns; a memory cycle requires 250 ns. What percentage of the memory's total operating time must be given to refreshes?

5.3 Figure 5.20 shows a simplified timing diagram for a DRAM read operation over a bus. The access time is considered to last from t_1 to t_2. Then there is a recharge time, lasting from t_2 to t_3, during which the DRAM chips will have to recharge before the processor can access them again.

a. Assume that the access time is 60 ns and the recharge time is 40 ns. What is the memory cycle time? What is the maximum data rate this DRAM can sustain, assuming a 1-bit output?

b. Constructing a 32-bit wide memory system using these chips yields what data transfer rate?

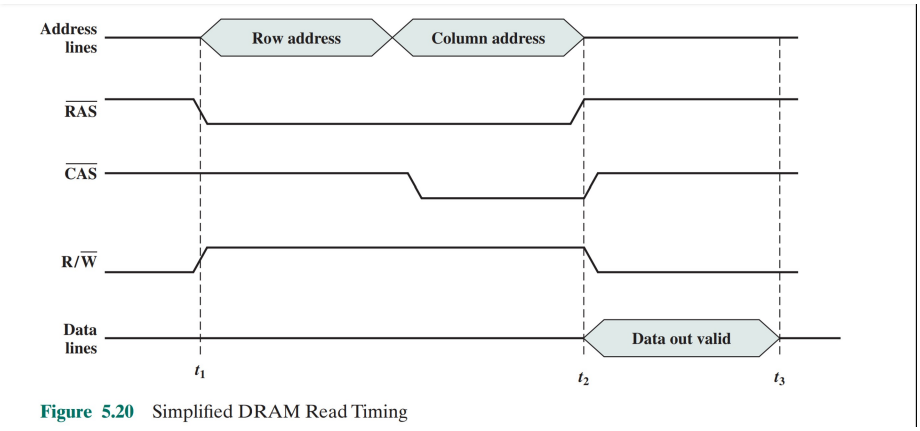

Figure 5.20 Simplified DRAM Read Timing

(Ref: T1 page 123)

- **Access time (latency):** For random-access memory, this is the time it takes to perform a read or write operation, that is, the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use. For non-random-access memory, access time is the time it takes to position the read–write mechanism at the desired location.
- **Memory cycle time:** This concept is primarily applied to random-access memory and consists of the access time plus any additional time required before a second access can commence. This additional time may be required for transients to die out on signal lines or to regenerate data if they are read destructively. Note that memory cycle time is concerned with the system bus, not the processor.
- **Transfer rate:** This is the rate at which data can be transferred into or out of a memory unit. For random-access memory, it is equal to 1/(cycle time). For non-random-access memory, the following relationship holds:

a)

Memory cycle time = Access time + other time before next access.

(here it is refresh time)

(Ref: T1 page 168)

DYNAMIC RAM RAM technology is divided into two technologies: dynamic and static. A **dynamic RAM (DRAM)** is made with cells that store data as charge on capacitors. The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0. Because capacitors have a natural tendency to discharge, dynamic RAMs require periodic charge refreshing to maintain data storage. The term

Given,

access time = 60 ns

refresh time = 40 ns

So memory cycle time = 60 + 40 ns

= 100 ns

= 100×10^{-9} s

= 10^{-7} s

transfer time is $\frac{1}{\text{cycle time}}$

= $\frac{1 \text{ bit}}{10^{-7} \text{ s}}$

= 10^{7} bit/s

= 10×10^{6} bit/s

= 10 $\frac{\text{mega bit}}{\text{s}}$

b) "Construct a 32 bit wide memory system using these chips"

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chips for which we calculated data transfer rate above, which was said to 1 bit output capable

for a 32 bit memory system