ROBUSTNESS OF MOSFET DEVICES UNDER HARD COMMUTATION OF THE BODY DIODE

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Abstract

This paper presents a study of the behavior of power MOSFET devices under hard commutation of the body diode as well as improvements of that behavior shown by latest technology developments based on detailed simulations of the device. Hard commutation of the body diode can represent a challenging mode of operation in regards to the ruggedness of power MOSFET devices. Also, the behavior of the body diode under hard commutation and its corresponding effects on the application are analyzed.

Introduction

The general trend in the industry towards the reduction in size of power systems imposes challenges on the design from the system down to the semiconductor level. The advances in power semiconductor technologies lower the system's associated losses. These allows for a general size reduction by various means ranging from the use of smaller magnetic components due to the use of higher switching frequencies to the possibility of reducing the size of, or even eliminating, the heatsinks.

This increase in power density translates into challenging conditions for the power devices. As an example, the Infineon OptiMOS^{TM} 200 V... 300 V family of power MOSFET can achieve a reduction of over 50 % in the general Figure of Merit ($R_{DS(on)} \cdot Q_G$) and Switching Figure of Merit ($R_{DS(on)} \cdot Q_{GD}$) with respect to the predecessor technology and other technologies on the market [1].

This large improvement in the switching speed leads in general to higher current and/or voltage slew rates (di/dt and dv/dt). At the same time, OptiMOS^{TM} 200V... 300V power MOSFETs can lower the $R_{DS(on)}$ of more than 50% compared to other technologies. The associated ohmic losses are therefore reduced by the same proportion. This allows for higher currents in the same chip increasing the current density through the device.

The previously mentioned higher di/dt, dv/dt and increased current densities that can be realized with the latest generation of devices play a significant role in the behavior and ruggedness of the so-called hard commutation of the body diode.

Application Requirements

Hard commutation of the body diode of a power MOSFET refers to the process as described in Fig. 1. This process is divided into 4 intervals as follows:
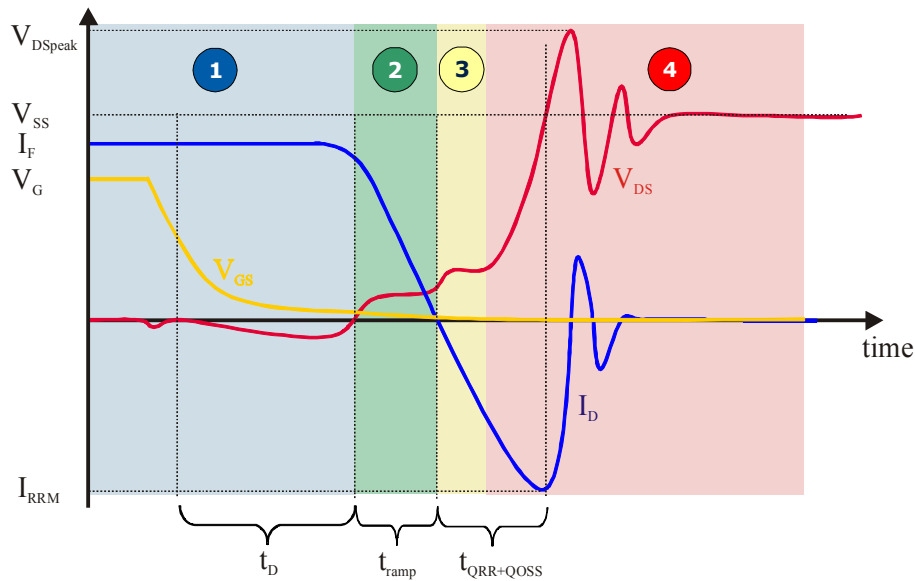
Fig. 1: Hard commutation of body diode

1. a given current I_F is initially flowing through the body diode of the power MOSFET.
2. an externally applied voltage V_{SS} now tries to reverse the polarity of the diode forcing the current to decrease
3. the current does not stop at zero but reverses, removing the previously stored charge Q_{RR}
4. once Q_{RR} is removed the voltage V_{DS} rises as the current now charges the output capacitance C_{OSS} of the device

Power MOSFET devices experience this hard commutation of the body diode process in a large number of different end applications. A typical example is Synchronous Rectification where the MOSFETs basic function is to replace a diode but the aforementioned hard commutation will also take place in other types of circuit, such as motor drives or primary side switching of SMPS power supplies.

However, the conditions at which it will happen differ significantly and depend on the specific application. The most important conditions to be considered with respect to its influence on ruggedness, generated loss and spikes are: the commutated current value I, the current slew rate di/dt, the di/dt governing mechanism (controlled by the switching speed of other devices or inductively limited) and dv/dt.

All these parameters influencing the behavior make it difficult to characterize the ruggedness of the device with a single or limited range of conditions. Attending to the typical relationship of current I and di/dt in the applications as summarized in Fig. 2, dv/dt arises as a possible parameter to cover a
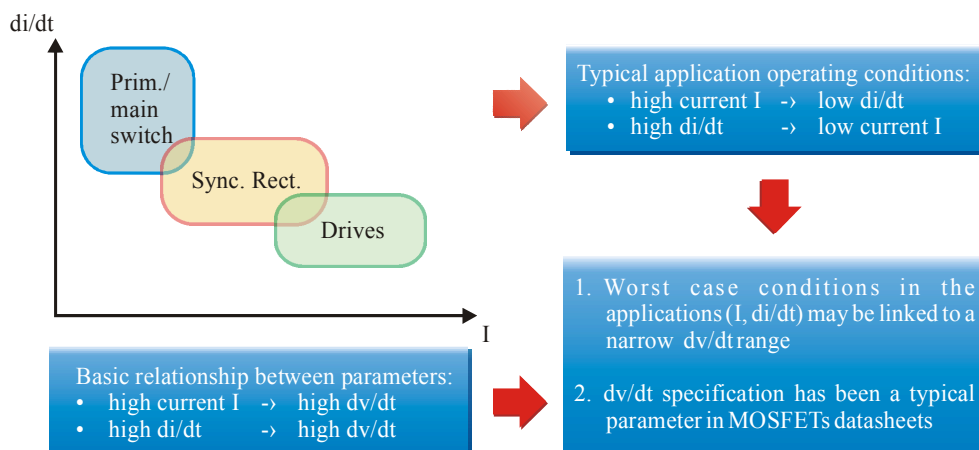

Fig. 2: Typical relationships between di/dt, dv/dt and current

wide range of conditions. Also note that a hard commutation of the body diode may easily drive the device into avalanche, depending on the present loop inductance and slew rate.

Improvement of Device Robustness

Measurement setup

The characterization of the devices was performed using a conventional double-pulse scheme, where the current di/dt is controlled by an external variable inductance. In order to achieve sufficiently high di/dt values, careful layout is required. The gate driving loop of the control MOSFET is also critical to avoiding unwanted oscillations in the system. The simplified test setup is shown in Fig. 3. As previously mentioned, the di/dt is adjusted by the variable inductor L1, which allows a very precise control of this parameter.

Basic device structure

Several years ago, the first generation of power MOSFET employing the compensation principle based on a field-plate concept was introduced [2]. In these devices, an isolated field-plate provides the mobile charges required to compensate the drift region donors under blocking conditions. The field-plate principle leads to an almost constant field distribution in the vertical direction, thereby reducing the required drift region length for a given breakdown voltage. In addition, the drift region doping can be increased. Both measures allow a significantly reduced on-state resistance. The device structure therefore not only offers an outstanding area-specific resistance, but also a low gate-charge, which is essential for fast switching. For higher blocking voltages, an edge-termination structure is added which provides the required lateral blocking capability [3]. Fig. 4 shows a possible structure of a field-plate MOSFET and an equivalent edge termination structure.

Destruction mechanism

Devices with structures such as that shown in Fig. 4, or structures with similar properties, might fail in critical operating conditions such as short-circuit or high load, despite no problems being found under regular operating conditions. In those critical operating conditions the device is subjected to fast commutation of the body diode with very high dv/dt, driving the body diode directly into avalanche. This can harm the MOSFET if large current levels are present.

As an example, Fig. 5 shows the measured current and voltage waveforms immediately before and during device destruction. As can be seen, the device commutates from body diode conduction directly into avalanche, and fails while in avalanche. A device failure was never found at substantially lower switching speeds where avalanche did not occur. The analysis of damaged devices showed melted spots in the transition region from the active cell field to the edge termination region.

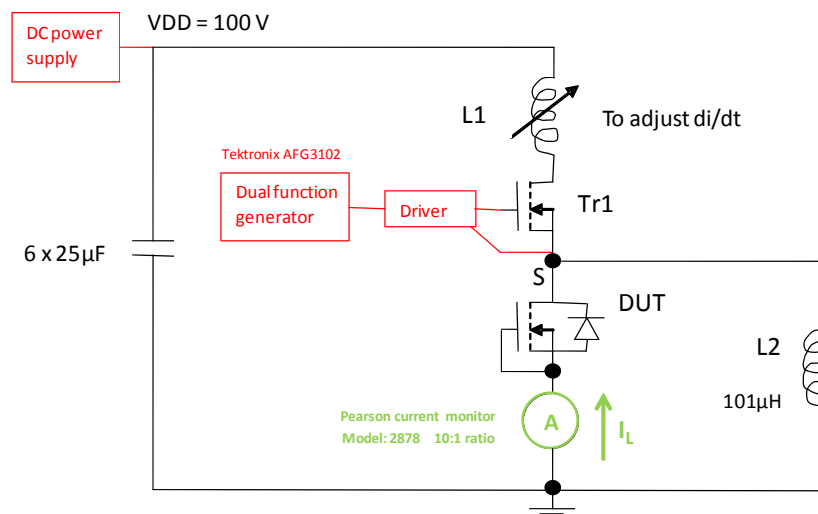In order to identify and understand the destruction mechanism, mixed-mode device simulation with

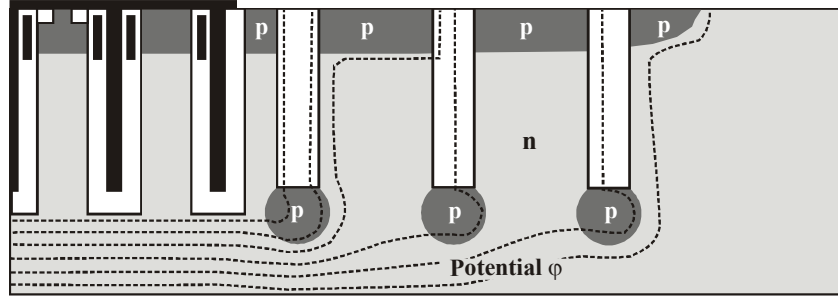Fig. 3: Schematic of the used measurement setup

Fig. 4: Schematic structure of a field-plate trench MOSFET and an appropriate edge-termination

consideration of self-heating was employed using the device simulator Medici [4]. Here the circuitry of the test setup was represented, while the MOSFET under test was modeled using two paralleled 2D devices, as shown schematically in Fig. 6. The first device consists of a MOSFET cell with an area of the active chip region. The second device represents the full edge-termination structure, its area being the product of the edge-termination width and the device perimeter. The load inductance is modeled by a constant current source. To improve the convergence of the simulation a 500 kΩ resistor and a 1 pF capacitor was added, which does not further influence the simulation results.

Using this simulation approach of two paralleled devices one can differentiate between the currents related to the active region and the edge-termination region.

Fig. 7 shows an example waveform already pointing to the root cause of destruction. The edge-termination continues to conduct after the active regions body diode stored charge is removed and its reverse recovery is almost complete. The carrier removal in the edge-termination is delayed with respect to the active region, indicated by the shifted reverse current peak of the edge region.

Fig. 8 shows the hole distribution and avalanche generation at the point in time where the maximum temperature peak is found. Fig. 8 indicates that the active cell region (left part) is already completely depleted and that a large carrier concentration is only found in the last cell adjacent to the edge termination. This is because all carriers which previously laterally diffused into the edge region during the body diode conduction phase must be removed. Since it is not an option to provide contacts to the p-wells of the edge-termination region, the carriers can only be removed via the first source contact of the active cells. However, the voltage across the device is already high. Due to the high field and the presence of carriers, this part of the structure is driven into avalanche. This leads to a strong local current flow and a strong local heat generation, resulting in a local peak temperature exceeding
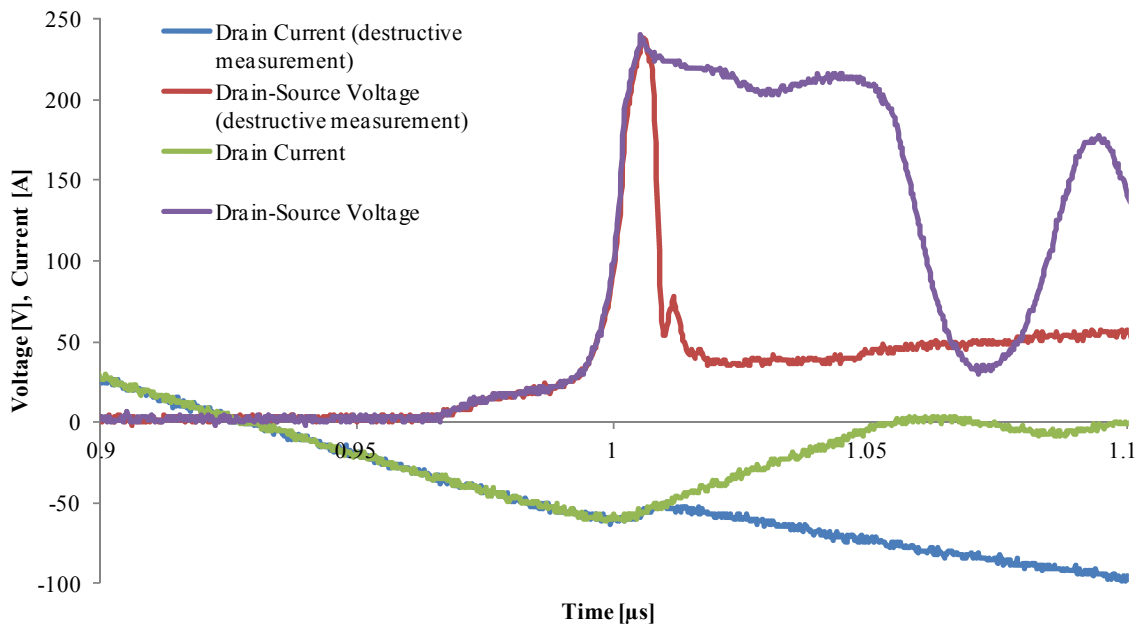

Fig. 5: Measured waveforms of a 200 V device with a current rating of 80 A before destruction (I_F = 159 A) and at destruction (I_F = 167 A)   [V_R = 100V, di/dt = 1000 A/µs]
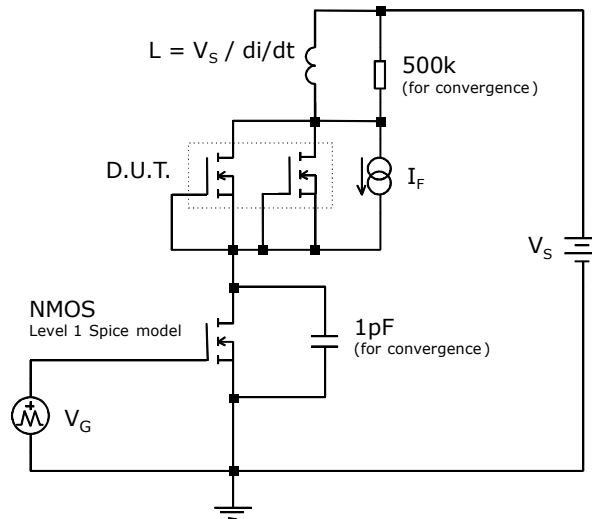
Fig. 6: Mixed-mode simulation approach

1200 K. In a real device such a high temperature is already far beyond device destruction.
It is evident that device destruction due to this failure mechanism only occurs in the case of very fast switching processes. At low switching speeds there is sufficient time to safely remove the carriers stored in the edge termination region of the device before the voltage builds up, which explains why the failure is only found under critical operation conditions.

Improvement of device robustness

To improve the ruggedness of the device under hard commutation conditions it is essential to avoid the edge-termination region being driven into avalanche. This means that either the carrier removal must be faster, less carriers must be removed, or the dynamic blocking capability in the critical part of the structure must be increased. Consequently there are several options which should all help to improve the device ruggedness. However, the effort needed to implement the different options into the existing device structure, and the resulting costs, may vary substantially.
A simple option is given by a modification of the transition region between the active cell region and the edge termination structure in order to realize a higher local dynamic blocking capability and/or to
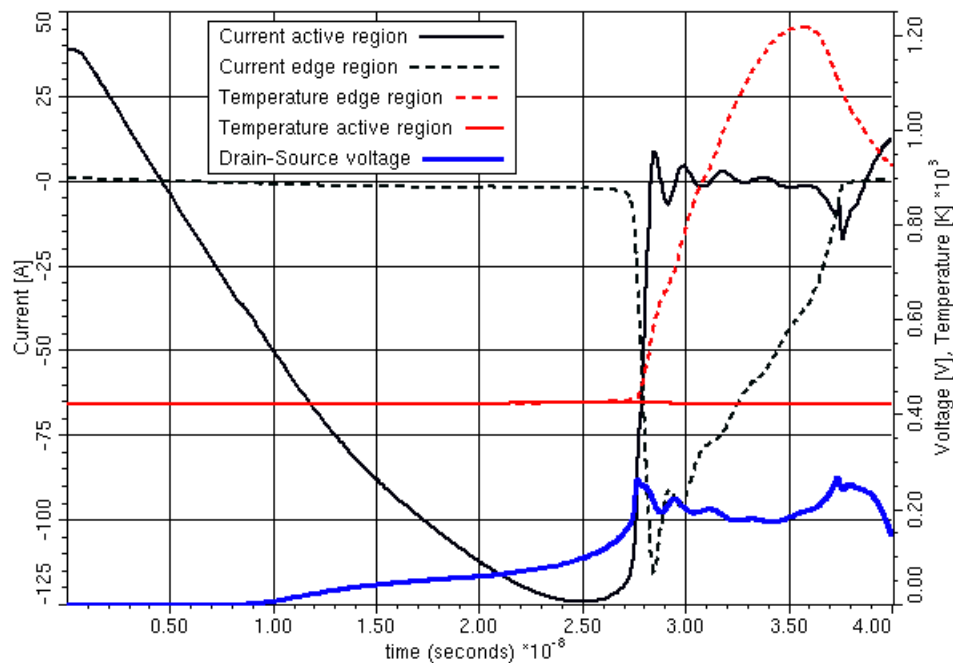

Fig. 7: Simulated commutation waveform of a 200V device with edge-termination
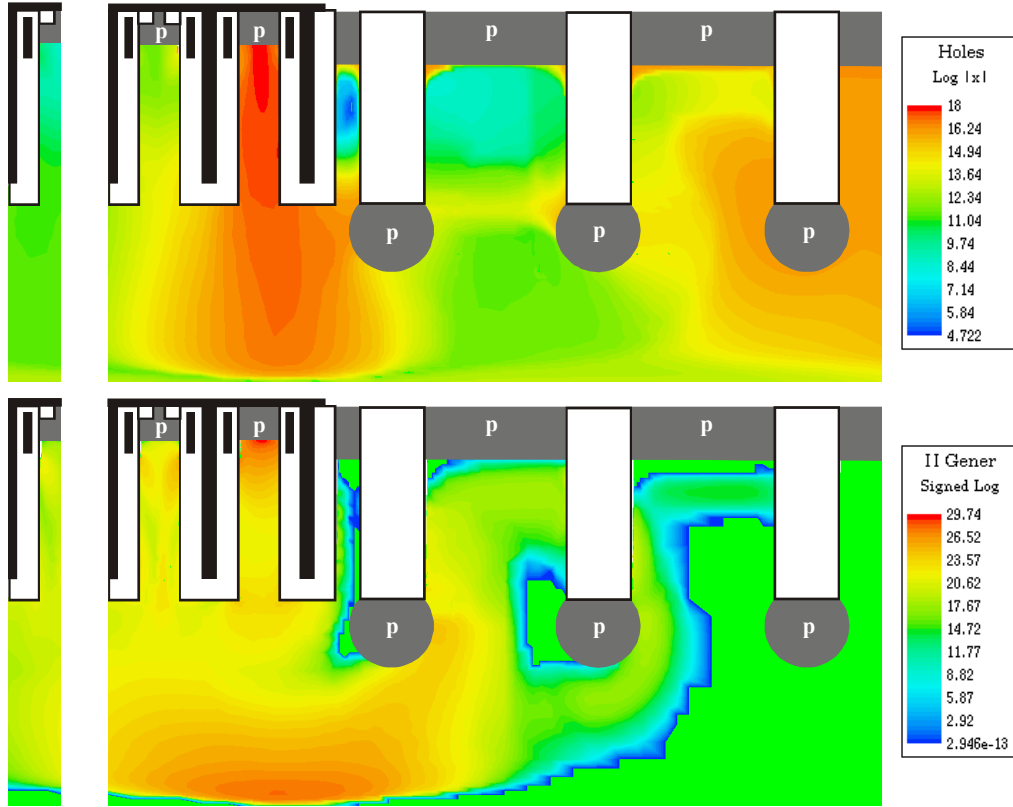
Fig. 8: Hole density (top) and avalanche generation (bottom) in the simulated structure at t = 35 ns

enable faster carrier removal. Technological options include the local modification of the vertical doping profile to further increase the blocking capability for the edge termination region and the first neighboring active cells. However, such measures may also affect the area-specific on-resistance of the device and add significant additional manufacturing costs. Further options include providing larger contact areas to prevent a possible punch-through to the contact, or reducing the lateral carrier diffusion into the edge region by a reduction of the diffusion length.

The first option investigated in this work is the extension of the buried p-regions towards the active cell region, aiming to improve the dynamic blocking capability. Fig. 9 gives the basic structure for such a modified device. The buried p-region now also extends below the last field-plate trench, which allows faster removal of the holes and improves the dynamic blocking capability.

Fig. 10 shows the simulated waveforms of such a structure with an extended buried p-region. There is clear evidence for the effectiveness of this measure. In case of the edge termination part, no delayed reverse current peak is found. The reverse current is now only fed by the stored charge of the active device region, having a much larger area than the edge region. Dynamic avalanche in the edge termination region is avoided, which prevents the device from being destroyed.

Fig. 11 gives the hole density and avalanche generation at a time of 30 ns. In contrast to the situation in the initial structure as depicted in Fig. 8, the hole concentration in the edge termination part is now
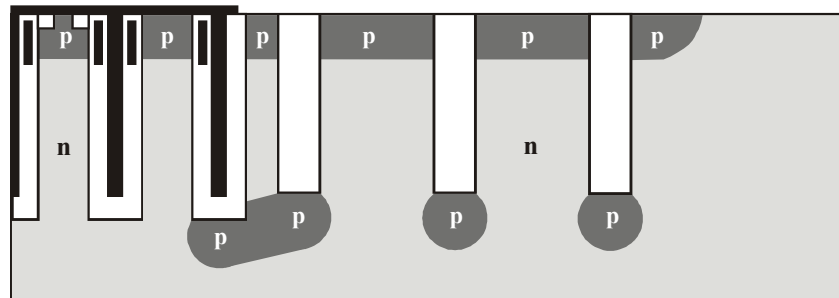

Fig. 9: Schematic structure of a field-plate trench MOSFET and improved edge-termination
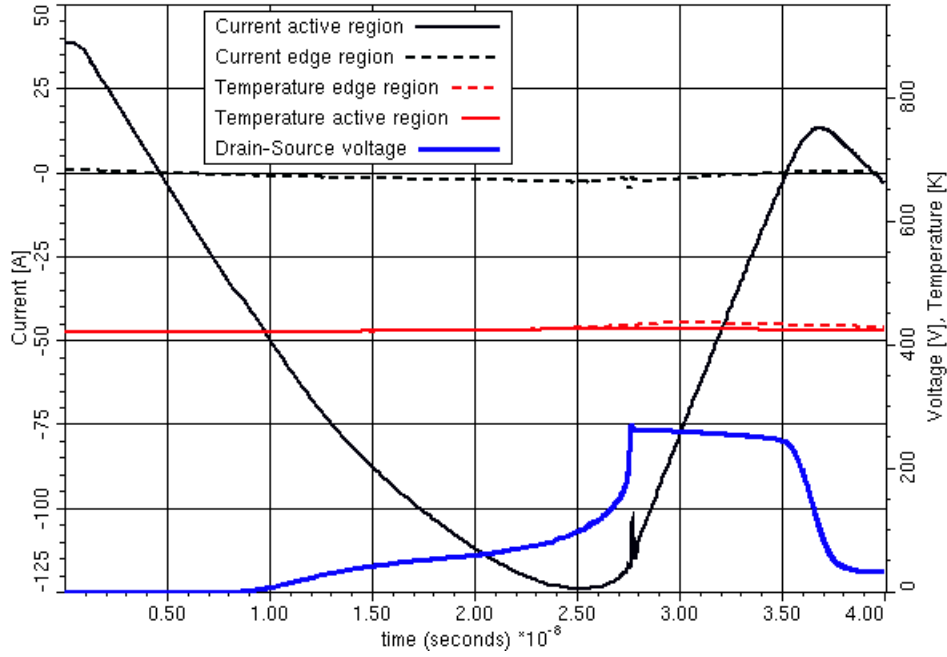
Fig. 10: Simulated commutation waveform of a 200 V device with improved edge-termination

much lower and avalanche generation is avoided. Therefore this measure is a very attractive option to gain a clear improvement in the commutation robustness of the device, since it only requires adaptations to the existing device without additional manufacturing costs.

Another potentially attractive option for the improvement of the device robustness under the given conditions is a reduction of the diffusion length of the carriers by applying carrier lifetime reduction methods. This would minimize the number of carriers diffusing into the edge termination region while the body diode is conducting. Consequently, less carriers will need to be removed, which also should help to avoid dynamic avalanche in the last cell.

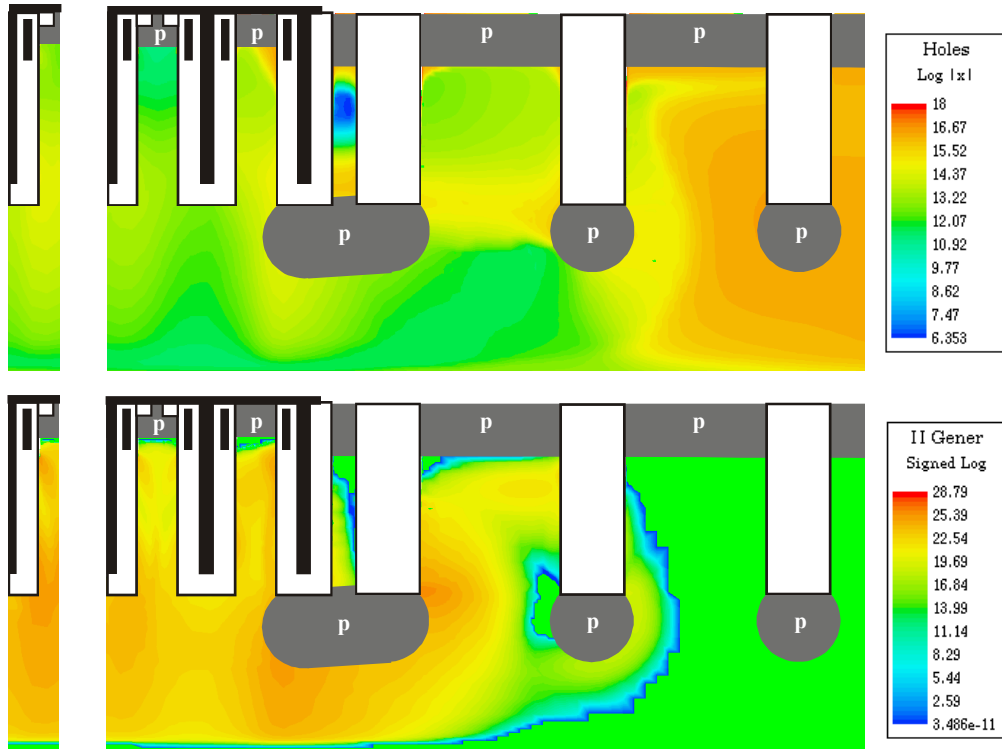The application of carrier lifetime control is a common technique widely used in high-voltage bipolar

Fig. 11: Hole density and avalanche generation in the structure with extended buried p-wells at t=30 ns
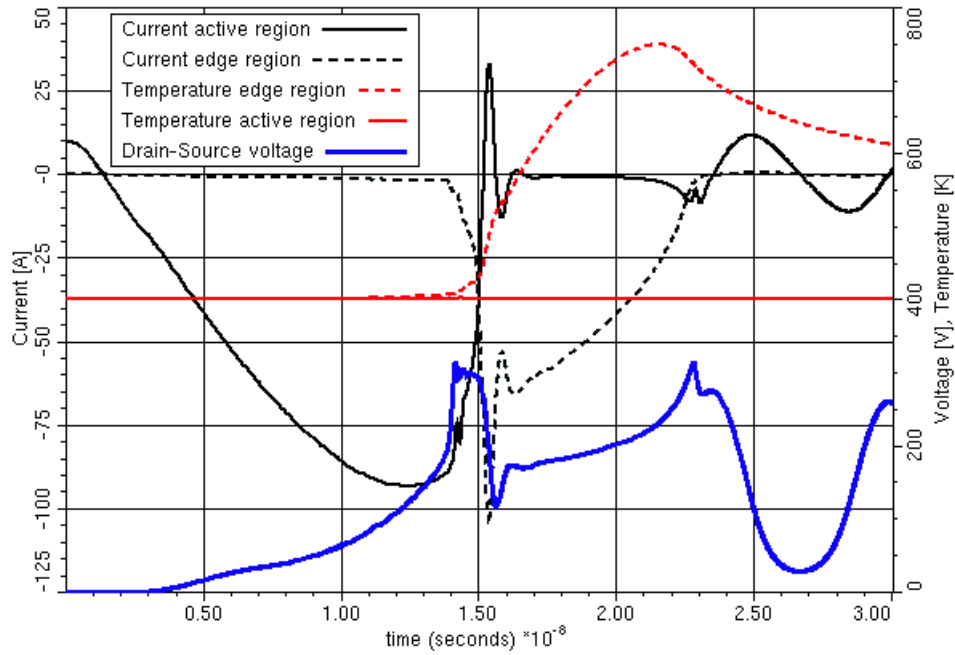
Fig. 12: Simulated commutation waveform of a standard 250 V device

power devices [5-8]. Carrier lifetime control is usually realized either by irradiation with highly-energetic light particles such as electrons, protons or helium ions, or by diffusion of heavy metals such as gold, platinum and the like [8]. All these techniques generate recombination centers in the band gap of the semiconductor material. For an exact simulation of the device properties and related effects, the full properties of the recombination centers must be known, and an extended recombination model which includes the full trap dynamics must be used. However, in many cases it is sufficient to consider only reduced carrier lifetimes to see the main effect, which was the approach adopted in this work.

Fig. 12 shows the simulated waveforms of a standard 250 V device. As in case of the 200 V standard device (see Fig. 7), the 250 V standard device also shows a delayed reverse current peak coupled to a strong local heating of the edge termination part of the device. Fig. 13 gives the waveforms for the same device with reduced carrier lifetime. Here no delayed reverse current peak of the edge termination part can be seen and the device temperature is not increased. The simulation confirms that
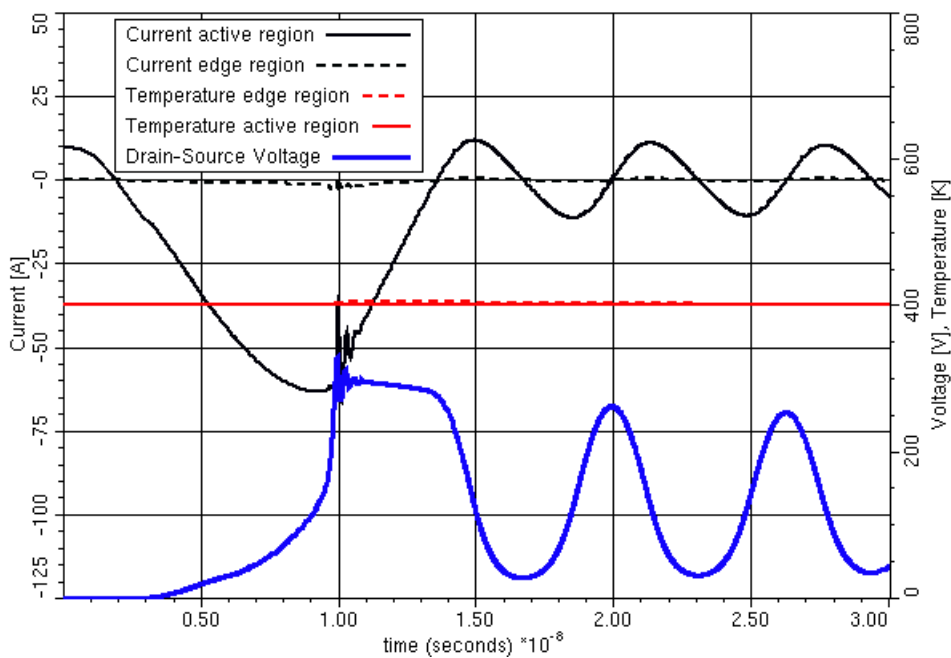

Fig. 13: Simulated commutation waveform of a 250 V device with reduced carrier lifetime

a reduction of the carrier lifetime will also improve the commutation robustness of the device. Additionally, the overall stored charge Q_{RR} of the device and the reverse-recovery peak I_{RRM} are also significantly reduced which helps to cut-down switching losses. However it must be considered that an additional carrier lifetime killing process adds significant manufacturing costs.

Experimental verification

Based on the previously discussed considerations, several measures were validated. In order to evaluate the effectiveness of the improvement measures, hard commutation measurements were done. In these measurements the forward current through the body diode was stepwise increased until device failure occured using the previously described setup (see Fig. 3). Fig. 14 compares the results for 200 V standard devices and for the devices with improved hard commutation ruggedness. A clear improvement compared to the initial structure is found; all tested robust devices survived the test as the maximum current capability of the test setup was reached. Subsequent repetitive commutation tests confirmed the ruggedness of the devices and proved the stability of the device parameters. The results clearly indicate the improvement in the hard commutation robustness of the MOSFET devices.

Next an investigation was carried-out to discover what further improvement of the device properties can be realized when additionally using carrier lifetime control measures. Fig. 15 indicates the reduction in the stored charge Q_{RR} for 200 V devices with carrier lifetime reduction applied. All of the devices with reduced carrier lifetime survived the hard commutation tests up to the measurement limit of 200 A. The aforementioned experimental investigations were also done for 250 V and 300 V devices with results qualitatively similar to the 200 V devices. Changes to the edge termination structure lead to a significant improvement of the commutation robustness while an additional carrier
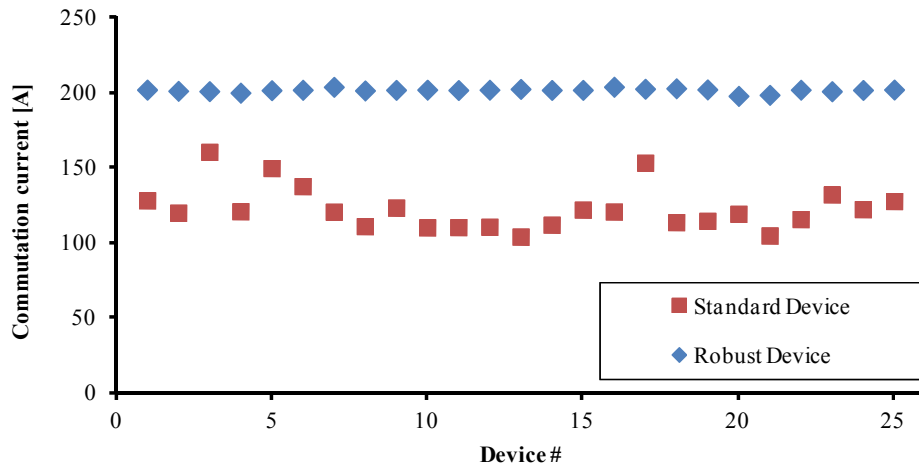

Fig. 14: Maximum forward current through body diode of 200 V MOSFET under hard commutation [$R_{DS(on)}$ = 12 mΩ, V_R = 80V, di/dt = 1900 A/µs]
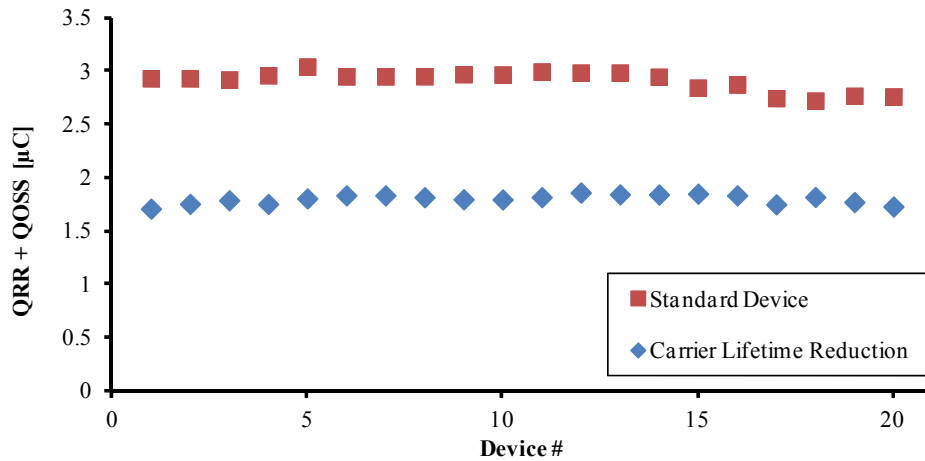

Fig. 15: Q_{RR} + Q_{OSS} for the body diode of 200 V MOSFET with and without carrier lifetime control [$R_{DS(on)}$ = 12 mΩ, I_F = 190 A, V_R = 100 V, di/dt = 1000 A/µs]
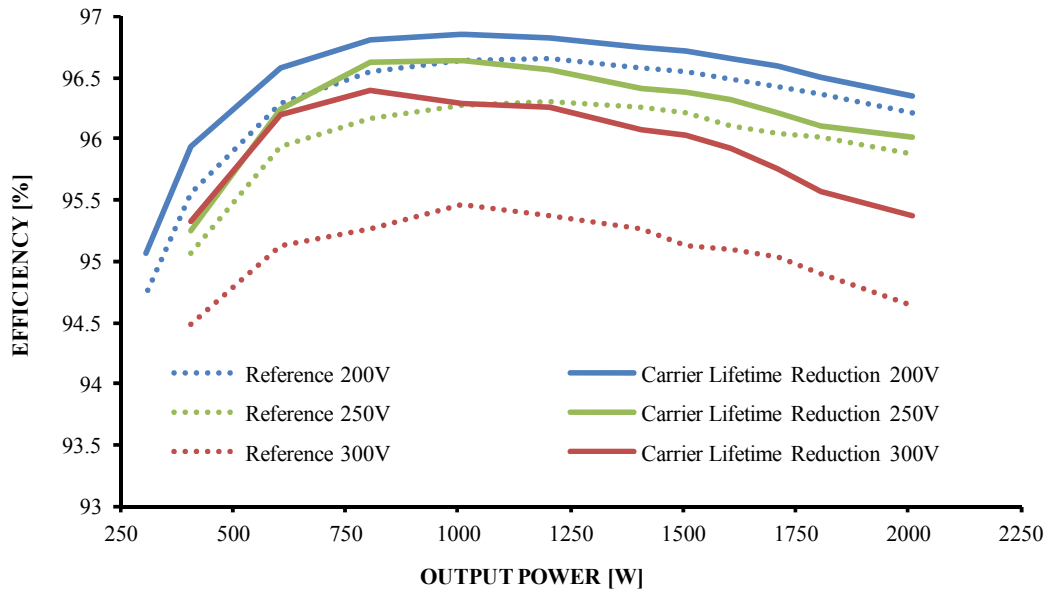
Fig. 16: Measured overall efficiency of a 2 kW full-bridge phase-shifted ZVS power supply

lifetime adjustment gives an additional performance advantage.

For a better judgment of the performance improvement, efficiency measurements were performed in a 2 kW full-bridge phase-shifted ZVS power supply. The tested MOSFET devices worked in the synchronous rectification stage in a center-taped configuration having two devices in parallel each branch of the center-tap circuit. Fig. 16 shows the efficiency gained for all three voltage classes between the commutation robust devices without and with carrier lifetime adjustment. Depending on the voltage class and load current, the overall efficiency of the power supply improved by 0.3 % … 1.2 %. This clear improvement enables a new technology for devices in the voltage range between 200 V and 300 V, which will be released as the OptiMOS™ Fast Diode.

Conclusion

In this work, the hard commutation capabilities of the MOSFET body diode were analyzed based on detailed simulation of the power device including its edge termination. A significant increase of the destructive commutation current of the initial structure was realized by modifications of the edge termination leading to an increased dynamic blocking capability. Moreover, the application of carrier lifetime control techniques as an additional measure enables a new technology generation which offers the chance for a further increase of the overall efficiency of power electronic systems.

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