

Analysis of Clamped Inductive Turnoff Failure in Railway Traction IGBT Power Modules Under Overload Conditions

Xavier Perpiñà, Jean-François Serviere, Jesús Urresti-Ibañez, Ignasi Cortés, Xavier Jordà, Salvador Hidalgo, Jose Rebollo, and Michel Mermet-Guyennet

Abstract—This paper studies the overload turnoff failure in the insulated-gate bipolar transistor (IGBT) devices of power multichip modules for railway traction. After a detailed experimental analysis carried out through a dedicated test circuit, electrothermal simulations at device level are also presented. The simulation strategy has consisted in inducing a current and temperature mismatch in two IGBT cells. Results show that mismatches in the electrothermal properties of the IGBT device during transient operation can lead to uneven power dissipation, significantly enhancing the risk of failure and reducing the lifetime of the power module. Concretely, simulations qualitatively demonstrate that localized hot-spot formation due to a dynamic breakdown could lead to a second breakdown mechanism.

Index Terms—Insulated-gate bipolar transistor (IGBT) power module, power inverter reliability, railway applications, semiconductor device breakdown, semiconductor device thermal factors.

I. INTRODUCTION

NOWADAYS, power inverter reliability is of main concern in railway traction applications. Inverters drive the train motor (inductive load) [1] using insulated-gate bipolar transistor (IGBT) multichip power modules, in which IGBT devices and freewheeling diodes are packaged together. In this application, the IGBTs are switched according to a pulsedwidth-modulation pattern (i.e., between 200 Hz and 2 kHz indicatively) to supply the required sinusoidal input current (train speed control), whereas the freewheeling diodes ensure a continuous path for the current coming from the motor [2]. These switching transitions can give rise to very stressful processes in terms of instantaneous dissipated power during both the reverse recovery in diodes and the IGBT turnoff, i.e., rugged-

ness failures when high-current and high-voltage levels coexist. Moreover, IGBT modules are also the most sensitive elements to other system failures. For instance, dysfunctions on the IGBT drivers [3], [4], sensing elements to monitor the critical electrical and thermal variables of the inverter [5], cooling system [6], and capacitors (decoupling or filter) [7] undoubtedly lead to their destruction (induced failures).

Mostly, the reliability problems related to this inverter technology have arisen from the ruggedness of the employed devices, particularly when their working conditions become more adverse. This is the case when the module wears out [8], a nonoptimum thermal management design has been carried out [9], and external electrical dysfunctions occur [7]. The package degradation limits the inverter lifetime since the working temperature inside the module increases due to the solder delamination within the package [1], [10]. This ageing process can be enormously accelerated as a consequence of a nonoptimum thermal management design (e.g., cooling system design or thermal interface selection) [9]. On the other hand, it has been observed that several failures depend on the power switch driving strategies. Sometimes, the dysfunctions on the driver produce abnormal events (short circuit, overcurrent, or overvoltage), which severely stress the components [11]. However, such events not only result from driving anomalies but also can be linked to environmental or load conditions [7]. In this failure scenario, it is interesting to determine “*a posteriori*” the device failure signature so as to derive precious information about the device failure origin. Along the years, this analysis has been tackled in both diodes and IGBTs, providing a physical insight into the failures that occurred during the diode reverse recovery and the IGBT turnoff under inductive loads.

In the case of diodes, numerous studies have concluded that the second breakdown is the electrical failure mechanism [e.g., [12]–[14]]. This phenomenon consists in an abrupt decrease of the device voltage capability with a simultaneous internal constriction of current, thus giving rise to a transition from a low to a high conductive state [15], [16]. This transition is mainly originated from an internal electrothermal instability. The inductive load forces the device to work under the so-called dynamic avalanche regime [17]–[19]. This behavior is always encountered in bipolar devices (e.g., pin diodes or IGBTs) when working under the coexistence of high-voltage and high-current levels. Under these electrical conditions, carriers are generated by an avalanche process at the p-n junction,

Manuscript received March 16, 2010; revised June 23, 2010; accepted July 24, 2010. Date of publication September 20, 2010; date of current version June 15, 2011. This work was supported in part by the European Project ‘Power Reliability for Traction Electronics’ (PORTES) under Contract MTKI-CT-2004-517224, by Alstom Transport Tarbes, by the Spanish Ministry of Science and Innovation through Research Programs THERMOS TEC2008-05577 and RUE CSD2009-00046, and by the Consejo Superior de Investigaciones Científicas under Contract “Junta para la Ampliación de Estudios,” JAE-Doc.

X. Perpiñà, J. Urresti-Ibañez, I. Cortés, X. Jordà, S. Hidalgo, and J. Rebollo are with the Instituto de Microelectrónica de Barcelona, Centro Nacional de Microelectrónica, Consejo Superior de Investigaciones Científicas, Campus Universitat Autónoma de Barcelona, 08193 Bellaterra, Spain (e-mail: xavier.perpinaya@imb-cnm.csic.es).

J.-F. Serviere and M. Mermet-Guyennet are with Alstom Transport Tarbes, 65600 Séméac, France.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TIE.2010.2077613

modifying the electric field distribution inside the device for a given anode-to-cathode voltage [17]. In the case of a triangular-like electric field distribution within the drift region, this phenomenon eventually decreases the breakdown voltage of a p-n junction (dynamic breakdown) [19], [20]. In addition, thermally generated carriers within the drift region increase with the operating temperature, also contributing to the electric field distortion. On the other hand, when the electric field adopts a trapezoidal-like shape within the drift region, a complex and local electrothermal coupling between current and temperature increase may eventually induce a stable current filamentation due to carrier injection from the n⁻-n⁺ junction close to the anode, as reported in [16], [20]–[22]. Therefore, the aforementioned phenomena may be thermally or current density driven (thermal- or current-mode second breakdown, respectively).

In the case of IGBT devices, there is a lack of knowledge on this subject. In fact, robustness and ruggedness studies in IGBTs have been mostly focused on their short-circuit performances [23], [24]. In the literature, the failure dynamics of IGBTs [planar nonpunch-through (NPT) devices] was theoretically analyzed in [23] for the clamped inductive turnoff and short-circuit events. They concluded that the physical mechanism in each situation was not the same. According to [23], the short-circuit failure was caused by two competing mechanisms: the parasitic thyristor latch-up and the thermally assisted carrier multiplication. On the other hand, the failure during the device turnoff under a clamped inductive load was only attributed to a thermally assisted carrier multiplication. This phenomenon eventually breaks down the IGBT body junction (thermal-mode second breakdown), as observed in diodes. Concerning the turnoff, the same behavior was experimentally reported in [25] under unclamped inductive conditions: the loss of the blocking capability of the IGBT when sustaining voltage (second breakdown). In that work, the technological characterization analysis of failed devices was not carried out.

This paper aims to verify whether the thermal-mode second breakdown occurs in IGBT power modules for railway traction under overcurrent and overtemperature conditions. The interest of this study is clear: The second breakdown is roughly presented or mentioned in the literature [25], but no rigorous analysis has manifested such fact under this particular failure case. Moreover, overcurrent conditions in the IGBT inductive turnoff are likely to occur, e.g., when an unexpected inductor current discharge (motor) is produced during braking processes. In such a situation, although the failure may be inferred from the device reverse-blocking safe operating area (RBSOA) [26], there is neither a reasonable explanation about the damage suffered by the component nor the details about the physical process. This investigation is faced via experimental robustness tests and assisted by physical numerical simulations, since the inverter main electrical parameters (e.g., gate voltages, phase currents, etc.) cannot be easily monitored.

II. EXPERIMENTAL RESULTS

A. Robustness Tests: Description and Results

The switching conditions encountered during an actual inverter operation can be reconstructed by the simplified

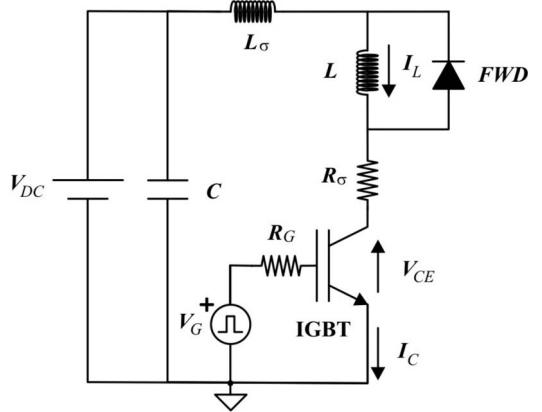


Fig. 1. Schematic of the test circuit used to reconstruct the actual inverter switching conditions.

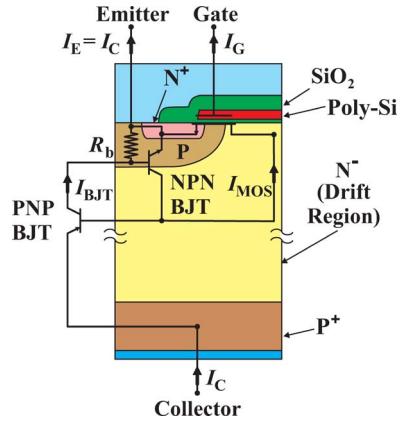


Fig. 2. Schematic cross-sectional view of a planar NPT IGBT.

schematic (clamped inductive test circuit) shown in Fig. 1. When the IGBT is in the ON-state regime, the current through the inductive load L increases proportionally to the input voltage value V_{DC} . Once the IGBT is turned off, the inductor current I_L diverts from the transistor to the freewheeling diode FWD . Typical features of the turnoff transition are the current tails, associated with the removal of the stored charge in the base of the IGBT, and the overshoot of the collector-emitter voltage, affected by the parasitic inductance L_σ [2]. In our experiments, V_{DC} , L , and R_G are set at 2500 V, 100 μ H, and 3.7 Ω , respectively, and for the used test circuit, $L_\sigma = 285$ nH has been measured. On the other hand, the modules are rated at 3.3 kV/1200 A and contain planar NPT IGBTs (first generation) [27] and emitter-controlled p-i-n diodes [28]. Under such working conditions, tests up to failure have been performed on ten IGBT power modules to determine and assess an electrical signature when the RBSOA limits of the IGBT transistors are overcome by either overcurrent or overtemperature events. The robustness tests for overcurrent conditions have been performed at $T = 398$ K, whereas for the overtemperature situation, they have been carried out for $I_C = 2400$ A. Fig. 2 shows a schematic cross-sectional view of an IGBT basic half cell, highlighting some features of interest for the following discussion. According to the bipolar junction transistor (BJT)-MOSFET-based compact model for an IGBT [27], the collector current I_C consists of two components:

an electron current flowing through the channel (I_{MOS}) and a hole current component flowing through the intrinsic p-n-p BJT (I_{BJT}). This current component also flows across the base resistance R_b of the parasitic n-p-n BJT structure, which can eventually lead to the device latch-up as long as the voltage drop across R_b becomes high enough to forward bias the p-n base-emitter junction (parasitic thyristor activation).

The most interesting waveforms obtained from all tests are shown in Fig. 3(a)–(d). Typical results for a safe overcurrent turnoff transition are shown in Fig. 3(a). When the turnoff signal is applied, at time t_0 , the gate-emitter voltage V_{GE} first falls down to a plateau and remains constant until the well-known Miller effect finishes [27]. Then, at time t_1 , the collector-emitter voltage V_{CE} starts rising up, while V_{GE} decreases further, leading to a reduction of I_{MOS} . Since I_C remains constant, I_{BJT} increases. At time t_2 , FWD is forward biased, it starts conducting, and, consequently, I_C starts decreasing. Therefore, V_{GE} falls rapidly to zero and below: Now, $I_C = I_{\text{BJT}}$ since $I_{\text{MOS}} = 0$. Then, dV_{CE}/dt is no longer constant, but also decreases since it is fixed by dynamic avalanche at the P-body junction [29]–[31], eventually showing a nearly flat region in the V_{CE} peak. This stressing working condition finishes when I_L only passes through FWD and I_C becomes zero due to the carriers' recombination mechanisms. At this point, V_{CE} falls abruptly to the nominal input value V_{DC} .

The experimental results corresponding to a failed overcurrent turnoff process are shown in Fig. 3(b). In the inspected IGBT modules, the failure is characterized by the fact that V_{CE} is not sustained at V_{DC} after its overshoot and it falls toward zero (as also observed in [25]), while I_C starts increasing again. Notice that, in Fig. 3(b), the device is turned off (I_C is zero), but suddenly, a slight increment in I_C appears. Moreover, the flat region in the voltage overshoot previously observed in Fig. 3(a) disappears. This behavior may be attributed to breakdown of a single or few IGBT cells (local breakdown). In such a situation, the critical electric field at the body-base junction may be reached at lower applied voltages because of the dynamic avalanche condition (electrically generated carriers) [19], [31] and the working local temperature (thermally generated carriers). This local effect was also suggested in the case of bipolar freewheeling diodes [32]. Subsequently, at the failed IGBT cells, the leakage current rises, leading to a hot-spot formation. From this overheated region, the heat flux radially diffuses to the neighboring cells, inducing the same electrothermal effect. When a critical temperature value is locally reached, the second breakdown phenomenon occurs, i.e., the device loses the blocking voltage capability. Consequently, V_{CE} collapses, turning off the freewheeling diodes. Therefore, the failed IGBT devices not only share the current I_L fixed by the load but also they withstand the high current from the diode reverse recovery, thus inducing a latch-up phenomenon. In the analyzed case, we observe from Fig. 3(b) that V_{GE} rises up at the same time that V_{CE} collapses. This fact suggests that a failure on the gate driver is induced by an overcurrent coming from the gate terminal (gate oxide breakdown).

On the other hand, Fig. 3(c) and (d) shows the results for a safe and a failed overtemperature turnoff transition, respectively. As can be inferred from Fig. 3(d), the failure signature on

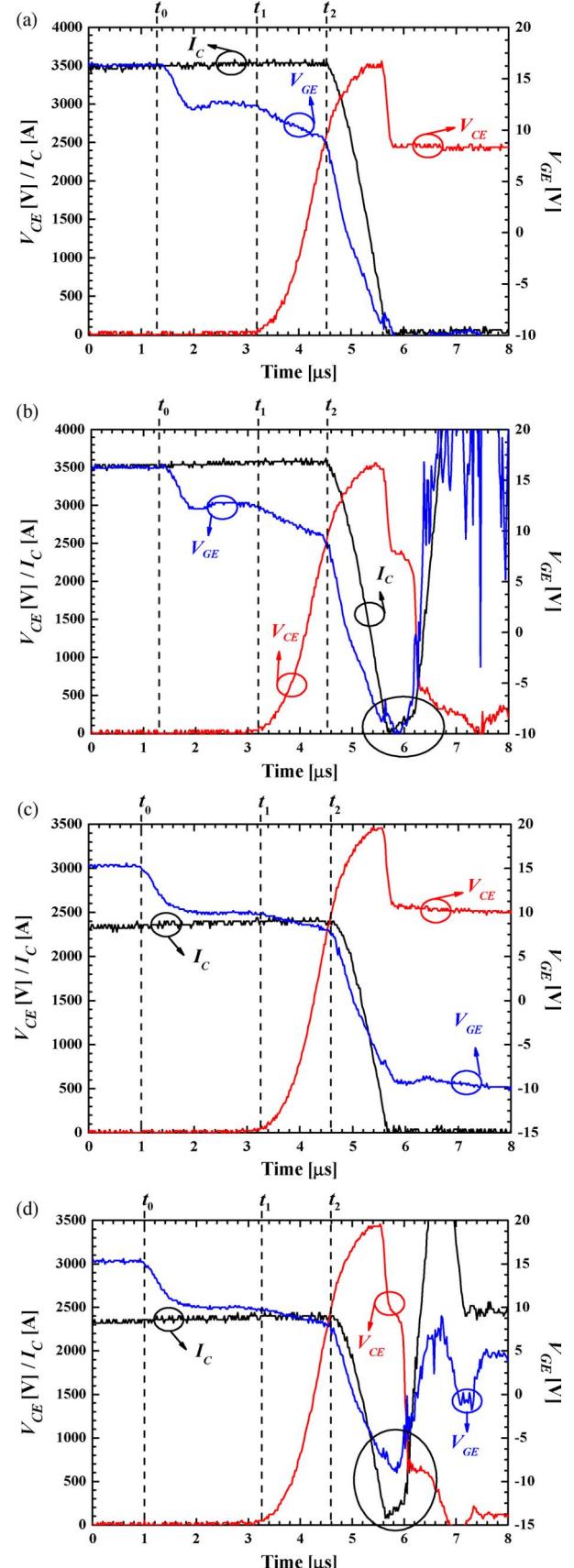


Fig. 3. Experimental current and voltage waveforms for (a) safe and (b) failure-affected overcurrent turnoff transitions. Experimental current and voltage waveforms for (c) safe and (d) failure-affected overtemperature turnoff transitions.

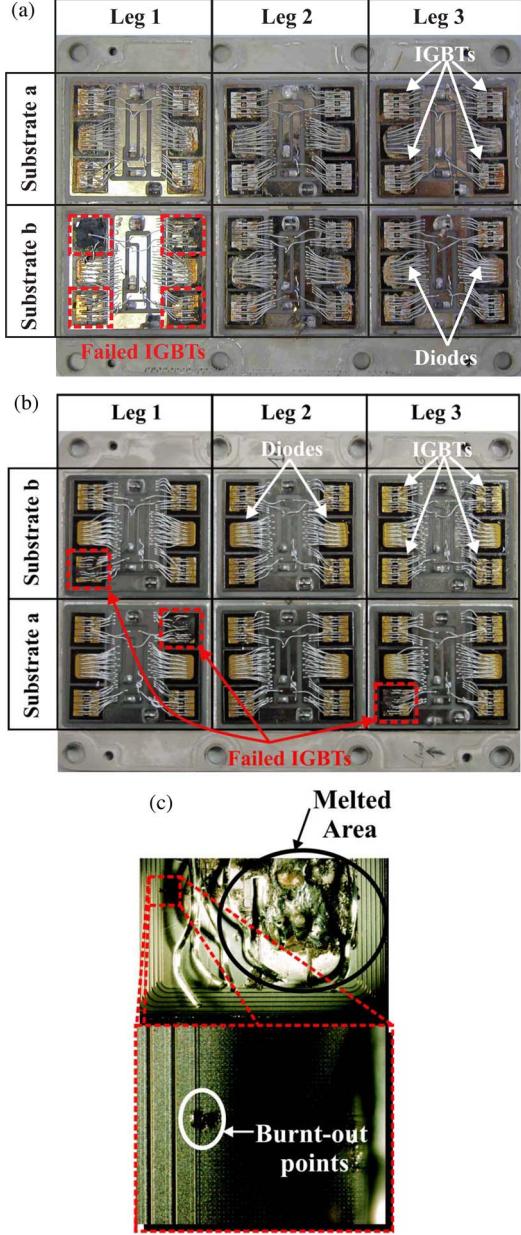


Fig. 4. Photographs of a failed IGBT module during a turnoff process when an (a) overcurrent or (b) overtemperature event occurs. (c) Zoom of the detected failure signatures in an IGBT.

the electrical waveforms, i.e., I_C increase when the IGBTs are completely turned off, is the same as in the previous case of an overcurrent turnoff process. The only difference is attributed to the body junction breakdown mainly due to thermally generated carriers. This fact indicates that the hot-spot formation is the most likely origin of the failure in both cases, eventually leading to a thermal runaway.

B. Damages Observed Within Multichip Modules

Fig. 4(a)–(c) shows some photographs related to the destroyed modules during the robustness tests. Fig. 4(a) and (b) shows the failed modules when an overcurrent or overtemperature event has occurred, respectively. In both events, the visual inspection of the failed power module reveals that its

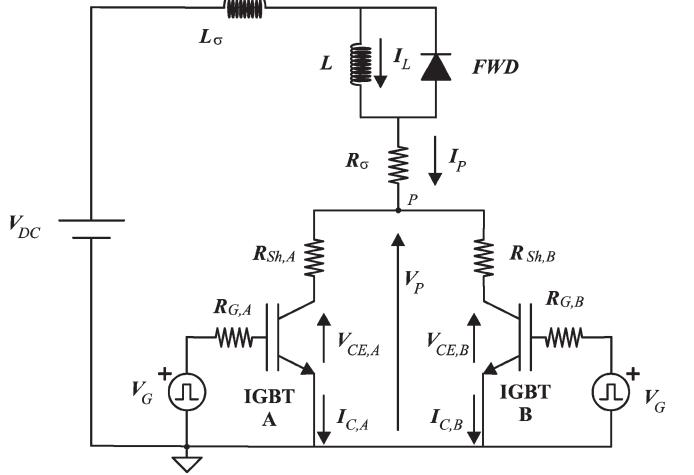


Fig. 5. Schematic of the simulation-assisted approach followed to emulate the failure conditions. $R_{G,A} = 68 \Omega$, $R_{G,B} = 12.5 \Omega$, $R_{Sh,A} = 0.09 \Omega$, $R_{Sh,B} = 0.01 \Omega$, and $R_\sigma = 0.01 \Omega$, leading to $\Delta t_{turnoff} = 1.3 \mu\text{s}$ and a current-sharing ratio of 1/9 between IGBTs A and B.

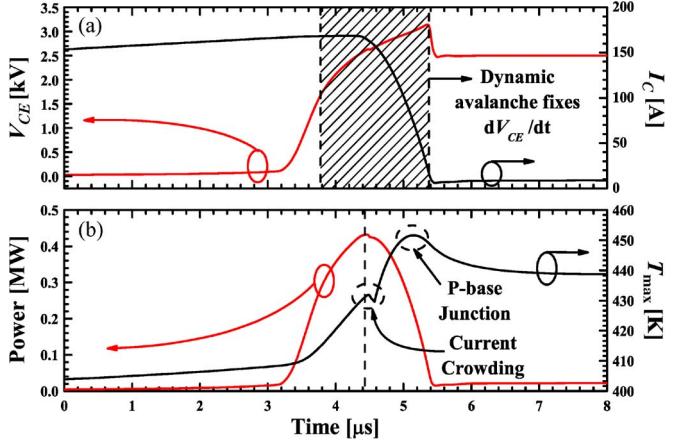


Fig. 6. (a) Simulated waveforms corresponding to the current and collector-to-emitter voltage during the turnoff process, also highlighting the region where dynamic avalanche injection fixes dV_{CE}/dt . (b) Evolution of the maximum temperature and the dissipated power.

loss of functionality is due to a limited number of failed IGBT transistors, thus indicating that the current-sharing or temperature distribution is highly nonuniform during this event. Consequently, the instantaneous power dissipated by the IGBT devices differs.

In the case of the overcurrent event, the same failure pattern was observed repeatedly, in which the parasitical elements establish the position of the failed IGBTs [devices in the Leg 1 substrate (a)]. This suggests the need to carefully consider electrothermal mismatches among the chips and all possible sources of current-sharing imbalances. This study has been carried out in previous works [33], [34], in which both the package parasitical and nonuniform thermal effects have been taken into account. These studies put in evidence that an uneven current sharing between IGBTs determines the most electrothermally stressed devices. Moreover, the destruction of an individual IGBT normally gives rise to the subsequent destruction of other self-heated adjacent IGBTs through which the current must flow. Concerning the overtemperature case, the affected devices

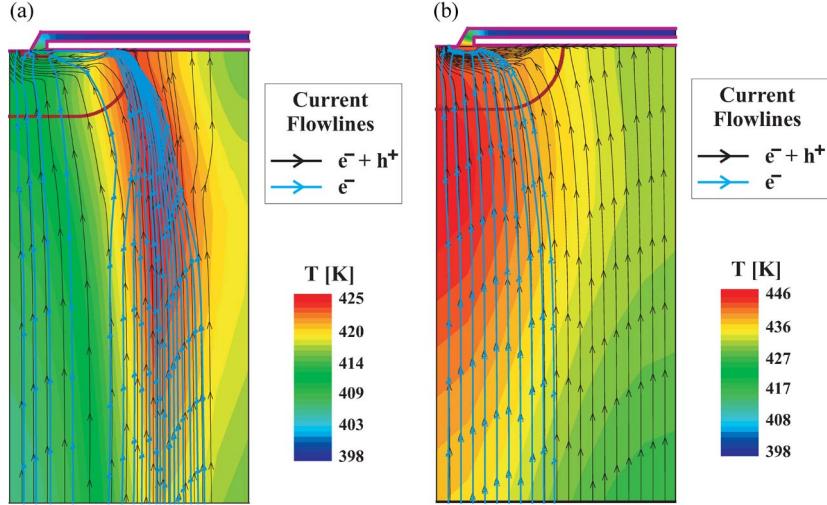


Fig. 7. Cross section corresponding to the simulated IGBT half cell, depicting the temperature distribution and current flow lines (total, electrons) (a) before diode forward biasing and (b) near the end of the turnoff.

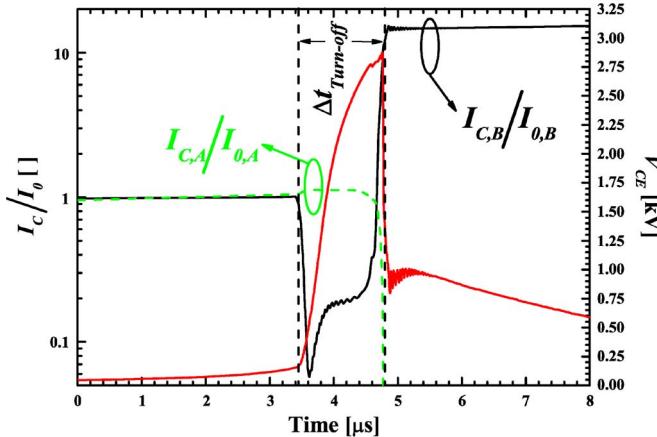


Fig. 8. Simulated turnoff waveforms (current for each half cell and voltage drop) under overcurrent conditions.

are randomly distributed [see Fig. 4(b)], since this is a thermally generated process. The failed devices are located at Leg 1, substrates (a) and (b), and at Leg 3 substrate (a).

Fig. 4(c) shows an example of the failure pattern repeatedly observed in both cases. This figure shows huge melted areas on the pads and burnt-out points at the end of the gate runner in the vicinity of the device edge termination [35], revealing a hot-spot formation at this location. These signatures have also been reported in [10]. This is related to the fact that the cell structure symmetry is broken at both the edge termination and gate runner zones. In these areas, the electric field is higher than that of the device core, since the last IGBT cells have no neighboring IGBT cells around their periphery, thus making these regions the weakest point of the device. The huge melted areas from Fig. 4(c) are related with the high-voltage level passed through the emitter pads, which leads to device explosion. This failure is extremely linked to the operation temperature, and the hot-spot location is related to the dynamic breakdown of the P-body junction in a localized number of IGBT cells. This fact reinforces the hypothesis of initial local hot-spot formation that will lead to a mesoplasma

generation, eventually provoking the second breakdown [36]. Once the second breakdown occurs, the diode is turned off. As a consequence, a high current coming from the diode reverse recovery must flow through the IGBT, producing the burnt-out zones and cavities (craters) in the region of the emitter pad [36].

III. FAILURE DISCUSSION

A. Failure Simulation Approach

Physical simulations with Sentaurus TCAD tools [37] have been performed to qualitatively validate the failure hypothesis (IGBT dynamic breakdown). The simulation strategy has been focused on creating an electrothermal instability by an overcurrent event in an individual single IGBT. For this purpose, IGBT half cells have been used (see Fig. 2). Another possibility would have consisted in reproducing the overtemperature event by performing transient simulations, in such a way that the device temperature is gradually increased until the failure observation. However, the last approach will not reveal whether the failure under overcurrent conditions is thermally or current density driven.

First of all, the simulation input parameters have been set to fit the simulation predictions to the experimental static and dynamic characteristics. Afterward, two different simulations have been performed: one with a single IGBT half cell (stable case; Fig. 1) and another with two mismatched structures (unstable case; see schematic in Fig. 5). In the stable case, the behavior of a current constriction during turnoff is analyzed, but the failure is not observed since it is not possible to unbalance the current. In the second case, a simulation strategy is introduced to account for a current and temperature mismatching between either two IGBT half cells or two IGBT devices inside the module, which allow observing the breakdown in one of them. The current mismatching has been introduced by considering different initial temperatures (T_A and T_B) and a delay in the turnoff instants ($\Delta t_{\text{turnoff}}$). Thereby, the increase of the leakage current with temperature in IGBT B is considered, thus modeling the thermally generated carriers

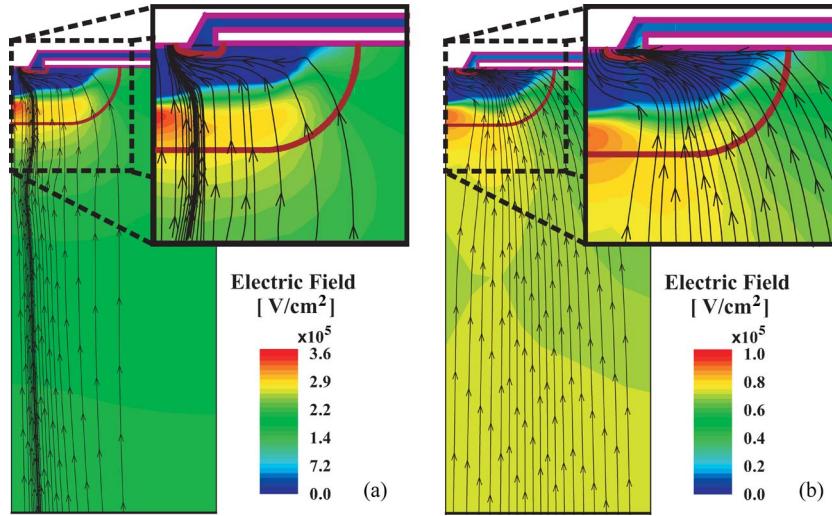


Fig. 9. Cross section corresponding to the simulated IGBT half cell A, presenting the electric field distribution and current flow lines during the failure: (a) Thermally assisted junction breakdown (the failure instant) and (b) a latch-up mechanism (resulting from the failure).

within the drift region. In this simulation, IGBT A is less electrothermally stressed than IGBT B. Namely, T_A ($125\text{ }^\circ\text{C}$) is lower than T_B ($190\text{ }^\circ\text{C}$), and IGBT A is turned off after IGBT B. It is worth to remark that the electrothermal mismatch has been stressed to show how the failure occurs. This situation cannot be reproduced following a simulation approach based on a single IGBT cell, since the simulation package does not allow setting the appropriate boundary conditions with the purpose of taking into account the analyzed mismatching [30]. In both simulation approaches, the SPICE model corresponding to the real freewheeling diode has been chosen to reduce the computation time. The temperature and current values have been extracted from other performed simulations, in which the module stray elements were considered following the approach shown in [34].

B. Comparison of Simulation and Experimental Results

Fig. 6 shows the I_C , V_{CE} , the maximum temperature (T_{\max}), and the dissipated power for the stable simulated IGBT turnoff process, also highlighting the region where dynamic avalanche fixes dV_{CE}/dt [see Fig. 6(a)]. The maximum dissipated power takes place when high-current and high-voltage levels simultaneously coexist across the device. During this process, T_{\max} presents two peaks, eventually decreasing to an almost constant level. Each peak is related to the heat source location within the IGBT basic cell during the turnoff process. For the first peak, previous to the diode's turn-on, dissipation is mainly due to the current constriction produced at the end of the MOS channel. Once I_L flows through the diode and the IGBT channel is cut off, power dissipation is produced below the body–base planar junction as a result of the hole flow (shortest path to the emitter).

Fig. 7 shows both mentioned phenomena: current constriction and hot-spot formation (a) when the channel is on and (b) when the current is supported by holes. In these figures, the current due to both carriers and only electrons is also highlighted (black and blue solid lines, respectively). Fig. 7(b) shows the aforementioned presence of carriers (mainly holes) close to the body–base junction, which are increased due to the inductive

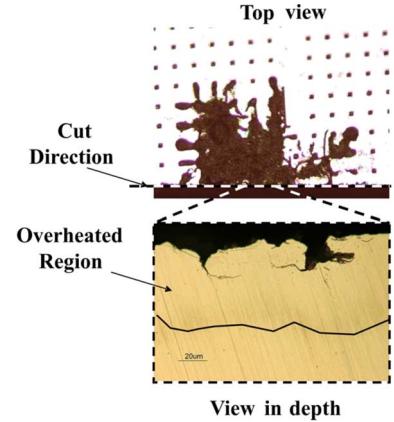


Fig. 10. Top view of the failure and its corresponding cross section, showing the melted and burnt-out areas.

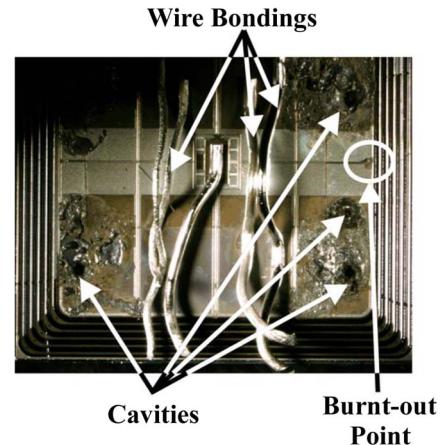


Fig. 11. Detail of a failed IGBT device, highlighting the small burnt-out spots close to IGBT edge termination and the cavities in the melted regions.

load discharge (dynamic avalanche-generated carriers) and the local temperature increase (thermally generated carriers). Under these conditions, the critical electric field to locally break down this junction would be reached at lower V_{CE} values (dynamic breakdown voltage), depending on the local temperature.

Consequently, the IGBT cell affected by this phenomenon will show a less resistive path, giving rise to a current crowding and a hot-spot formation (regenerative feedback). When the hot spot's temperature overcomes a certain critical value, the second breakdown occurs, leading to the V_{CE} collapse and the ensuing current increase across the device (latch-up). Fig. 8 partly shows these phenomena, showing V_{CE} and the currents for IGBTs A and B ($I_{C,A}$ and $I_{C,B}$) normalized to their ON-state values ($I_{0,A}$ and $I_{0,B}$). In this case, the junction breakdown is due to the leakage current that is thermally generated, as can be observed in the failed I_C waveform in Fig. 3(b).

Fig. 9 shows the electric field distribution and the current flow lines inside IGBT B at time instants corresponding to (a) the failure and (b) the subsequent latch-up. Fig. 9(a) shows the junction breakdown once the IGBT is completely turned off. Fig. 9(b) shows a latch-up destruction mechanism due to the parasitic thyristor activation (IGBT B takes all the current from IGBT A and from the load), once the second breakdown condition is reached. The results shown in Fig. 9(b) do not depict the loss of control on the gate terminal (see V_{GE} signal) observed in Fig. 3(b), since not all possible phenomena involved in the failure process can be taken into account in the present simulation.

Microsections and chemical etchings have been performed on the failed IGBT devices to determine whether the defect is located at the surface or in depth. Fig. 10 shows the microsection results from a failed device. In this figure, it can be observed how the failure event occurs in the device bulk (located at 50- μm depth), which is in accordance with the performed simulations [see Fig. 9(a)]. According to the simulation results, the hot spot produced by the current constriction (due to junction breakdown) is not in agreement with the latch-up destruction mechanism, since the signature related to a second breakdown takes place inside the drift region (junction breakdown). The latch-up failure is observed behind the wire bonding areas melted by a huge current, as shown in Fig. 11. As mentioned before, this current corresponds to the diode reverse recovery induced by the V_{CE} collapse, which turns off the freewheeling diode. Moreover, Fig. 11 shows the melted areas with cavities, which gives evidence of the mesoplasma formation and the ensuing current filamentation [16], [38], [39] coinciding with the final latch-up phenomenon.

IV. CONCLUSION

The operation of IGBT modules used in power inverters is affected by abnormal events which impose severe stresses on the devices, particularly on IGBT devices. At this point, the converter robustness should be capable to avoid the IGBT transistor destruction (e.g., by using current discharging branches for both the induction discharge and diode reverse recovery processes). Having a higher physical insight into the failure is useful to foresee possible design problems and to evaluate the influence of various circuit parameters. In addition, the followed simulation methodology should be rigorous to obtain reliable results, which would perfectly reflect the real failure mechanism. It is worthy to remark that, in this kind of failures, the temperature contribution (thermally generated carriers) has

more relevance in high-voltage devices, since its base doping level is lower than their medium- and low-voltage counterparts. Even the reported failure would be more important when using IGBT modules with higher breakdown capabilities than in the present work. Hence, special care should be taken into account during the converter thermal management design to avoid high-temperature working conditions for high-voltage IGBT modules. On the other hand, the reduction of the thermomechanical mismatch in multichip modules with new available materials should be also envisaged.

REFERENCES

- [1] M. Mermet-Guyennet, X. Perpiñà, and M. Piton, "Revisiting power cycling test for better lifetime prediction in traction," *Microelectron. Reliab.*, vol. 47, no. 9–11, pp. 1690–1695, Sep.–Nov. 2007.
- [2] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*, 2nd ed. New York: Wiley, Apr. 1995.
- [3] A. Steimel, "Direct self-control and synchronous pulse techniques for high-power traction inverters in comparison," *IEEE Trans. Ind. Electron.*, vol. 51, no. 4, pp. 810–820, Aug. 2004.
- [4] A. Bouscayrol, M. Pietrzak-David, P. Delarue, R. Peña-Eguiluz, P.-E. Vidal, and X. Kestlyn, "Weighted control of traction drives with parallel-connected ac machines," *IEEE Trans. Ind. Electron.*, vol. 53, no. 6, pp. 1799–1806, Dec. 2006.
- [5] B. K. Bose, "Power electronics and motor drives recent progress and perspective," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 581–588, Apr. 2006.
- [6] H. Baumann, P. Heinemeyer, W. Staiger, M. Töpfer, K. Unger, and D. Müller, "Optimized cooling systems for high-power semiconductor devices," *IEEE Trans. Ind. Electron.*, vol. 48, no. 2, pp. 298–306, Apr. 2001.
- [7] G. Malagoni-Buiatti, J. A. Martín-Ramos, C. H. Rojas-García, A. M. R. Amaral, and A. J. Marques Cardoso, "An on-line and non-invasive technique for the condition monitoring of capacitors in boost converters," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 8, pp. 2134–2143, Aug. 2010.
- [8] T. Lhommeau, X. Perpiñà, C. Martin, R. Meuret, M. Mermet-Guyennet, and M. Karama, "Thermal fatigue effects on the temperature distribution inside IGBT modules for zone engine aeronautical applications," *Microelectron. Reliab.*, vol. 47, no. 9–11, pp. 1779–1783, Sep.–Nov. 2007.
- [9] X. Perpiñà, A. Castellazzi, M. Piton, M. Mermet-Guyennet, and J. Millán, "Failure-relevant abnormal events in power inverters considering measured IGBT module temperature inhomogeneities," *Microelectron. Reliab.*, vol. 47, no. 9–11, pp. 1784–1785, Sep.–Nov. 2007.
- [10] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectron. Reliab.*, vol. 42, no. 4/5, pp. 653–667, Apr./May 2002.
- [11] A. K. Khargekar and P. P. Kumar, "A novel scheme for protection of power semiconductor devices against short circuit faults," *IEEE Trans. Ind. Electron.*, vol. 41, no. 3, pp. 344–351, Jun. 1994.
- [12] F. Weitzsch, "A discussion of some known physical models for second breakdown," *IEEE Trans. Electron Devices*, vol. ED-13, no. 11, pp. 731–734, Nov. 1966.
- [13] H. B. Grutchfield and T. J. Moutoux, "Current mode second breakdown in epitaxial planar transistors," *IEEE Trans. Electron Devices*, vol. ED-13, no. 11, pp. 743–748, Nov. 1966.
- [14] B. S. Khurana and T. Sugano, "Thermal breakdown in silicon p-n junction devices," *IEEE Trans. Electron Devices*, vol. ED-13, no. 11, pp. 763–770, Nov. 1966.
- [15] K. Hane and T. Suzuki, "Effect of injected current on current-mode second breakdown in Silicon PNN + structure," *Jpn. J. Appl. Phys.*, vol. 14, no. 12, pp. 1961–1968, Dec. 1975.
- [16] V. A. Vashchenko and V. F. Sinkevitch, *Physical Limitations of Semiconductor Devices*. New York: Springer-Verlag, 2008.
- [17] M. Domeij, B. Breitholtz, L. M. Hillkirk, J. Linnros, and M. Östling, "Dynamic avalanche in 3.3-kV Si power diodes," *IEEE Trans. Electron Devices*, vol. 46, no. 4, pp. 781–786, Apr. 1999.
- [18] G. K. Wachutka, "Analytical model for the destruction mechanism of GTO-like devices by avalanche injection," *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1516–1523, Jun. 1991.
- [19] J. Lutz and M. Domeij, "Dynamic avalanche and reliability of high voltage diodes," *Microelectron. Reliab.*, vol. 48, no. 4, pp. 529–536, Apr. 2003.
- [20] M. Domeij, J. Lutz, and D. Silber, "On the destruction limit of Si power diodes during reverse recovery with dynamic avalanche," *IEEE Trans. Electron Devices*, vol. 50, no. 2, pp. 486–493, Feb. 2003.

- [21] J. Oetjen, R. Jungblut, U. Kuhlmann, J. Arkenau, and R. Sitting, "Current filamentation in bipolar power devices during dynamic avalanche breakdown," *Solid State Electron.*, vol. 44, no. 1, pp. 117–123, Jan. 2000.
- [22] H. Egawa, "Avalanche characteristics and failure mechanism of high voltage diodes," *IEEE Trans. Electron Devices*, vol. ED-13, no. 11, pp. 754–758, Nov. 1966.
- [23] M. Trivedi and K. Shenai, "Failure mechanisms of IGBT's under short-circuit and clamped inductive switching stress," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 108–116, Jan. 1999.
- [24] A. Kopta, M. Rahimo, U. Schlapbach, N. Kaminski, and D. Silber, "Limitation of the short-circuit ruggedness of high-voltage IGBTs," in *Proc. ISPSD*, Barcelona, Spain, Jun. 2009, pp. 33–36.
- [25] C. C. Shen, A. R. Hefner, Jr., D. W. Berning, and J. B. Bernstein, "Failure dynamics of the IGBT during turnoff under unclamped inductive loading conditions," *IEEE Trans. Ind. Appl.*, vol. 36, no. 2, pp. 614–624, Mar./Apr. 2000.
- [26] K. Heumann and M. Quenou, "Second breakdown and latch-up behavior of IGBT's," in *Proc. EPE*, Brighton, U.K., Sep. 1993, vol. 4, pp. 301–305.
- [27] B. J. Baliga, *Power Semiconductor Devices*. Boston, MA: PWS Publishing Company, 1996.
- [28] A. Porst, F. Auerbach, H. Brunner, G. Debay, and F. Hille, "Improvement of the diode characteristics using emitter-controlled principles (EMCON diode)," in *Proc. ISPSD*, Weimar, Germany, May 1997, pp. 213–216.
- [29] P. Lefranc, D. Planson, H. Morel, and D. Bergogne, "Analysis of the dynamic avalanche of punch through insulated gate bipolar transistor (PT-IGBT)," *Solid State Electron.*, vol. 53, no. 9, pp. 944–954, Sep. 2009.
- [30] P. Rose, D. Silber, A. Porst, and F. Pfirsch, "Investigations on the stability of dynamic avalanche in IGBTs," in *Proc. ISPSD*, Santa Fe, NM, Jun. 2002, pp. 165–168.
- [31] T. Ogura, H. Ninomiya, K. Sugiyama, and T. Inoue, "Turn-off switching analysis considering dynamic avalanche effect for low turn-off loss high-voltage IGBTs," *IEEE Trans. Electron Devices*, vol. 51, no. 4, pp. 629–635, Apr. 2004.
- [32] M. T. Rahimo and N. Y. A. Shammas, "Freewheeling diode reverse-recovery failure modes in IGBT applications," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 661–670, Mar./Apr. 2001.
- [33] R. De Maglie, G. Lourdel, P. Austin, J.-M. Dienot, J.-L. Schanen, and J.-L. Sanchez, "Use of accurate chip level modeling and analysis of a power module to establish reliability rules," in *Proc. ISIE*, Montreal, QC, Canada, Jul. 2006, pp. 1571–1576.
- [34] A. Castellazzi, M. Ciappa, W. Fichtner, G. Lourdel, and M. Mermet-Guyennet, "Compact modelling and analysis of power-sharing unbalances in IGBT-modules used in traction applications," *Microelectron. Reliab.*, vol. 46, no. 9–11, pp. 1754–1759, Sep.–Nov. 2006.
- [35] X. Perpiñà, J. F. Serviere, X. Jordà, A. Fauquet, S. Hidalgo, J. Urresti-Ibañez, J. Rebollo, and M. Mermet-Guyennet, "IGBT module failure analysis in railway applications," *Microelectron. Reliab.*, vol. 48, no. 8/9, pp. 1427–1431, Aug./Sep. 2008.
- [36] T. Puritis, "Problems related to the avalanche and secondary breakdown of silicon P-N junctions," *Microelectron. Reliab.*, vol. 35, no. 5, pp. 713–719, May 1997.
- [37] TCAD TOOL Suite. Synopsys, Mountain View, CA, 2006. [Online]. Available: <http://www.synopsys.com/products/tcad/tcad.html>
- [38] D. J. Rose, "Microplasmas in silicon," *Phys. Rev.*, vol. 105, no. 2, pp. 413–418, Jan. 1957.
- [39] S. K. Ghandhi, *Semiconductor Power Devices*. New York: Wiley, 1977, pp. 1–32.



Xavier Perpiñà was born in Almenar, Spain, in 1976. He received the B.S. degree in physics, the M.Phil. degree in electronic engineering, and the Ph.D. degree from the Universitat Autònoma de Barcelona, Bellaterra, Spain, in 1999, 2002, and 2005, respectively.

In 1999, he was with the Instituto de Microelectrónica de Barcelona, Centro Nacional de Microelectrónica, Consejo Superior de Investigaciones Científicas, Bellaterra, where he worked in the clean room, began his research activity with the Power Devices and Systems Group in 2005, and is currently a Contracted Researcher. From 2005 to 2007, he was with Alstom Transport Tarbes, Séméac, France, where he developed studies on thermal management and power-converter reliability. He has authored and coauthored more than 50 research papers in international conferences and journals.



Jean-François Serviere was born in 1953. He received the B.S. degree in electrical engineering from Institut National des Sciences Appliquées de Lyon, Lyon, France.

He joined Alstom Transport (formerly Traction CEM–Oerlikon), Villeurbanne, France, in 1982. He worked on the design of two series gate turn-off thyristor (GTO) choppers of the Spanish high-speed train (AVE) in 1986 and other GTO-based railway choppers and inverters. After that, he moved to Alstom Transport Tarbes, Séméac, France. Since 1998, he has been in charge of the reliability testing and failure analysis of bipolar power semiconductor devices coming from the field. His current fields of interest are the physical modeling and numerical simulation of the observed failures in insulated-gate bipolar transistors and diodes in real railway inverters, as well as electrical tests at the limit of high-power multichip modules. Moreover, he is also involved in developing experimental setups for accelerated ageing tests addressed to high-power multichip modules for railway traction applications.



Jesús Urresti-Ibañez was born in Zaragoza, Spain, in 1976. He received the B.S. degree in physics and the Ph.D. degree from Universidad Autónoma de Barcelona, Bellaterra, Spain, in 1999 and 2008, respectively.

From 2001 to 2005, he was with the Power Devices and Systems Group, Instituto de Microelectrónica de Barcelona, Centro Nacional de Microelectrónica (IMB-CNM), Consejo Superior de Investigaciones Científicas (CSIC), Bellaterra. His work was focused on the study of transient voltage suppressor for low-voltage applications. From 2006 to 2008, he was with Alstom Transport Tarbes, Séméac, France, where he studied the reliability of power multichip modules. Its research activity was focused on the determination of the reverse-blocking safe operating area of insulated-gate bipolar transistors. He is currently a Contracted Researcher with IMB-CNM, CSIC. He has authored and coauthored more than 25 research papers in conferences and journals. His research interests are the modeling, design, fabrication, and characterization of power devices.



Ignasi Cortés received the M.Sc. degree and the Ph.D. degree in electronic engineering from the Universitat Politècnica de Catalunya, Barcelona, Spain, in 2002 and 2008, respectively.

From 2003 to 2008, he was with the Instituto de Microelectrónica de Barcelona, Centro Nacional de Microelectrónica (IMB-CNM), Consejo Superior de Investigaciones Científicas (CSIC), Bellaterra, Spain, where he was involved in RF power device design optimization in bulk and silicon-on-insulator (SOI) technologies. In 2008, he joined the Intégration de Systèmes de Gestion de l'Énergies Group, Laboratoire d'Analyse et d'Architecture des Systèmes, Centre National de la Recherche Scientifique, Toulouse, France, where he worked on LDMOS transistors for the new generation of Smart-Power technology and on TCAD modeling and characterization of different configurations of MOS test structures in GaN substrate. He is currently with the Power Device Group, IMB-CNM, CSIC. His research of interests are in RF power semiconductor devices in silicon (bulk and SOI) and GaN technologies, TCAD (Synopsys and Silvaco) modeling, characterization and fabrication processes, and microengineering.



Xavier Jordà was born in Barcelona, Spain, in 1967. He received the B.S. degree from the Universitat Autònoma de Barcelona, Bellaterra, Spain, in 1990 and the Ph.D. degree from the Institut National des Sciences Appliquées de Lyon, Lyon, France, in 1995.

From 1990 to 1995, he was with the Centre de Génie Électrique de Lyon, Equipe de Composants de Puissance et Applications, Lyon, where he worked on vector control of induction motors, three-phase pulsewidth-modulation methods, and ac drives. Since 1995, he has been with the Power Devices and Systems Group, Instituto de Microelectrónica de Barcelona, Centro Nacional de Microelectrónica, Consejo Superior de Investigaciones Científicas, Bellaterra. He has authored and coauthored more than 100 research papers in journals and conferences. His current research activity deals with the thermal management, modeling, and electrothermal characterization of power semiconductor devices and systems.



Salvador Hidalgo was born in Granada, Spain, in 1961. He received the B.S. and Ph.D. degrees in physics from the Autonomous University of Barcelona, Bellaterra, Spain, in 1986 and 1990, respectively.

In 1987, he joined the Instituto de Microelectrónica de Barcelona, Centro Nacional de Microelectrónica, Consejo Superior de Investigaciones Científicas, Bellaterra, as a Member of the Power Devices and Systems Group, specializing in the development of power devices with MOS gate control in vertical, lateral, and trench configurations. He also works in the field of surge protection power semiconductor devices with high (thyristor)- and low (Zener)-voltage capabilities. He is the author of 45 publications in international journals, 130 communications to international congresses (five received the prize for the best paper), and nine units in international collective volumes.



Jose Rebollo was born in 1959. He received the B.S. and Ph.D. degrees in physics from the Autonomous University of Barcelona, Bellaterra, Spain, in 1982 and 1987, respectively.

He was an Assistant Professor with the Autonomous University of Barcelona, teaching electronics and physics as well as postgraduate microelectronic courses. In 1989, he joined the Power Devices and Systems Group, Instituto de Microelectrónica de Barcelona, Centro Nacional de Microelectrónica, Consejo Superior de Investigaciones Científicas, Bellaterra, where he has been working on the physics, technology, modeling, and reliability of power semiconductor devices. He has published more than 200 papers in scientific journals and conferences, and is the holder of several patents in these fields. He has participated and managed several EU-funded projects and industrial contracts, including technology transfer, as well as R&D projects funded by the Spanish administration.



Michel Mermet-Guyennet was born in 1957. He received the B.S. degree from the Ecole Centrale de Paris, Paris, France, in 1981 and the Ph.D. degree in physics from the Université de Marseille, Luminy, France, in 1984.

He was successively with Thomson Militaire et Spatial, SGS-Thomson, Advanced Computer Research Institute, and Compagnie des Signaux, where he was in charge of the R&D programs in the field of electronic components and system hardware. He has been with Alstom Transport Tarbes, Sémeac, France, since 1996, where he has been the Technical Director of the Power Electronics Associated Research Laboratory since 2001. He is the holder of several patents in the field of power integration.