

RMS Current Balancing of Parallel SiC Bridge Arms based on a Rotational Rest Control Strategy

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Abstract—Silicon carbide MOSFETs face challenges due to on-resistance variability, leading to an imbalanced RMS current distribution among parallel converter bridge arms. To address this imbalance, both passive and active methods have previously been reported. However, passive methods are often costly and offer little flexibility in adjusting the balancing ratio, whereas existing active methods either rely on expensive customized gate drivers or interfere with the primary control loop. In this paper, we proposed an active method for arm-level RMS current balancing based on a rotational rest control strategy. The proposed method reduces hardware costs by using only standard gate drivers and is decoupled from the primary control loop. Simulation and experimental results demonstrate that the proposed method achieves high balancing accuracy in various numbers of arms and maintains a rapid balancing response.

Index Terms—silicon carbide (SiC), parallel operation, current balancing, consensus control

I. INTRODUCTION

SILICON carbide (SiC) MOSFETs are promising alternatives to silicon (Si) IGBTs for low-voltage high-power converters due to their significantly lower switching losses and higher switching frequency capabilities [1], [2], [3]. These characteristics lead to performance improvements, such as higher overall efficiency and lower total harmonic distortion (THD). However, the production of SiC substrates and epitaxial layers faces challenges due to defects such as micropipes, dislocations, and stacking faults [4]. These manufacturing imperfections lead to significant inconsistencies in the critical parameters of SiC MOSFETs, such as the threshold voltage and the on-resistance, causing an imbalanced current distribution between parallel arms [5]. Additionally, as a result of thermal management and space optimization, it is possible that the converter has an asymmetric power circuit layout and length mismatches in the power cables, introducing parasitic parameter inconsistencies that further degrade the current balancing in parallel arms.

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For low-voltage applications with a device breakdown voltage around 1200V, economically priced, high-current Si IGBTs have been widely supplied by manufacturers, largely mitigating the need for parallel-arm topologies. In contrast, although commercially mass-produced SiC MOSFETs can also reach 1200V in terms of breakdown voltage [6], their current-carrying capability is comparatively limited for the same price. High-current or high-voltage SiC MOSFETs are still too costly for widespread commercial use, thereby motivating the adoption of parallel topologies [7], [8], [9]. As a result of manufacturing difficulties, the parameter inconsistency for SiC MOSFETs is generally greater than that of Si IGBTs, causing more severe balancing issues. With the production of 1200V SiC MOSFETs becoming increasingly mature, the cost of regular rating switches (e.g. 30mΩ and 30-50A) is no longer the dominant component of converter hardware expenses. However, the cost associated with current and thermal balancing processes remains high.

The imbalance of currents in parallel arms can be categorized into two types: dynamic and static imbalances [10]. The dynamic current imbalance is mainly caused by mismatched threshold voltages, but also differences in on-resistances [11]. This issue results in uncoordinated switching and short-term current stress spikes, raising transient safety concerns [12]. Comparatively, the static current imbalance is mainly due to mismatched on-resistances, leading to heat generation imbalances, long-term junction temperature differences, and eventually to the asynchronous aging of SiC MOSFETs [6]. Together, these imbalance issues damage the reliability and lifespan of SiC MOSFET-based converters and pose significant challenges to long-life equipment, such as battery energy storage systems, electric vehicles, and renewable energy sources [13]. As potting with thermal conductive gels becomes increasingly adopted in mature products for thermal management, replacement of individual MOSFETs becomes extremely difficult, let alone the challenge of performing frequent maintenance across a large number of deployed products.

In this paper, our focus is on the static current (RMS) imbalance issue in parallel arms composed of SiC MOSFETs. Existing RMS current balancing methods for parallel arms can be categorized into passive and active methods. Passive methods generally focus on parameter screening, ancillary components, and layout optimizations. Reference [14] proposed a min-max fit criterion for the screening of on-resistance, taking temperature drift into the screening to improve accuracy. Although screening methods are widely adopted in industrial applications, they inevitably increase

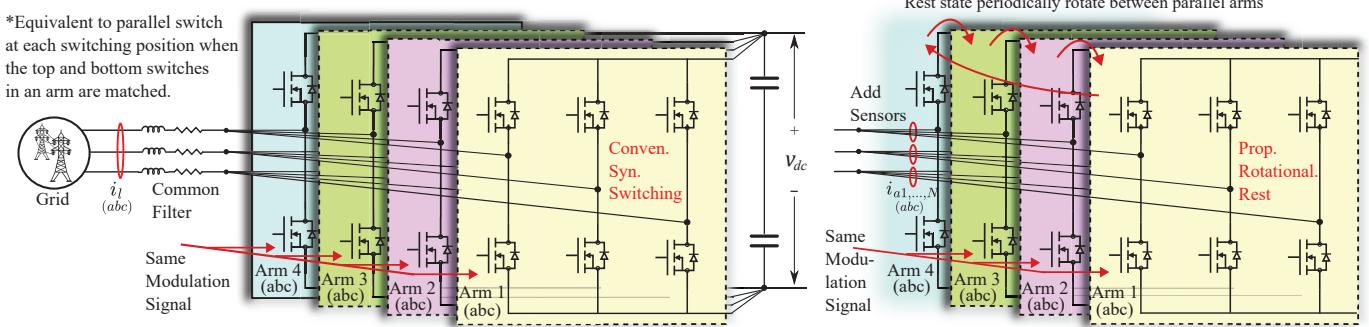


Fig. 1. A common two-level, four-parallel-arm, and SiC MOSFET-based inverter topology in low-voltage systems under synchronized switching control and the proposed rotational rest control.

production costs and introduce quality control challenges in commercial mass production. Furthermore, screening methods cannot compensate for parameter mismatches caused by asymmetric layouts and cable length variations. The method of adding coupled inductors in parallel arms is discussed in [15] and [16]. Unlike dynamic current balancing, where the induced inductance diminishes after the switching transient, the use of coupled inductors for RMS current balancing results in persistent induced inductance during steady states, which leads to elevated switch-off voltage spikes. Besides, this method is not expand-friendly as the design complexity of coupled inductors increases significantly with the number of parallel arms. Reference [17] suggested that the RMS current imbalance can be mitigated by adjusting the inductance of the power cables. Although mathematically possible, this method is parameter-sensitive and time-consuming in real-world applications. Another method of adjusting the inductance of bus bars through a laminated structure is proposed in [18], which faces challenges similar to the former method. In [19], a circuit layout optimization method was proposed for RMS current balancing through simulations in Maxwell3D, but this method is useful only after modeling the converter geometry and electrical behaviors, which can be difficult in reality.

Whereas passive methods operate without corrective intervention for different operating conditions, active methods implement feedback-controlled regulation to balance the arm RMS currents and gain control over the balancing ratio. Multilevel active gate drivers (AGD) for RMS current balancing were discussed in [20], [21]. By modulating the on-time of each voltage level, RMS current balancing can be achieved, albeit at the cost of increased gate driver complexity and expenses for the additional MOS switches used. Continuous control AGDs are proposed in [22], [23], where gate voltages are modulated by pulse-width modulation (PWM) of two fixed voltage rails. The RMS current balancing issue can also be solved by a dedicated control loop in the converter controller rather than the gate driver. Reference [24] proposed master-slave and references [25], [26], [27] proposed uniform reference control structures for RMS current balancing. Both methods derive compensation signals proportional to the measured current imbalance in each arm, and subsequently integrate these compensation signals into the modulation references of

the primary control loop. Although this method eliminates hardware modifications like in AGD methods and offers a rapid balancing response, its current balancing loop is coupled to the primary control loop, allowing oscillations and noise from the current balancing control loop to affect the stability and reliability of the primary control functions.

The literature review identifies significant limitations in both passive and active RMS current balancing methods for industrial applications. To bridge this gap, an ideal balancing method for low-voltage SiC converters should address three requirements simultaneously: (1) a decoupled control structure to prevent interfering the primary control loop; (2) optimized costs and complexity for commercial mass production; (3) flexible balancing ratios and rapid transient response to adapt the modulation speed of low-voltage converters. In this paper, we proposed a method to achieve active arm-level RMS current balancing through a rotational rest control strategy. The rest periods of individual arms are dynamically modulated using a PI-based consensus control algorithm [28], [29], which is widely used in navigation of swarm robotics, state-of-the-charge balancing of batteries, and microgrid control. By constructing a specific rest sequence, precise and flexible RMS current balancing can be achieved for parallel arms. Compared with the existing methods, the proposed method leads to the following main contributions.

- The proposed method is decoupled from the primary control loop while maintaining rapid balancing response, guaranteeing uncompromised voltage/current regulation capability at the point of common coupling (PCC) - even under unstable conditions in the balancing control loop.
- The proposed method provides active RMS current balancing with programmable balancing ratios using industrial standard gate drivers, while the associated hardware costs and induced losses scale inversely with the number of parallel arms.

This paper is organized as follows. Section II provides the theoretical details of the proposed method. Section III presents simulation results to evaluate the improvement of the proposed method. Section IV contains experimental results to verify the real-world performance of the proposed method. Finally, Section V gives the conclusion of this paper.

TABLE I
COMPARISON OF DIFFERENT OPTIONS FOR HANDLING RMS CURRENT IMBALANCE ON A 100kW SiC MOSFET ($\pm 14\% R_{ds}$ MISMATCH) INVERTER

Method	Ref.	Extra Hardware (\$)	Extra PCB Space (cm ²)	Overload Ability	Advantages	Disadvantages
Derating without balancing	N/A	• 284 (3 arms) • 473 (5 arms) • 661 (7 arms)	• 7 (3 arms) • 11 (5 arms) • 15 (7 arms)	★ (Hot spot)	• Do nothing about balancing • No additional hardware • PCC unaffected	• Hot spot exists • Wasting MOSFET ratings • Balancing error increase with time • Overcurrent risk in transients
MOSFET Screening and Picking	[14]	Depends (labor & equipment)	None	★★	• Straightforward • No additional hardware • PCC unaffected by balancing	• No programmable ratios • Labor-intensive with high costs • Yield loss/scrap • Parameter sensitive
Power Circuit Optimization	[17], [18], [19]	Depends (labor & equipment)	Depends (design)	★★	• Straightforward • No additional hardware • PCC unaffected by balancing	• No programmable ratios • Labor-intensive with high costs • Unit-by-unit tuning • Parameter sensitive
Inductive Coupling Balancing	[15], [16]	• 18 (3 arms) • 36 (5 arms) • 54 (7 arms)	• 5 (3 arms) • 10 (5 arms) • 16 (7 arms)	★ (Higher losses)	• Low hardware costs • PCC unaffected by balancing • Help dynamic balancing	• No programmable ratios • Complex to expand • Increased arm losses and switching voltage spikes • Steady-state error
Modulation Signal Intervention	[24], [25], [26], [27]	• 26 (3 arms) • 42 (5 arms) • 59 (7 arms)	• 13 (3 arms) • 22 (5 arms) • 31 (7 arms)	★ (High PCC THD)	• Fast balancing • Programmable ratios • Low hardware costs	• Limited mismatch tolerance at high/low switching duty cycles • Low PCC power quality • Balancing instability affects PCC
Multi-level /Continuous Control AGDs	[20], [21], [22], [23]	• 553 (3 arms) • 922 (5 arms) • 1290 (7 arms)	• 125 (3 arms) • 208 (5 arms) • 291 (7 arms)	★★★	• Ultra-fast balancing • Programmable ratios • High mismatch tolerance • Help dynamic balancing	• Sensitive to EMI • High hardware cost • Proportional expansion cost • Balancing instability affects PCC
Rotational Rest Control (Proposed)	This one	• 146 (3+1 arms) • 163 (5+1 arms) • 180 (7+1 arms)	• 52 (3+1 arms) • 61 (5+1 arms) • 70 (7+1 arms)	★★ ★★ (Extra arms)	• Fast balancing • Programmable ratios • Low expansion cost • PCC unaffected by balancing	• Higher arm losses than balanced case with same arm numbers • Relatively lower mismatch tolerance than AGD

Price and Space Reference: **Normal Drive Module:** BM61S41RFV-EVK002, 24.88\$, 33.0 × 32.0mm²; **Multi-level AGD Module:** 2ASC-12A2HP-DC, 86.31\$, 61.0 × 40.0mm²; **1200V, 77A SiC MOSFET:** NTBG030N120M3S, 6.30\$, 10.2 × 4.7mm²; **1200V, 102A SiC MOSFET:** NTH4L020N120SC1, 22.04\$, 15.8 × 5.2mm²; **100A, 500kHz Hall-effect current sensor:** TMCS1148, 2.79\$, 13.0 × 11.1mm²; **50A, 100nH Coupled Inductor:** ATL-1Z120705SR10MT, 2.96\$, 12.0 × 7.0mm².

II. THE PROPOSED METHOD

In this paper, we select the two-level parallel arm inverter topology (Fig. 1) commonly employed in low-voltage SiC MOSFET-based applications as an example. The presented paralleling topology is functionally equivalent to switch-level paralleling at each switching position, provided that consistency within each arm is maintained. It adopts a different wiring configuration to reduce the number of current sensors, as the control focuses solely on arm-level current balancing. In this paper, we assumed that the on-resistance difference between the upper and lower MOSFETs in any arm is negligible ($\leq 5\%$). A larger mismatch results in an increased harmonic distortion and the emergence of a DC component in the arm currents, thereby reducing the balancing capability of the proposed method in terms of the maximum allowable mismatch to achieve full current balancing.

To enable the rotational rest mechanism while preventing arm overload, a redundant arm is introduced into the parallel group, whose structure is identical to the existing ones. With the redundant arm, the proposed control strategy can temporarily deactivate one of the parallel arms for RMS current

regulation, as demonstrated in Fig. 2, and periodically rotate the rest condition among all parallel arms, as illustrated in Fig. 3 for a 3+1 parallel group, where T_{r1-4} are the rest periods and T_c is the rotation cycle. By enforcing a strict rotational rest sequence and regulating the rest periods of all parallel arms, RMS current balancing can be achieved while ensuring uninterrupted voltage/current control at the PCC. The default balancing ratio is set to unity (1:1:...:1) across all parallel arms, though it can be adjusted as needed. The proposed rotational rest control method is compared with other mainstream balancing methods in Table I for a 100kW inverter scenario. From the table, the proposed method provides a fast balancing response, programmable current-sharing ratios, and robust PCC power quality and stability, while requiring only a modest additional hardware cost and PCB space. It overcomes the key limitations of the modulation signal intervention method while requiring significantly less hardware cost than AGD methods.

The theoretical details of the proposed method are introduced in the following three sub-Sections.

- Section II-A involves describing the concept and charac-

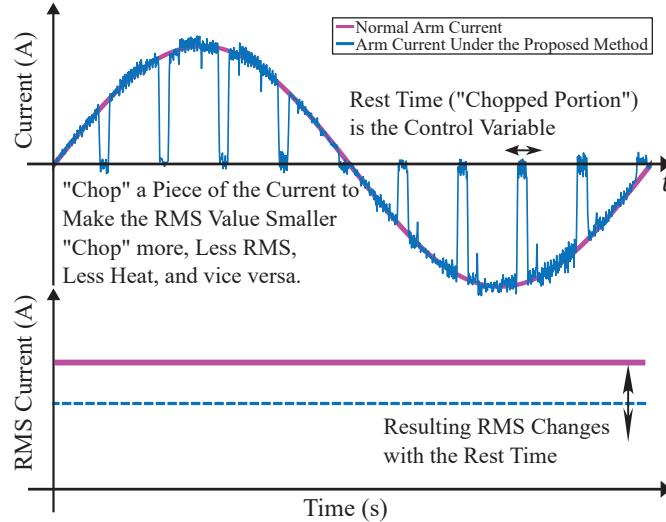


Fig. 2. A simple demonstration of the RMS regulation mechanism used by the proposed method.

teristics of rotational rest control and deriving the base vector of rest periods for parallel arms based on the on-resistances of their constituent SiC MOSFETs at room temperature.

- Section II-B discusses the implementation challenges of the proposed method, including transitional current surges between rest periods, interference from freewheeling current pulses during switching deadtimes, and junction temperature variations caused by current cycling.
- Section II-C presents a closed-loop control strategy to regulate rest periods, ensuring a reliable convergence of all arms' RMS currents to a uniform state (or other programmed ratios) with arm currents as feedback signals.

A. The Rotational Rest Mechanism

With the traditional synchronized switching method, the modulation signals for all arms are identical within a given phase of the three-phase inverter. If parasitic parameters are omitted, the fundamental RMS current distribution (50Hz component) among all arms is given by Eq. (1):

$$I_{ai} = I_t \frac{1}{\sum_{j=1}^N \frac{1}{R_{aj}}} = I_t \frac{1}{R_{ai}} \frac{1}{\sum_{j=1}^N \frac{1}{R_{aj}}}, \quad (1)$$

where I_t is the total fundamental RMS current of the parallel group, I_{ai} and R_{ai} are the fundamental RMS current and the on-resistance of the i^{th} arm, respectively. As previously mentioned, this study assumes negligible parametric differences among MOSFETs within each arm, which means that the on-resistance of each arm is considered equivalent to that of its constituent MOSFETs.

Under the rotational rest control strategy, an arm's current is zero during its rest periods. However, when an arm is active, its parallel peers change periodically as other arms enter their respective rest periods in a sequence, as illustrated in Fig. 3. Note that each time the parallel peers change, the RMS current

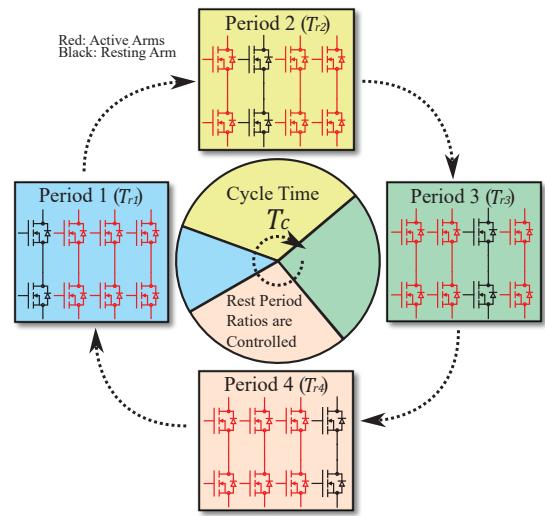


Fig. 3. Illustration of the proposed rotational rest mechanism.

distribution of the group changes. Therefore, the calculation of the fundamental RMS current of an individual arm is rest period-based. Assuming the i^{th} arm rests in period T_{ri} , the fundamental RMS current of the i^{th} arm I_{ai} is given by Eq. (2):

$$I_{ai} = \frac{1}{T_c} \sum_{k=1, k \neq i}^N I_{ai,rk} T_{rk}, \quad (2)$$

where $I_{ai,rk}$ is the fundamental RMS current of the i^{th} arm during the rest period T_{rk} . Note that the resting arm in any rest period has to be excluded from the calculation of the fundamental RMS current distribution, which results in the current distribution given by Eq. (3):

$$I_{ai,rk} = \frac{I_t}{R_{ai}} \frac{1}{\sum_{j=1, j \neq k}^N \frac{1}{R_{aj}}}, \quad k \neq i. \quad (3)$$

Combining Eqs. (2) and (3), we derive the representation of I_{ai} as a function of the vector of all rest periods $\vec{T}_r \in \mathbb{R}^{N \times 1}$ in Eqs. (4) and (5):

$$I_{ai}(\vec{T}_r) = \frac{I_t}{R_{ai} T_c} \sum_{k=1, k \neq i}^N \frac{T_{rk}}{\sum_{j=1, j \neq k}^N \frac{1}{R_{aj}}}, \quad (4)$$

$$\vec{T}_r = [T_{r1}, T_{r2}, \dots, T_{rN}]^T. \quad (5)$$

Once the mathematical relationships in Eqs. (4) and (5) are established, the subsequent task is to solve the optimal base vector of the rest periods $\vec{T}_r^* \in \mathbb{R}^{N \times 1}$. This is achieved by solving Eqs. (6)-(8):

$$\frac{\vec{I}_a}{I_t} = \frac{\vec{1}_N}{N}, \quad (6)$$

$$\vec{1}_N^T \vec{T}_r^* = T_c, \quad (7)$$

$$\vec{I}_a = [I_{a1}(\vec{T}_r^*), I_{a2}(\vec{T}_r^*), \dots, I_{aN}(\vec{T}_r^*)]^T, \quad (8)$$

where $\vec{I}_a \in \mathbb{R}^{N \times 1}$ is a vector of fundamental RMS currents of all arms and $\vec{1}_N$ is a N -dimensional unit vector. The solution

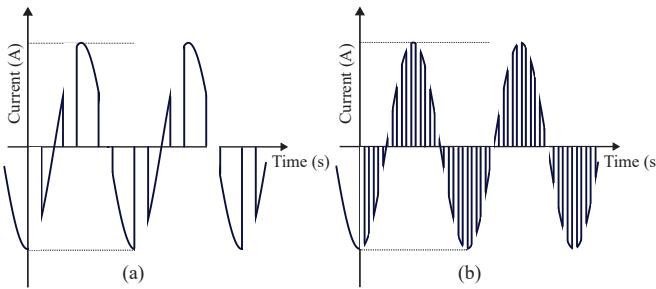


Fig. 4. General arm current waveform under different rotation cycles (peer alternation effects not shown): (a) long cycle; (b) short cycle.

to Eqs. (6)-(8) is in p.u. of T_c , and therefore all rest periods are determined after choosing an appropriate rotation cycle. The rotation cycle substantially impacts the current waveform in each arm, as evidenced in Fig. 4. Although a shorter rotation cycle helps mitigate oscillations in RMS current measurements and relax subsequent filtering requirements, it also increases switching losses and exacerbates the detrimental effect of rest-transition deadtimes. These side-effects are explained later in this Section and Section II-B.

The cycling between the rest and active status of parallel arms is controlled through a series of PWM signals $g_{r1,2,\dots,N}$. These PWM signals serve as triggers that determine whether to propagate the primary control PWM signal vector for one phase $\vec{g}_c \in \mathbb{B}^{2 \times 1}$ (2-level) to each individual arm. As a result, the actual PWM signal vector that goes to the i^{th} arm $\vec{g}_{ai} \in \mathbb{B}^{2 \times 1}$ is obtained through Eq. (9):

$$\vec{g}_{ai} = \begin{cases} \vec{0}_2, & g_{ri} = \text{high} \\ \vec{g}_c, & \text{else} \end{cases}. \quad (9)$$

The rotational rest control periodically interrupts the arm current by disabling the arm MOSFETs, which inevitably increases the THD of the arm currents, leading to an increase in conduction losses of the parallel group. For simplicity, we assume that the current level changes due to peer alternations are neglected. The true RMS current of the i^{th} arm \mathcal{I}_{ai} , accounting for all harmonics, is therefore given by Eq. (10):

$$\begin{aligned} \mathcal{I}_{ai} &= \sqrt{\frac{1}{T_g} \int_0^{T_g} \left(1 - \frac{T_{ri}}{T_c}\right) \left[K_i \sin\left(\frac{2\pi}{T_g} t\right)\right]^2 dt} \\ &\approx \frac{K_i}{\sqrt{2}} \sqrt{1 - \frac{T_{ri}}{T_c}}, \quad \forall T_c \ll T_g, \end{aligned} \quad (10)$$

where K_i is the current amplitude of the i^{th} arm and T_g is the nominal power period (20ms). With the proposed method, consider $\mathcal{I}_{a1} = \mathcal{I}_{a2} = \dots = \mathcal{I}_{aN}$ in steady states, which leads to the relationship given by Eq. (11):

$$\frac{K_i}{K_1} = \sqrt{\frac{T_c - T_{r1}}{T_c - T_{ri}}} = \alpha_i, \quad (11)$$

where α_i is an intermediate ratio variable. In addition, the fundamental RMS current of the i^{th} arm is given by Eq. (12):

$$I_{ai} = \frac{K_i}{\sqrt{2}} \left(1 - \frac{T_{ri}}{T_c}\right). \quad (12)$$

The conduction loss increment in the parallel group, ΔP_{cl} , introduced by the proposed method, is determined by the square of the current increment, as expressed in p.u. in Eq. (13):

$$\Delta P_{cl} = \left(\frac{\sum_{i=1}^N \mathcal{I}_{ai}}{\sum_{i=1}^N I_{ai}} \right)^2 - 1 = \left(\frac{N \sqrt{1 - \frac{T_{r1}}{T_c}}}{\sum_{i=1}^N \alpha_i \left(1 - \frac{T_{ri}}{T_c}\right)} \right)^2 - 1. \quad (13)$$

The numerical solutions of ΔP_{cl} show that the distribution of $T_{r1,2,\dots,N}$ imposes a minor effect on ΔP_{cl} and the dominant factor is N . For example, if there are 4, 6, and 8 parallel arms, true RMS current increment roughly equals 15%, 9%, and 7%, and therefore ΔP_{cl} equals 34%, 19%, and 14%, respectively, indicating that ΔP_{cl} decreases as N increases. This also causes the current rating requirements for SiC MOSFETs to differ from those under traditional synchronized switching control. Taking into account the specific characteristics of the rotational rest control, the new minimum required current rating per arm, denoted as I_{MOS}^{ppr} , can be estimated using the empirical relationship provided in Eq. (14):

$$I_{MOS}^{ppr} = \frac{S_{max}}{3NV_g} \left(1 + \frac{0.809}{N^{1.182}}\right), \quad (14)$$

where S_{max} is the maximum apparent power of the inverter and V_g is the grid voltage in RMS. Note that in practical applications, an additional 10–15% redundancy margin should be ensured on top of I_{MOS}^{ppr} .

The proposed method alters the switching pattern, thereby affecting the overall switching loss as well. For a total number of N parallel arms, the synchronized switching method continuously switches N arms, while the proposed method continuously switches only $N - 1$ arms. This leads to a difference in the magnitude of the switching current between the two methods. As a result, the switching energies of active MOSFETs under the proposed method must be scaled up from the values of the synchronized switching method ($E_{on,off}^{con}$, benchmark). Moreover, although the resting arm remains off in the proposed method, its MOSFET still contributes an effective output capacitance, C_{oss} . Consequently, the total output capacitance in the parallel group that must be charged and discharged during each switching transient remains NC_{oss} . This implies that even though only $N - 1$ arms are actively switched, an additional output capacitance loss (E_{oss}) from the resting arm must still be accounted for. Note that E_{oss} losses of the active arms are already included in their $E_{on,off}$. Assuming that the switching energies are linearly proportional to the drain current according to the datasheet, the average turn-on and turn-off energies per MOSFET under the proposed method, $E_{on,off}^{ppr}$, are given by Eq. (15):

$$\begin{aligned} E_{on,off}^{ppr} &= \frac{(N - 1)E_{on,off}^{con} \frac{I_t/(N - 1)}{I_t/N} + E_{oss}}{N - 1} \\ &= \frac{NE_{on,off}^{con} + E_{oss}}{N - 1}, \end{aligned} \quad (15)$$

In addition, at each transition between rest periods, the previously resting arm is activated while the pre-resting arm

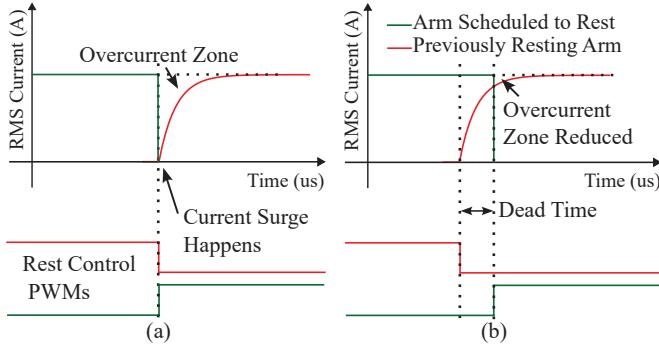


Fig. 5. Illustration of the rest-transition deadtime between rest periods: (a) without any deadtime; (b) with a suitable deadtime.

is deactivated. This action introduces one set of extra turn-on and turn-off energy losses per transition between rest periods, which should be counted in the total switching loss. Combining all mentioned effects, the total switching loss increment caused by the proposed method in p.u., ΔP_{sl} , is as given by Eq. (16):

$$\begin{aligned} \Delta P_{sl} &= \frac{\frac{(N-1)(E_{on}^{ppr}+E_{off}^{ppr})}{T_{sw}} + \frac{N(E_{on}^{ppr}+E_{off}^{ppr})}{T_c}}{\frac{N(E_{on}^{con}+E_{off}^{con})}{T_{sw}}} - 1, \\ &= \frac{NT_{sw}}{T_c(N-1)} + \frac{2E_{oss}}{N(E_{on}^{con}+E_{off}^{con})} \left(\frac{NT_{sw}}{T_c(N-1)} + 1 \right), \quad (16) \end{aligned}$$

where T_{sw} is the switching period of the MOSFETs. Since SiC MOSFET inverters typically switch between 50kHz to 100kHz [30] [31] [32] [33], we consider a T_{sw} of 1/80kHz and a T_c of 2ms. Using a commercial SiC MOSFET module (C3M0032120K) as an example, with a DC bus voltage of 800V, a benchmark switching current of 40A per MOSFET, the datasheet specifies switching energies of E_{on}^{con} (367μJ), E_{off}^{con} (123μJ), and E_{oss} (55μJ). Under these conditions, for 4, 6, and 8 parallel arms, the corresponding ΔP_{sl} are approximately 6.5%, 4.5%, and 3.5%, respectively, indicating that ΔP_{sl} decreases as N increases.

B. Implementation Challenges

For each transition between rest periods, it is imperative that the previously resting arm is reactivated slightly prior to the deactivation of the pre-resting arm. If this is violated, the parallel group temporarily loses two of its current-sharing arms, as illustrated in the overcurrent region of Fig. 5(a). Such a condition leads to a redistribution of the total load current among a reduced number of active arms, resulting in current surges in all remaining arms. The induced instantaneous current surge ratio β is given by Eq. (17):

$$\beta = \frac{N-1}{N-2}. \quad (17)$$

According to Eq. (17), β decreases as N increases ($N \geq 3$).

To alleviate these current surges, it is essential to implement deadtimes in each transition between rest periods, as illustrated in Fig. 5(b). This rest-transition deadtime should be sufficiently long to allow the current of the reactivated arm

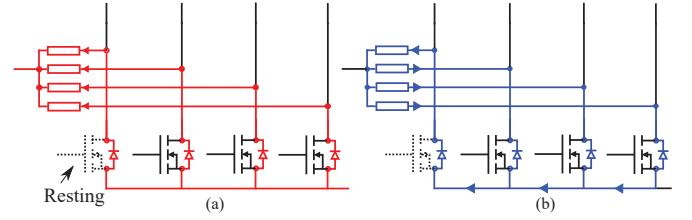


Fig. 6. Free-wheeling current flow in the parallel arm group while one arm is in the rest mode: (a) total free-wheeling current flow; (b) circulating pulses.

to approach its full activation level, but not excessively long to significantly compromise the rotational rest sequence. The fundamental RMS current of the previously resting arm during the reactivation process is given by Eq. (18):

$$I_{ai}(t) = I_{ai,r(i+1)} \left(1 - e^{-\frac{R_{ai}}{L_{ai}} t} \right), \quad (18)$$

where L_{ai} is the total parasitic inductance within the i^{th} arm. From Eq. (18), we can write the theoretical minimum requirement of the rest-transition deadtime T_d^{rtr} as given by Eq. (19):

$$T_d^{rtr} \geq -\frac{\bar{L}_a \ln(1-\gamma)}{\bar{R}_a}, \quad (19)$$

where γ is the desired percentage of current rising, \bar{L}_a and \bar{R}_a are average parameters for all parallel arms. As the implementation of T_d^{rtr} slightly compromises the rest sequence, the T_d^{rtr}/T_c ratio should be tuned to balance the control accuracy and the surge magnitude. An suggestion of experiences for selecting T_d^{rtr} is 0.5-1% of T_c .

During the calculation of T_d^{rtr} , we only considered the inertia from arm parasitic inductance and assumed an ideal MOSFET turn-on time. However, if the switching frequency is not fast enough, this turn-on time may not be negligible. This delay slows the current rise in the previously resting arm and effectively forces an increase in rest-transition deadtimes to maintain the intended performance. However, the increased deadtimes must still remain within a certain fraction of the rotation cycle period T_c to avoid a significant impact on the balancing accuracy. Therefore, the turn-on time tolerance, which leads to an estimation of the MOSFET switching period limit T_{sw}^{max} , can be calculated with Eq. (20) once T_c and T_d^{rtr} are obtained:

$$\kappa T_{sw}^{max} = \frac{\epsilon T_c}{N} - T_d^{rtr}, \quad (20)$$

where κ is the percentage of turn-on time in the switching period (typical $\leq 3\%$), and ϵ is the distortion percentage tolerance of the rotation cycle (typical $\leq 5\%$).

Free-wheeling current pulse interference presents another practical issue that impacts the balancing accuracy of the proposed control strategy. This arises from the fact that the free-wheeling diode is not controllable via the gate driver. During switching deadtimes of MOSFETs, the diode in the resting arm conducts a portion of the total free-wheeling current, as illustrated in Fig. 6(a). This introduces unintended interference in the resting arm, which compromises the intended zero current state. During positive (outward) half-cycles of the 50 Hz current, this interference becomes high-frequency circulating

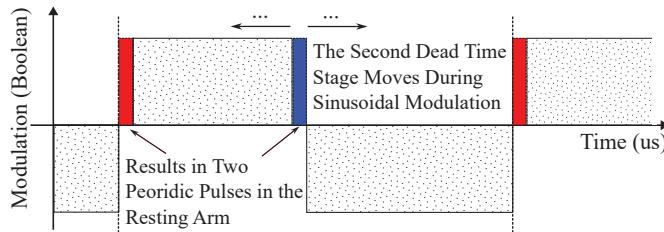


Fig. 7. The content of the circulating current pulses.

current pulses through the lower diode of the resting arm, as shown in Fig. 6(b). This disturbance mechanism exhibits symmetric behavior during negative (inward) half-cycles.

By examining the causes of circulating pulse interference in a resting arm, it is evident that these pulses are the combination of two asymmetric square waves if there is no arm inductance. This behavior can be attributed to the presence of two switching deadtimes within each switching period, as shown in Fig. 7. These asymmetric square waves exhibit a period equal to the switching period and pulse widths determined by the fixed switching deadtime. This causes the arm RMS current to increase in p.u. as given by Eq. (21):

$$\frac{\Delta I_{ai}}{I_{ai}} = \frac{1}{I_{ai}} \sqrt{\frac{1}{T_g} \int_{\frac{T_g}{T_{sw}}}^{\frac{T_g}{T_{sw}} + 2T_d^{sw}} \left[K_i \sin \left(\frac{2\pi}{T_g} t \right) \right]^2 dt} \approx \sqrt{\frac{2T_{ri}T_d^{sw}}{(T_c - T_{ri})T_{sw}}}, \quad \forall T_c \ll T_g, \quad (21)$$

where T_d^{sw} is the switching deadtime of MOSFETs. If $T_d^{sw} \ll T_{sw}$, the interference from circulating pulses can be neglected.

The last practical challenge of the proposed method involves the thermal impact of current cycling on the interior of SiC MOSFETs. Because the rotational rest control periodically switches between the active and rest states, the MOSFET junction undergoes repeated heating and cooling cycles, which may potentially damage the bond wire integrity. To evaluate the severity of this effect, we use a verified Cauer model from [34] for a typical 1200V/55A discrete SiC MOSFET module (APTM120AM55CT1AG by Microsemi), as illustrated in Fig. 8. The analysis considers a test scenario with a 50°C heatsink temperature, a switching current of 50A during active times, a 2ms rotation cycle, and a 25% (T_c) rest period. Fig. 9 shows the calculated temperature variations on the SiC die, revealing a temperature variation of 4.7°C at a frequency of 500Hz. The corresponding lifetime impact under this current cycling fatigue can be estimated using the Coffin–Manson model [35], and the results confirm that the proposed method introduces a negligible impact on the lifetime of the SiC MOSFETs.

C. Closed-loop Regulation of Rest Periods

In Section II-A, \vec{T}_r^* is calculated, but this vector only ensures a high balancing accuracy for the fundamental RMS currents. To balance the harmonics induced by the rotational rest control and accommodate varying operating conditions, closed-loop regulation of all rest periods is required. As

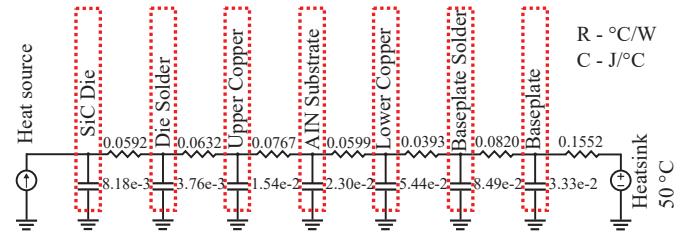


Fig. 8. A Cauer model for a SiC MOSFET (APTM120AM55CT1AG) [34].

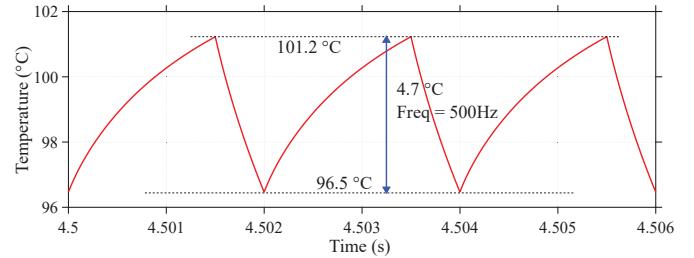


Fig. 9. SiC MOSFET Junction temperature variations due to rotational rest mechanism.

established in Section II-A, all rest periods must occur sequentially with a sum equal to the rotation cycle. Consequently, any modification to one arm's rest period necessitates equal compensations for all other arms, as given by Eq. (22):

$$T_{ri} = T_{ri}^* + \Delta T_{ri} - \sum_{j=1, j \neq i}^N \frac{\Delta T_{rj}}{N-1}, \quad (22)$$

where ΔT_{ri} is the rest period regulation signal of the i^{th} arm. The real-time calculation of ΔT_{ri} is based on the feedback of filtered true RMS currents of parallel arms. In this paper, we adopt a PI-based consensus control algorithm to calculate ΔT_{ri} . Consensus control is initially invented as a distributed approach in which each agent updates its state based on interactions with neighboring agents, ensuring that the states of all agents converge to a consensus equilibrium over time. In this paper, each arm can be seen as an agent and, because of pure local control, all other arms can be seen as its neighbors without communications. However, this part can also be replaced by conventional balancing control algorithms with reduced transient performance, such as master-slave control. Based on the PI-based consensus algorithm, the controller of the i^{th} arm updates its ΔT_{ri} output with the law given by Eq. (23) and the saturation law given by Eq. (24):

$$\Delta T_{ri} = k_p^{syn} \sum_{j=1}^N (\mathcal{I}_{ai}^f - \mathcal{I}_{aj}^f) + k_i^{syn} \int \sum_{j=1}^N (\mathcal{I}_{ai}^f - \mathcal{I}_{aj}^f) dt, \quad (23)$$

$$\Delta T_{ri} = \begin{cases} \Delta T_r^{max}, & \Delta T_{ri} \geq \Delta T_r^{max} \\ \Delta T_{ri}, & -\Delta T_r^{max} < \Delta T_{ri} < \Delta T_r^{max} \\ -\Delta T_r^{max}, & \Delta T_{ri} \leq -\Delta T_r^{max} \end{cases}, \quad (24)$$

where \mathcal{I}_{ai}^f is the filtered true RMS current of the i^{th} arm and ΔT_r^{max} is the control saturation limit. The resultant control block diagram of the overall inverter system is shown in Fig. 10, where v_g and i_g are the voltage and current measurements at the PCC, v_c is the modulation reference of

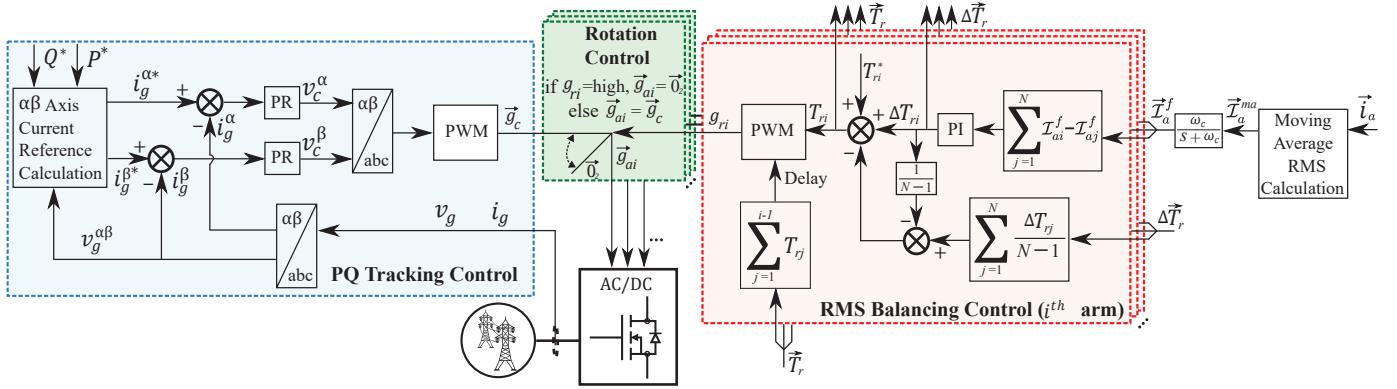


Fig. 10. Control block diagram of a two-level parallel-arm inverter system with the primary control loop and the RMS current balancing control loop.

the inverter output voltage, P^* and Q^* are the active and reactive power references, \vec{i}_a is the arm current measurement vector, \vec{I}_a^{ma} is the output of the true RMS calculations, and ω_c is the cut-off frequency of the low-pass filter.

The rotational rest control strategy modifies the parallel connection pattern of arms while remaining fully decoupled from the primary control loop. This structural independence ensures that the stability and dynamic performance of the primary control loop are preserved. However, the PI gains of the consensus controller still govern the current balancing convergence characteristics of all parallel arms. Improper selection of these PI gains could trigger unstable oscillations in all rest periods, which destroy the current balancing functionality. These PI gains should be designed on the basis of analyzing the dynamic model of the balancing control loop. For simplicity, this dynamic model is derived based on the fundamental RMS currents, since including higher-order current harmonics contribute negligibly to the stability analysis.

Assuming all rest period regulation signals are within saturation limits, according to Eqs. (22) and (23), the discrete state-space representation of the PI-based consensus balancing controller is given by Eqs. (25) and (26):

$$\vec{x}_b(k+1) = \vec{x}_b(k) + \mathbf{B}_b \vec{I}_a^f(k), \quad (25)$$

$$\vec{T}_r(k) = \mathbf{C}_b \left[k_i^{syn} \vec{x}_b(k) + k_p^{syn} \mathbf{B}_b \vec{I}_a^f(k) \right] + \vec{T}_r^*, \quad (26)$$

where $\vec{x}_b \in \mathbb{R}^{N \times 1}$ is the state vector of the balancing controllers, T_s^{syn} is the time step of the balancing control loop, and matrices $\mathbf{B}, \mathbf{C}_b \in \mathbb{R}^{N \times N}$. The control action vector $\vec{T}_r \in \mathbb{R}^{N \times 1}$ causes the fundamental RMS currents of all arms to change. As there is only negligible inertial effects in parallel arms, the RMS currents are updated as given by Eq. (27):

$$\vec{I}_a(k+1) = \mathbf{H} \vec{T}_r(k), \quad (27)$$

where matrix $\mathbf{H} \in \mathbb{R}^{N \times N}$. The updated fundamental RMS current vector needs to go through the dynamics of the moving average RMS calculations, which is based on a window

$$\mathbf{B}_b = T_s^{syn} \begin{bmatrix} N-1 & -1 & \cdots & -1 \\ -1 & N-1 & \cdots & -1 \\ \vdots & \vdots & \ddots & \vdots \\ -1 & -1 & \cdots & N-1 \end{bmatrix}, \quad \mathbf{C}_b = \begin{bmatrix} 1 & -\frac{1}{N-1} & \cdots & -\frac{1}{N-1} \\ -\frac{1}{N-1} & 1 & \cdots & -\frac{1}{N-1} \\ \vdots & \vdots & \ddots & \vdots \\ -\frac{1}{N-1} & -\frac{1}{N-1} & \cdots & 1 \end{bmatrix}, \quad \mathbf{A}'_{ma} = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \\ 1 & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & 1 & 0 \end{bmatrix}, \quad \mathbf{B}'_{ma} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix},$$

$$\mathbf{C}'_{ma} = \frac{T_s^{syn}}{T_w^{ma}} [1 \ 0 \ \cdots \ 0 \ -1],$$

$$\mathbf{D}'_{ma} = \frac{T_s^{syn}}{T_w^{ma}},$$

$$\mathbf{A}_f = \begin{bmatrix} e^{-\omega_c T_s^{syn}} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & e^{-\omega_c T_s^{syn}} \end{bmatrix}, \quad \mathbf{H} = \frac{I_t}{T_c} \begin{bmatrix} 0 & \frac{1}{R_{a1}} & \frac{1}{\sum\limits_{j=1, j \neq 1}^N \frac{1}{R_{aj}}} & \cdots & \cdots & \frac{1}{R_{a1}} & \frac{1}{\sum\limits_{j=1, j \neq N}^N \frac{1}{R_{aj}}} \\ \frac{1}{R_{a2}} & \frac{1}{\sum\limits_{j=1, j \neq 2}^N \frac{1}{R_{aj}}} & 0 & \frac{1}{R_{a2}} & \frac{1}{\sum\limits_{j=1, j \neq 3}^N \frac{1}{R_{aj}}} & \cdots & \frac{1}{R_{a2}} & \frac{1}{\sum\limits_{j=1, j \neq N}^N \frac{1}{R_{aj}}} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ \frac{1}{R_{aN}} & \frac{1}{\sum\limits_{j=1, j \neq 1}^N \frac{1}{R_{aj}}} & \frac{1}{R_{aN}} & \frac{1}{\sum\limits_{j=1, j \neq 2}^N \frac{1}{R_{aj}}} & \cdots & \cdots & \cdots & 0 \end{bmatrix},$$

$$\mathbf{B}_f = \mathbf{I}_N - \mathbf{A}_f, \quad \mathbf{C}_f = \mathbf{I}_N,$$

$$\mathbf{A}_t = \begin{bmatrix} \mathbf{I}_N & \mathbf{0}_{N \times MN} & T_s^{syn} B_b C_f \\ k_i^{syn} B_{ma} H C_b & A_{ma} & k_p^{syn} B_{ma} H C_b B_b C_f \\ k_i^{syn} B_f D_{ma} H C_b & B_f C_{ma} & A_f + k_p^{syn} B_f D_{ma} H C_b B_b C_f \end{bmatrix}, \quad \mathbf{B}_t = \begin{bmatrix} \mathbf{0}_{N \times N} \\ B_{ma} H \\ D_{ma} H \end{bmatrix},$$

length of T_w^{ma} and a buffer vector $\vec{x}_{ma} \in \mathbb{R}^{MN \times 1}$. This mathematical process is given by Eqs. (28)-(31):

$$\vec{x}_{ma}(k+1) = \mathbf{A}_{ma} \vec{x}_{ma}(k) + \mathbf{B}_{ma} \vec{I}_a(k), \quad (28)$$

$$\vec{I}_a^{ma}(k) = \mathbf{C}_{ma} \vec{x}_{ma}(k) + \mathbf{D}_{ma} \vec{I}_a(k), \quad (29)$$

$$\mathbf{A}, \mathbf{B}, \mathbf{C}, \mathbf{D}_{ma} = \mathbf{I}_N \otimes \mathbf{A}', \mathbf{B}', \mathbf{C}', \mathbf{D}'_{ma}, \quad (30)$$

$$M = \frac{T_w^{ma}}{T_s^{syn}}, \quad (31)$$

where matrices $\mathbf{A}'_{ma} \in \mathbb{R}^{M \times M}$, $\mathbf{B}'_{ma} \in \mathbb{R}^{M \times 1}$, $\mathbf{C}'_{ma} \in \mathbb{R}^{1 \times M}$, and $\mathbf{D}'_{ma} \in \mathbb{R}^{1 \times 1}$. As mentioned earlier, \vec{I}_a^{ma} needs to be filtered by a low-pass filter to obtain \vec{I}_a^f , which is described in Eqs. (32) and (33):

$$\vec{x}_f(k+1) = \mathbf{A}_f \vec{x}_f(k) + \mathbf{B}_f \vec{I}_a^{ma}(k), \quad (32)$$

$$\vec{I}_a^f(k) = \mathbf{C}_f \vec{x}_f(k), \quad (33)$$

where $\vec{x}_f \in \mathbb{R}^{N \times 1}$ is the state vector related to the low-pass filter, matrices $\mathbf{A}, \mathbf{B}, \mathbf{C}_f \in \mathbb{R}^{N \times N}$. Finally, combining Eqs. (25)-(33), the total closed-loop dynamic model of the balancing control loop is given by Eq. (34):

$$\begin{bmatrix} \vec{x}_b(k+1) \\ \vec{x}_{ma}(k+1) \\ \vec{x}_f(k+1) \end{bmatrix} = \mathbf{A}_t \begin{bmatrix} \vec{x}_b(k) \\ \vec{x}_{ma}(k) \\ \vec{x}_f(k) \end{bmatrix} + \mathbf{B}_t \vec{T}_r^*, \quad (34)$$

where $\mathbf{A}_t \in \mathbb{R}^{(MN+2N) \times (MN+2N)}$ and $\mathbf{B}_t \in \mathbb{R}^{(MN+2N) \times N}$.

Before selecting $k_{p,i}^{syn}$, the stability margin of these gains should be determined. The stability condition can be verified by eigenvalue analysis of the state matrix A_t for the rated I_t , because A_t changes with I_t . The maximum permissible gain margin is determined by constraining all eigenvalues to remain within the unit circle. Once the stability margin is determined, $k_{p,i}^{syn}$ can be selected within this stable region through numerical simulations of the dynamic model.

Besides the PI gains, ΔT_r^{max} is also a critical parameter. This saturation is designed to ensure that the rest period does not become negative. Since PWM signals cannot have a negative duty cycle, the executed rest period is capped at zero. However, compensation adjustments for other arms are still computed based on the unsaturated negative value, thereby disrupting the intended rotational rest sequence. This disruption can lead to an overflow of the rotation cycle and potential overlaps between rest periods, resulting in current surges during the overlapping intervals. To mitigate these effects, the saturation limit should generally be scaled inversely with the error band of the on-resistances across all arms.

III. SIMULATION RESULTS

In this Section, Matlab/Simulink is used as the simulation platform. The default simulation parameters are shown in the Appendix A. As the proposed method works similarly for all phases, only the result of one phase is shown. All balancing controllers are based on true RMS currents of parallel arms.

As shown in Fig. 11(a), the traditional synchronized switching method results in a true RMS current imbalance that causes arm 4 to conduct 38% more current than arm 1, which can significantly shorten the expected equipment lifespan due to the thermal stress inequality. In contrast, Fig. 11(b) shows that

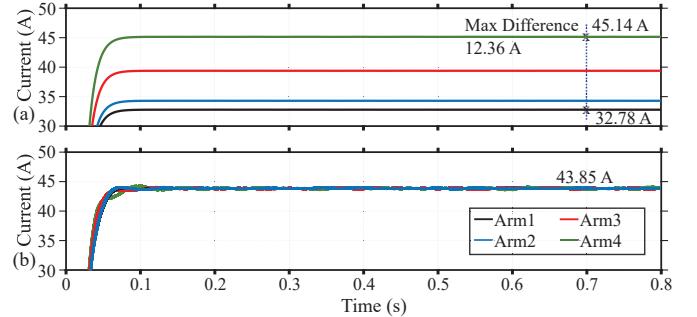


Fig. 11. True RMS current balancing comparison for a random 4 arms parallel configuration: (a) with the traditional method; (b) with the proposed method.

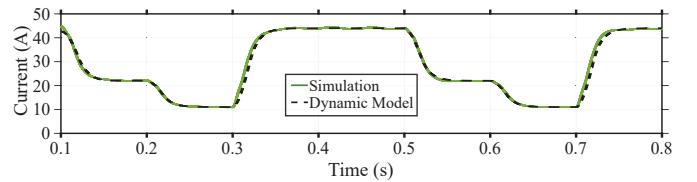


Fig. 12. Simulation results and dynamic model output of an individual arm's true RMS current under power step changes.

the proposed method achieves an almost uniform true RMS current distribution under the same operating conditions. With the proposed method, the total true RMS current increases roughly 15%, which confirms our analysis for a 4-arm scenario in Section II-A. The minor periodic oscillations observed in Fig. 11(b) result from the moving average process, and their amplitude typically reduces with T_s^{syn} . The dynamic model derived in Section II-C runs concurrently with the simulation model, and Fig. 12 presents a comparative analysis of the true RMS current results for an individual arm. The high-level fit between the two sets of results confirms the accuracy of the derived dynamic model.

To evaluate the proposed method under various numbers of parallel arms and different on-resistance error bands, a series of tests with uniformly distributed on-resistances were performed, with the results summarized in Table II. The findings indicate that as the number of parallel arms increases, the allowed on-resistance error band for achieving near complete current balancing becomes more constrained. When the on-resistance error band exceeds this allowed limit, the rest period regulation signal saturates to prevent negative rest periods, leading to accuracy deviations in balancing results. Furthermore, the data in Table II show that the additional conduction loss power decreases as the number of parallel arms increases, which is similar to the reduction in hardware costs associated with the proposed method. Although these results highlight the benefits of using more arms, the final parallel configuration must be carefully designed based on the on-resistance mismatch level of the procured MOSFETs and the allowed true RMS current mismatch thresholds.

Table II also compares the necessary derating factors of the synchronized switching method and the proposed method under identical inverter rating, maximum allowed junction temperature, and arm current sensing conditions. The results show that the derated synchronized switching method of

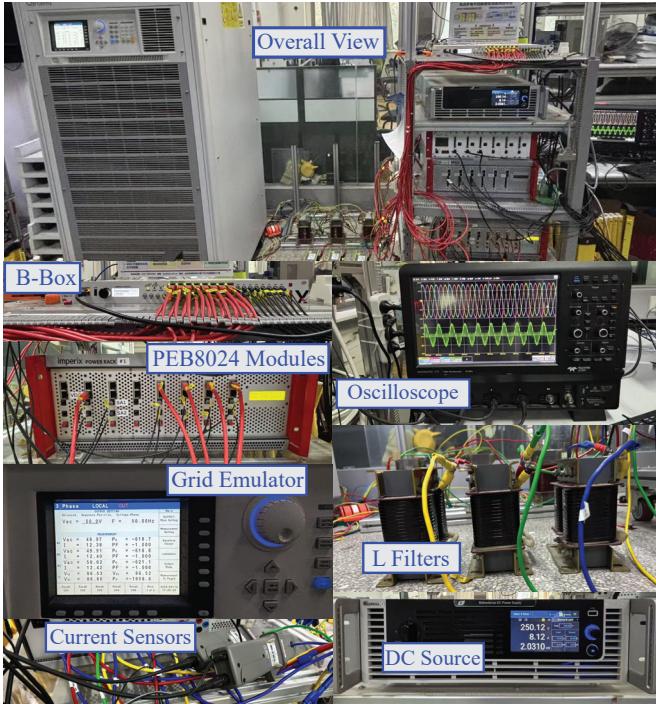


Fig. 13. The low-power experimental setup for the proposed method.

fers higher available power when on-resistance mismatches are mild. However, imbalanced junction temperatures and asynchronous aging under derated synchronized switching can gradually amplify resistance mismatch, further increasing thermal disparity and reducing available power over time. This issue is especially critical in applications with frequent power cycling, such as electric vehicles and frequency-support battery energy storage systems. Comparatively, the proposed method may start with slightly lower available power, but it maintains consistent performance as the asynchronous aging effect is significantly alleviated.

IV. EXPERIMENTAL RESULTS

The low-power experimental setup (2 kVA) for the two-level parallel arm inverter system (Fig. 1) is shown in Fig. 13, where phase A is configured with 4 parallel arms, while phases B and C each use a single arm. Arm currents are measured through a set of Hall current sensors, and their real-time RMS values

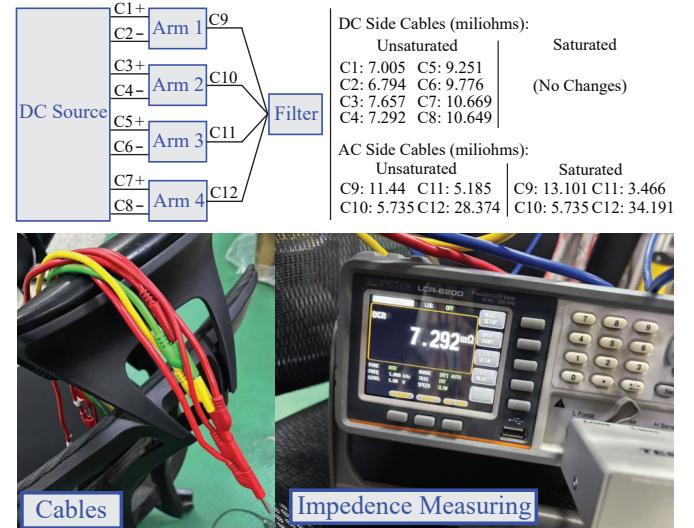


Fig. 14. Cable arrangement in the experiments for creating resistance mismatch between parallel PEB8024 modules.

are calculated in the B-Box control unit through the moving average algorithm. Due to hardware constraints, new control parameters are required, as specified in the Appendix B. Since the SiC MOSFETs in the PEB8024 arm modules have already been screened and picked by Imperix, we introduced on-resistance mismatches between these arm modules by power cables of different resistances. In total, three experiments were conducted: (1) a comparison of the traditional synchronized switching and proposed balancing methods without control saturation; (2) a comparison under control saturation; and (3) an instability injection test in the balancing control loop. The parameters of all the cables used in both saturated and unsaturated experiments are listed in Fig. 14, and the instability experiment uses the same cables as in the unsaturated case. Note that the cable configurations for the unsaturated and saturated experiments are different, and the saturated scenario has a larger parameter mismatch on the AC side.

For the unsaturated scenario, the steady-state behaviors of inverter currents with the traditional and proposed methods are illustrated in Figs. 15 and 16. A comparison between Fig. 15(a) and Fig. 16(a) demonstrates that the experimental results align well with the expected true RMS current balancing

TABLE II
TRUE RMS CURRENT BALANCING RESULTS OF PARALLEL ARMS WITH EVENLY SPACED MISMATCHES (100 kW, $T_s^{syn}=50 \mu s$)

N	R_a band (mΩ)	$I_{a1\dots N}$ Trad. (A)	$I_{a1\dots N}$ Prop. (A)	Saturation	Trad. Derating (%)	Prop. Derating (%)
4	55 ± 7.5 (13.63%)	33.00-43.44	43.85	No(Edge)	14.7 ↑↑, t ↑	15.8
4	45 ± 6.5 (14.44%)	32.74-43.80	43.85	No(Edge)	15.7 ↑↑, t ↑	15.8
4	35 ± 5.0 (14.28%)	32.80-43.71	43.85 (+15.8%)	No(Edge)	15.5 ↑↑, t ↑	15.8
4	35 ± 6.0 (17.14%)	31.83-44.99	43.15-44.56	Yes	18.9 ↑↑, t ↑	17.7 ↑, t ↑
4	35 ± 7.0 (20.00%)	30.88-46.30	42.25-45.69	Yes	22.3 ↑↑, t ↑	20.7 ↑, t ↑
4	35 ± 8.0 (22.86%)	29.95-47.66	41.29-46.81	Yes	25.9 ↑↑, t ↑	23.6 ↑, t ↑
6	35 ± 3.0 (8.57%)	23.20-27.55	27.65 (+9.5%)	No(Edge)	9.1 ↑, t ↑	9.5
8	35 ± 2.4 (6.86%)	17.70-20.31	20.25 (+6.9%)	No(Edge)	7.3 ↑, t ↑	6.9
10	35 ± 1.8 (5.14%)	14.41-15.97	15.98 (+5.5%)	No(Edge)	5.4 ↑, t ↑	5.5

Note: "↑" represent a growing trend over time, and "↑↑" means comparatively faster;

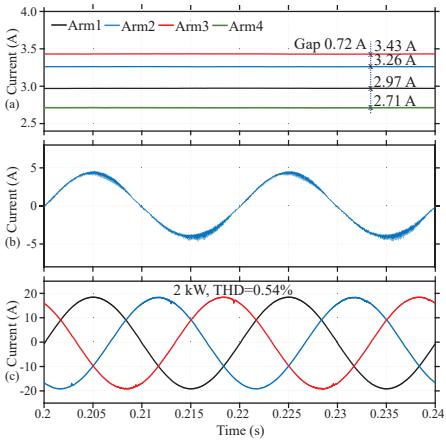


Fig. 15. Steady-state experimental results with the synchronized switching method for the unsaturated scenario: (a) true RMS currents of parallel arms; (b) current waveform of arm 1; (c) PCC current.

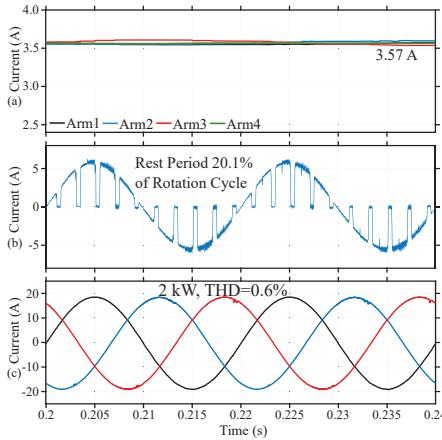


Fig. 16. Steady-state experimental results with the proposed method for the unsaturated scenario: (a) true RMS currents of parallel arms; (b) current waveform of arm 1; (c) PCC current.

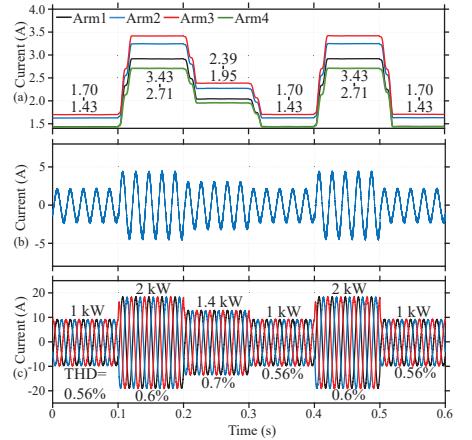


Fig. 17. Dynamic experimental results with the synchronized switching method for the unsaturated scenario: (a) true RMS currents of parallel arms; (b) current waveform of arm 1; (c) PCC current.

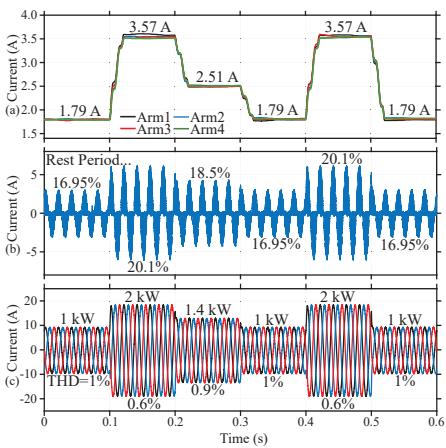


Fig. 18. Dynamic experimental results with the proposed method for the unsaturated scenario: (a) true RMS currents of parallel arms; (b) current waveform of arm 1; (c) PCC current.

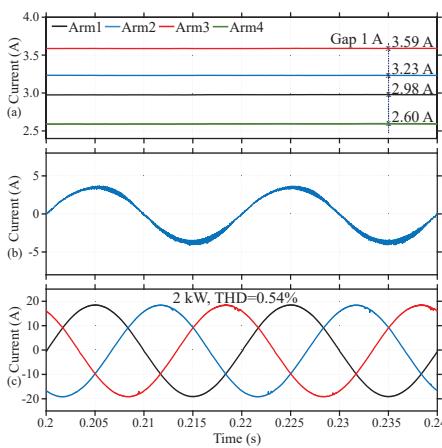


Fig. 19. Steady-state experimental results with the synchronized switching method for the saturated scenario: (a) true RMS currents of parallel arms; (b) current waveform of arm 4; (c) PCC current.

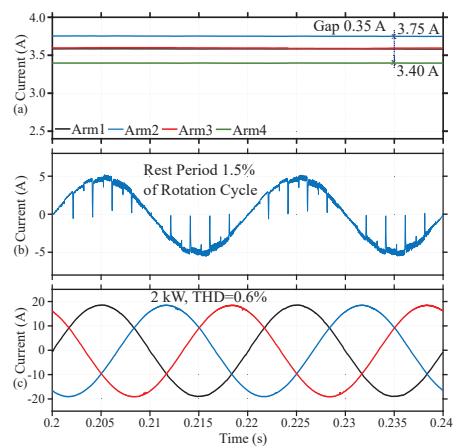


Fig. 20. Steady-state experimental results with the proposed method for the saturated scenario: (a) true RMS currents of parallel arms; (b) current waveform of arm 4; (c) PCC current.

performance. Furthermore, the total true RMS current across all arms reveals a 15% increment under the rotational rest control, which is consistent with our theoretical expectations. Fig. 15(b) and Fig. 16(b) present the current profiles of arm 1, where the interrupted sinusoidal waveform clearly indicates the respective rest periods. Data in Fig. 16(b) also confirms that the implemented deadtime effectively mitigated current surges during rest period transitions. In addition, Fig. 15(c) and Fig. 16(c) show that the proposed method generally preserves the PCC current profile while achieving current balancing of parallel arms. Regarding dynamic performance, Fig. 17 and Fig. 18 illustrate the inverter response with the traditional and proposed methods under active power step changes. The results in Fig. 17(a) and Fig. 18(a) indicate that the proposed method maintains high accuracy and speed (tens of ms) in balancing under rapid power variations, while Fig. 17(b,c) and Fig. 18(b,c) prove that the proposed method maintains the arm and PCC current profiles for different operating conditions.

For the saturated scenario, Fig. 19 and Fig. 20 compare the steady-state performance of the traditional and proposed

methods, while Fig. 21 and Fig. 22 compare their dynamic performance. Although control saturation reduces the accuracy of the proposed method in true RMS current balancing, as evidenced in Fig. 20(a) and Fig. 22(a), the proposed method still achieves an improvement of over 60% in the accuracy of balancing compared to the traditional method at full power. However, as shown in Fig. 20(b) and Fig. 22(b), the rest periods for arm 4 (smallest rest period) are saturated to prevent the situation of zero rest period, and thus reducing balancing performance. In practical implementations, the saturation limit can be adjusted according to specific design priorities, such as high accuracy at the rated power or consistent accuracy throughout the entire power operating range. Regarding the PCC current profile, the data presented in Fig. 20(c) and Fig. 22(c) indicate that control saturation does not affect the PCC current performance of the proposed method under steady-state or dynamic conditions.

Furthermore, Fig. 23 illustrates the impact of instability in the balancing control loop on the PCC current. As depicted in Fig. 23(a) and (b), a manual change of k_p^{syn} at approximately

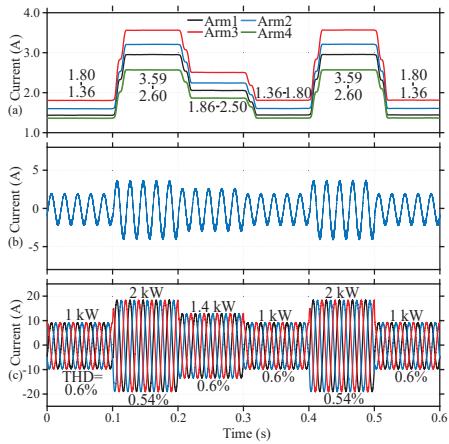


Fig. 21. Dynamic experimental results with the synchronized switching for the saturated scenario: (a) true RMS currents of parallel arms; (b) current waveform of arm 4; (c) PCC current.

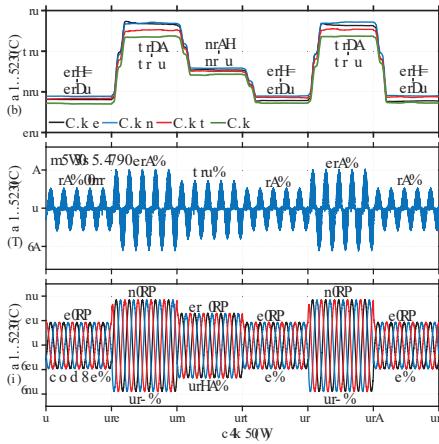


Fig. 22. Dynamic experimental results with the proposed method for the saturated scenario: (a) true RMS currents of parallel arms; (b) current waveform of arm 4; (c) PCC current.

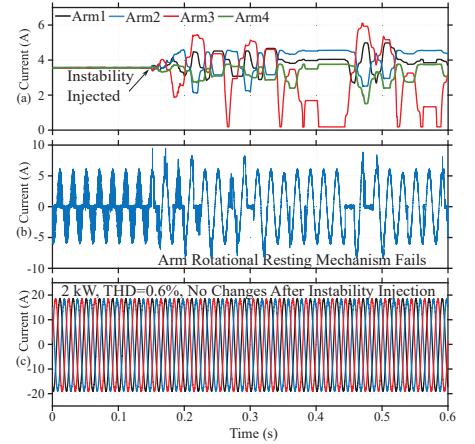


Fig. 23. The impact of the proposed method's instability on the inverter currents: (a) true RMS currents of parallel arms; (b) current waveform of arm 1; (c) the PCC current.

0.15 seconds triggers unstable oscillations in the arm currents, resulting in a failure of the balancing control. However, this instability only affects the current distribution among the parallel arms; the merged current at the PCC remains unaffected during and after the disturbance, as shown in Fig. 23(c). This confirms that the balancing control does not compromise the stability of the inverter's primary control loop. Recall that the previous experimental results also demonstrated a negligible impact of the proposed method on the PCC current THD. By combining both THD and stability results, it is evident that the proposed balancing control loop is effectively decoupled from the inverter's primary control loop.

V. CONCLUSION

Parallel arm SiC-based converters are susceptible to on-resistance inconsistencies, causing imbalanced RMS currents and eventually asynchronous aging of SiC MOSFETs. Existing balancing methods either incur significant costs or adversely affect the reliability of the converter primary control system. This paper proposes a rotational rest control strategy to achieve RMS current balancing in parallel arms. The proposed method does not require customized gate drivers, and the associated hardware cost percentage is inversely scaled with the number of parallel arms. In addition, the proposed balancing control loop is decoupled from the converter's primary control loop, ensuring stable and reliable voltage or current control at the PCC even if the balancing loop suddenly becomes unstable. Future work should focus on reducing the induced conduction losses and improving the parameter error tolerance for large arm numbers.

REFERENCES

- [1] S. Zhao, A. Kempitiya, W. T. Chou, V. Palija, and C. Bonfiglio, "Variable DC-Link Voltage LLC Resonant DC/DC Converter With Wide Bandgap Power Devices," *IEEE Transactions on Industry Applications*, vol. 58, no. 3, pp. 2965–2977, 5 2022.
- [2] K. Hamada, M. Nagao, M. Ajioka, and F. Kawai, "SiC—Emerging Power Device Technology for Next-Generation Electrically Powered Environmentally Friendly Vehicles," *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 278–285, 2 2015.
- [3] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2872–2882, 7 2011.
- [4] R. Heckman and C. Quinn, "The Growth of Wide Bandgap Technology in Industrial Power Conversion," *IEEE Power Electronics Magazine*, vol. 11, no. 4, pp. 54–60, 12 2024.
- [5] T. Bertelshofer, A. März, and M. Bakran, "Modelling parallel SiC MOSFETs: thermal self-stabilisation vs. switching imbalances," *IET Power Electronics*, vol. 12, no. 5, pp. 1071–1078, 5 2019.
- [6] H. Li, S. Zhao, X. Wang, L. Ding, and H. A. Mantooth, "Parallel Connection of Silicon Carbide MOSFETs—Challenges, Mechanism, and Solutions," *IEEE Transactions on Power Electronics*, vol. 38, no. 8, pp. 9731–9749, 8 2023.
- [7] C. Zhao, L. Wang, X. Yang, F. Zhang, and Y. Gan, "Comparative Investigation on Paralleling Suitability for SiC MOSFETs and SiC/Si Cascode Devices," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 4, pp. 3503–3514, 4 2022.
- [8] C. Zhao, L. Wang, F. Zhang, and F. Yang, "A Method to Balance Dynamic Current of Parallelized SiC MOSFETs With Kelvin Connection Based on Response Surface Model and Nonlinear Optimization," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 2068–2079, 2 2021.
- [9] K. Mainali, R. Wang, J. Sabate, and S. Klopman, "Current Sharing and Overvoltage Issues of Parallelized SiC MOSFET Modules," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 9 2019, pp. 2413–2418.
- [10] G. Wang, J. Mookken, J. Rice, and M. Schupbach, "Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*. IEEE, 3 2014, pp. 1478–1483.
- [11] X. Chen, W. Chen, X. Yang, Y. Ren, and L. Qiao, "Common-Mode EMI Mathematical Modeling Based on Inductive Coupling Theory in a Power Module With Parallel-Connected SiC MOSFETs," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6644–6661, 6 2021.
- [12] C.-W. Chang, M. Spieler, A. M. EL-Refaie, R. A. Torres, R. Burgos, and D. Dong, "A current-balancing gate driver for dynamic current sharing of paralleled sic mosfets with kelvin-source connection," *IEEE Transactions on Power Electronics*, vol. 40, no. 1, pp. 1215–1233, 2025.
- [13] J. Hu, O. Alatise, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. A. Mawby, "The Effect of Electrothermal Nonuniformities on Parallel Connected SiC Power Devices Under Unclamped and Clamped Inductive Switching," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4526–4535, 6 2016.
- [14] B. Zhao, Q. Yu, P. Sun, Y. Cai, and Z. Zhao, "Device Screening Strategy for Suppressing Current Imbalance in Parallel-Connected SiC MOSFETs," *IEEE Transactions on Device and Materials Reliability*, vol. 21, no. 4, pp. 556–568, 12 2021.
- [15] Y. Mao, Z. Miao, C.-M. Wang, and K. D. T. Ngo, "Balancing of Peak Currents Between Paralleled SiC MOSFETs by Drive-Source Resistors

- and Coupled Power-Source Inductors," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8334–8343, 10 2017.
- [16] Z. Miao, Y. Mao, G.-Q. Lu, and K. D. T. Ngo, "Magnetic Integration Into a Silicon Carbide Power Module for Current Balancing," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 11 026–11 035, 11 2019.
- [17] N. Lin, Y. Zhao, and H. A. Mantooth, "An Effective Current Balancing Method for Inverters With Paralleled Silicon Carbide Power Modules," *IEEE Transactions on Industry Applications*, vol. 59, no. 6, pp. 6986–7000, 11 2023.
- [18] K. Matsubara and K. Wada, "Current Balancing for Parallel Connection of Silicon Carbide MOSFETs Using Bus Bar Integrated Magnetic Material," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 3 2019, pp. 2688–2693.
- [19] J. Fabre and P. Ladoux, "Parallel Connection of 1200 V/100 A SiC MOSFET Half-bridge Modules," *IEEE Transactions on Industry Applications*, pp. 1–1, 2015.
- [20] Y. Wen, Y. Yang, and Y. Gao, "Active Gate Driver for Improving Current Sharing Performance of Paralleled High-Power SiC MOSFET Modules," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1491–1505, 2 2021.
- [21] X. Du, Y. Wei, A. Stratta, L. Du, V. S. Machireddy, and A. Mantooth, "A Four-level Active Gate Driver with Continuously Adjustable Intermediate Gate Voltages," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 3 2022, pp. 1379–1386.
- [22] N. Lin, A. J. R. A. Hmoud, and Y. Zhao, "An Active Gate Driver Control Scheme for Steady-State Current Balancing of Paralleled SiC MOSFETs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, no. 9, pp. 4341–4345, 9 2024.
- [23] L. Du, X. Du, S. Zhao, Y. Wei, Z. Yang, L. Ding, and H. A. Mantooth, "Digital Close-Loop Active Gate Driver for Static and Dynamic Current Sharing of Paralleled SiC MOSFETs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 2, pp. 1372–1384, 4 2024.
- [24] K. Siri, C. Lee, and T.-E. Wu, "Current distribution control for parallel connected converters. I," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 28, no. 3, pp. 829–840, 7 1992.
- [25] D. Liu, A. Hu, G. Wang, and W. Hu, "Current Sharing Schemes for Multiphase Interleaved DC/DC Converter with FPGA Implementation," in *2010 International Conference on Electrical and Control Engineering*. IEEE, 6 2010, pp. 3512–3515.
- [26] J. Burkard, M. Pfister, and J. Biela, "Control Concept for Parallel Interleaved Three-Phase Converters with Decoupled Balancing Control," *2018 20th European Conference on Power Electronics and Applications, EPE 2018 ECCE Europe*, pp. P.1–P.9, 2018.
- [27] A. Viatkin, M. Ricco, R. Mandrioli, T. Kerekes, R. Teodorescu, and G. Grandi, "Sensorless Current Balancing Control for Interleaved Half-Bridge Submodules in Modular Multilevel Converters," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 1, pp. 5–16, 1 2023.
- [28] V. Nasirian, S. Moayedi, A. Davoudi, and F. L. Lewis, "Distributed Cooperative Control of DC Microgrids," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2288–2303, 4 2015.
- [29] A. Bidram, A. Davoudi, F. L. Lewis, and J. M. Guerrero, "Distributed Cooperative Secondary Control of Microgrids Using Feedback Linearization," *IEEE Transactions on Power Systems*, vol. 28, no. 3, pp. 3462–3470, 8 2013.
- [30] Y. Liu, D. Jin, S. Jiang, W. Liang, J. Peng, and C.-M. Lai, "An active damping control method for the llcl filter-based sic mosfet grid-connected inverter in vehicle-to-grid application," *IEEE Transactions on Vehicular Technology*, vol. 68, no. 4, pp. 3411–3423, 2019.
- [31] Y. Liu, K.-Y. See, S. Yin, R. Simanjorang, C. F. Tong, A. Nawawi, and J.-S. J. Lai, "Lcl filter design of a 50-kw 60-khz sic inverter with size and thermal considerations for aerospace applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8321–8333, 2017.
- [32] E. Gurpinar, D. De, A. Castellazzi, D. Barater, G. Buticchi, and G. Francheschini, "Performance analysis of sic mosfet based 3-level anpc grid-connected inverter with novel modulation scheme," in *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2014, pp. 1–7.
- [33] W. Choi, D. Han, C. T. Morris, and B. Sarlioglu, "Achieving high efficiency using sic mosfets and reduced output filter for grid-connected v2g inverter," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, 2015, pp. 003 052–003 057.
- [34] M. Chen, H. Wang, D. Pan, X. Wang, and F. Blaabjerg, "Thermal characterization of silicon carbide mosfet module suitable for high-temperature computationally efficient thermal-profile prediction," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 3947–3958, 2021.
- [35] H. Cui, "Accelerated temperature cycle test and coffin-manson model for electronic packaging," in *Annual Reliability and Maintainability Symposium, 2005. Proceedings.*, 2005, pp. 556–560.

APPENDIX A SIMULATION PARAMETERS

Parameter	Description	Value	Unit
R_{a1}	On-Resistance of Arm 1	39.2	mΩ
R_{a2}	On-Resistance of Arm 2	37.4	mΩ
R_{a3}	On-Resistance of Arm 3	32.5	mΩ
R_{a4}	On-Resistance of Arm 4	28.3	mΩ
f_{sw}	Switching Frequency	80.0	kHz
V_g	Grid Voltage	220.0	V
T_s	Control Time Step (PQ Tracking)	0.1	μs
P^*	Active Power References	100.0	kW
T_c	Rotation Cycle	2.0	ms
k_p^{syn}	Gains of Consensus Controllers	1×10^{-5}	N/A
k_i^{syn}	Gains of Consensus Controllers	1×10^{-3}	N/A
ω_c	Cut-off Frequency (RMS)	100.0	rad s ⁻¹
T_w^{ma}	Moving Average Window	20.0	ms
T_s^{syn}	Control Time Step (Balancing)	50.0	μs
T_d^{trtr}	Rest-Transition Deadtime	20.0	μs

APPENDIX B EXPERIMENTAL PARAMETERS

Parameter	Description	Value	Unit
f_{sw}	Switching Frequency	20.0	kHz
V_g	Grid Voltage	50.0	V
V_{dc}	DC Source Voltage	250.0	V
T_s	Control Time Step (PQ Tracking)	25.0	μs
P^*	Active Power References	2.0	kW
T_c	Rotation Cycle	2.0	ms
k_p^{syn}	Gains of Consensus Controllers	1×10^{-3}	N/A
k_i^{syn}	Gains of Consensus Controllers	1.5×10^{-3}	N/A
ω_c	Cut-off Frequency (RMS)	100.0	rad s ⁻¹
T_w^{ma}	Moving Average Window	20.0	ms
T_s^{syn}	Control Time Step (Balancing)	50.0	μs
T_d^{trtr}	Rest-Transition Deadtime	20.0	μs