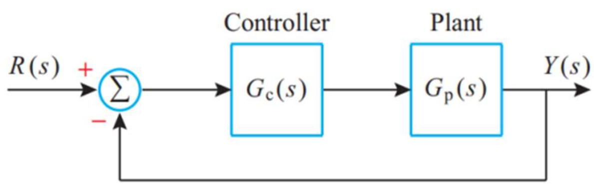
EE49001: Control and Electronic System Design

Assignment-3: Lead-Lag Compensator Design

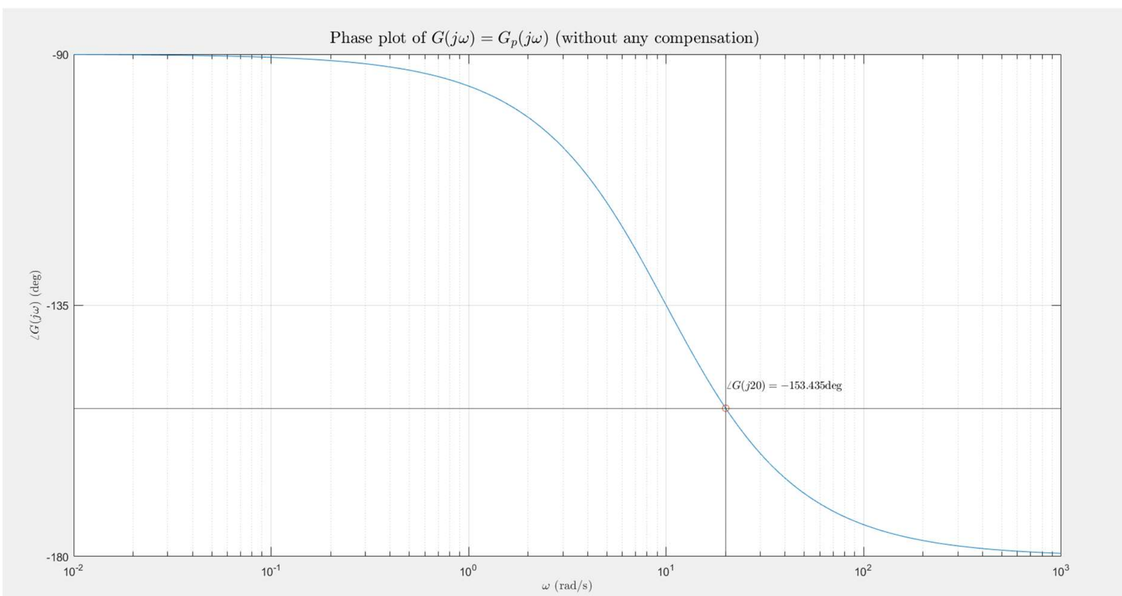
Submitted By:

21EE30004: Anirvan Krishna | 21EE30001: Aditya Kumar



In the above block diagram,

$$G_p = \frac{10}{s(s+10)}$$



Design of Lead Compensator

For a lead compensator the controller is assumed to be of form

$$G_{c1} = \frac{K(Ts+1)}{\beta Ts + 1}$$

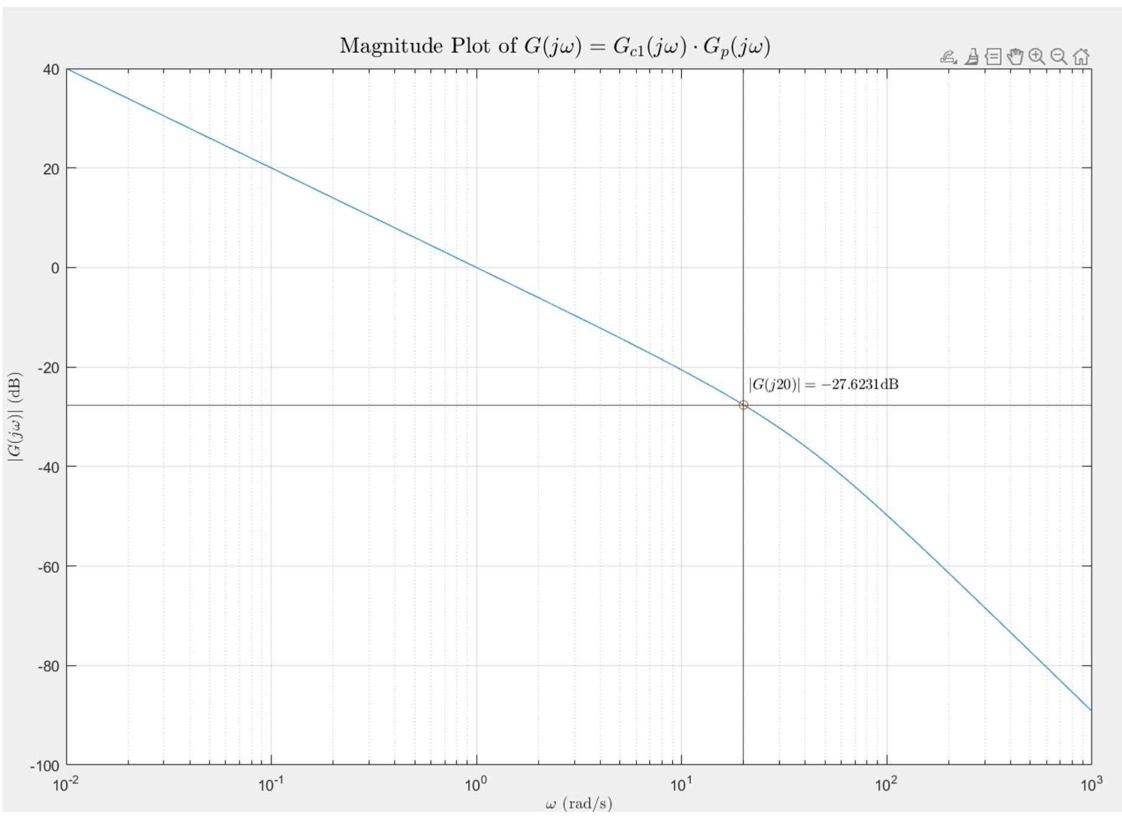
Where, $K > 0, T > 0$ and $0 < \beta < 1$

$$\omega_c = 0.995 \text{ rad/s}$$

From the above plot it can be observed that, uncompensated phase margin is $PM_u = \angle G(j20) + 180° = 26.565°$

Therefore, the controller parameters are

$\phi_m = PM - PM_u$ $= 33.435°$	$\beta = \frac{1 - \sin\phi_m}{1 + \sin\phi_m}$ ≈ 0.2895	$T = \frac{1}{\omega_c\sqrt{\beta}}$ ≈ 0.093



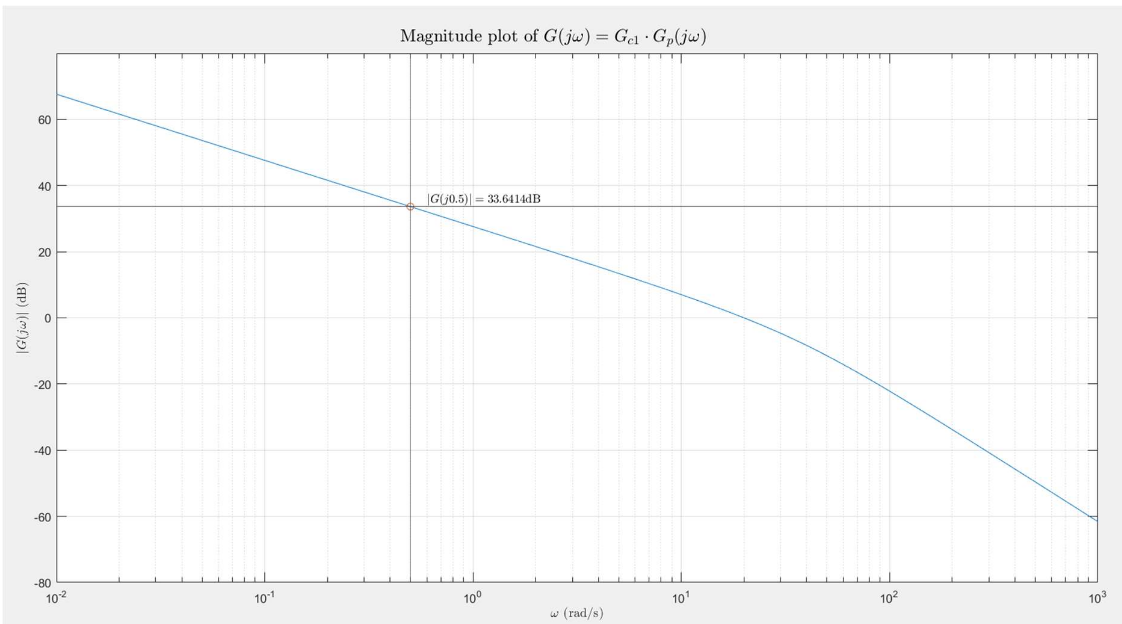
From the graph it can be observed that $20\log\left|G_{c1} \cdot G_p(j20)\right| = -27.6231$dB. Hence to make $\left|G_{c1} \cdot G_p(j20)\right| = 1$, the magnitude plot needs to be brought up by 27.6231dB. Therefore, our required DC gain is

$$\boxed{K = 10^{\frac{27.6231}{20}} \approx 24.0522}$$

Design of Lag Compensator

For a lag compensator the controlled is assumed to be of form

$$G_{c2} = \frac{\alpha(T_1 s + 1)}{\alpha T_1 s + 1}$$



Where, $T_1 > 0, \alpha > 1$

Here,

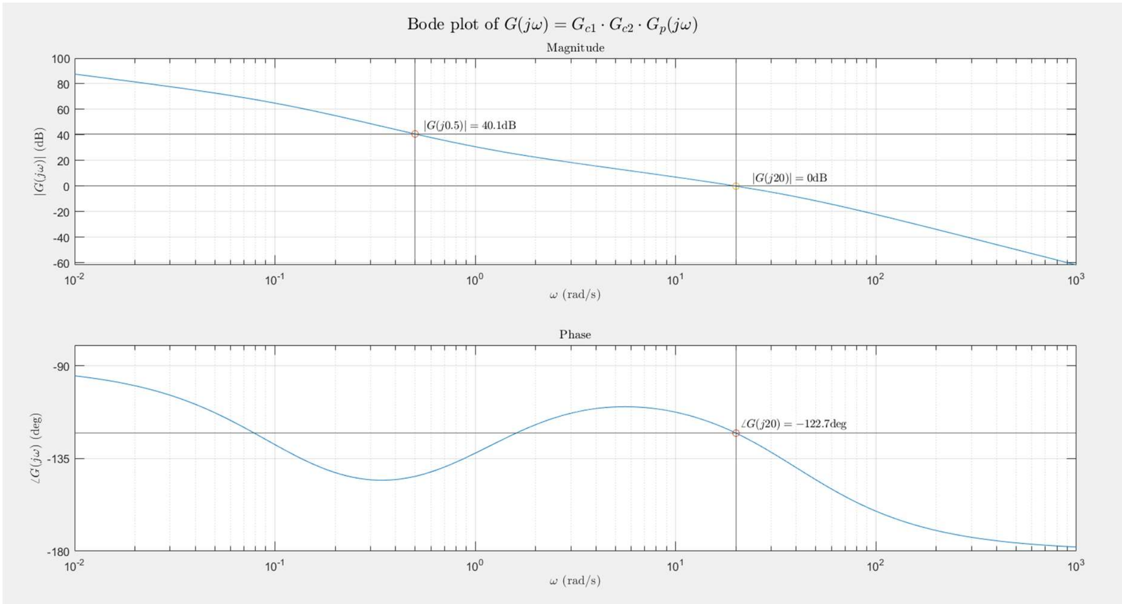
$$\boxed{T_1 = \frac{7}{\omega_c} \approx 0.35}$$

And from the above plot is observed that $20 \log\left|G_{c1} \cdot G_p(j0.5)\right| = 33.6414$. Therefore,

Thus, the controller parameters are

$F = \dfrac{100}{\left|G_{c1} \cdot G_p(j0.5)\right|} \approx 2.08$	$\alpha \geq F = 10$

Verification



The compensated system is $G(s) = G_{c1} \cdot G_{c2} \cdot G_p(s)$ and from the above plot it can observed that the gain crossover frequency is 20rad/s and the corresponding phase margin is $\angle G(j20) + 180 = 57.3$deg. Also loop gain at $\omega \in [0,0.5] \geq 100$ (40dB) as $|G(j\omega)|$ is decreasing in the lower frequencies and $20 \log |G(j0.5)| = 40.1$dB.

Thus, the desired specifications are met.