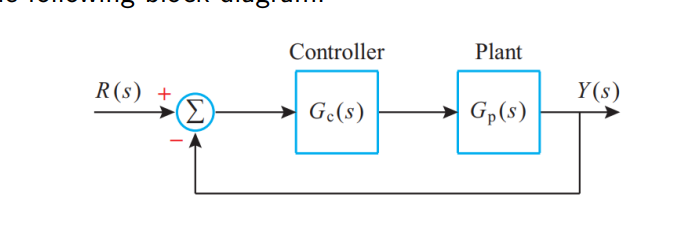
**EE49001: Control and Electronic System Design**

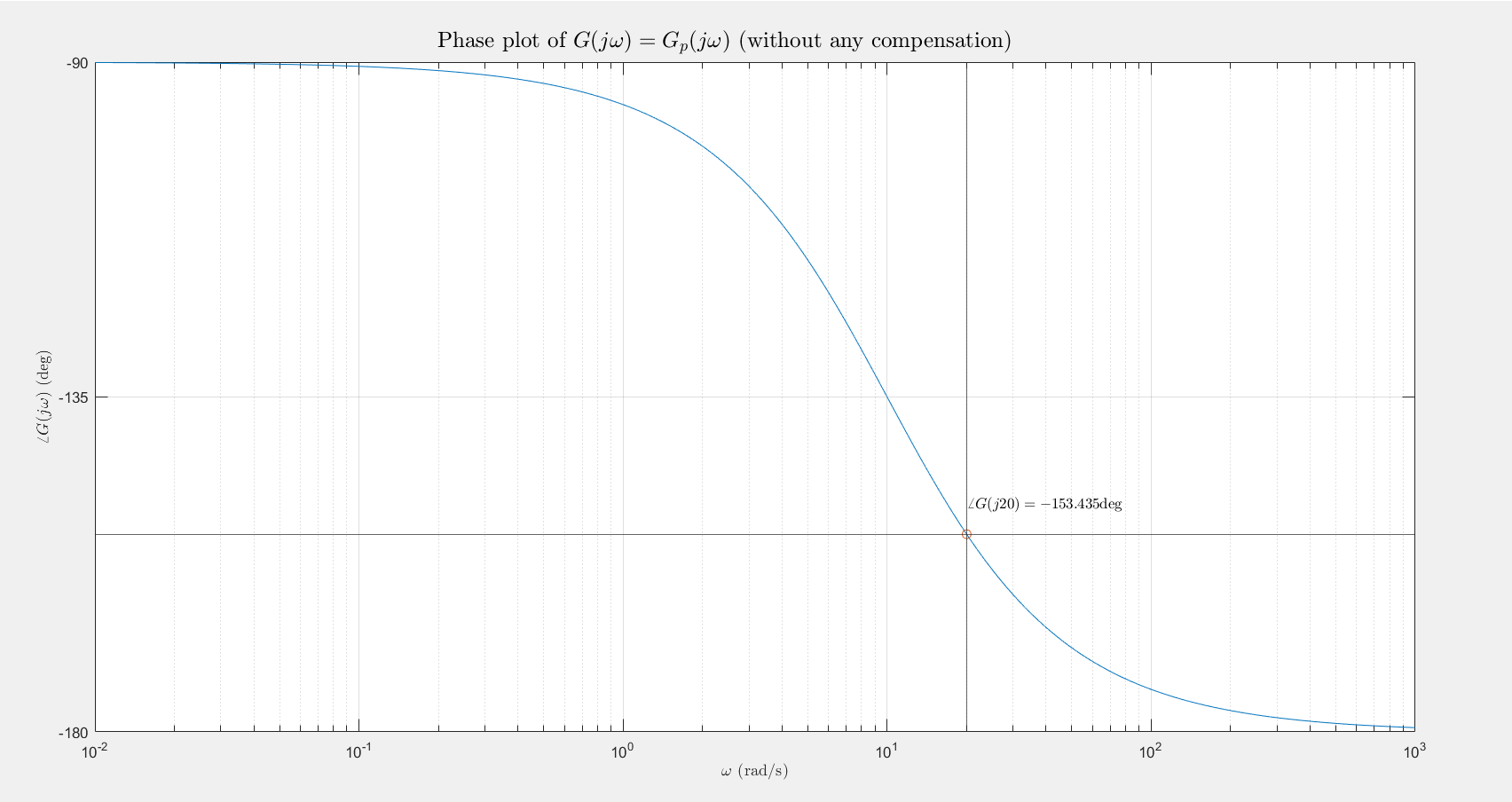
Assignment-3: Lead-Lag Compensator Design

Submitted By:

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In the above block diagram,



# Design of Lead Compensator

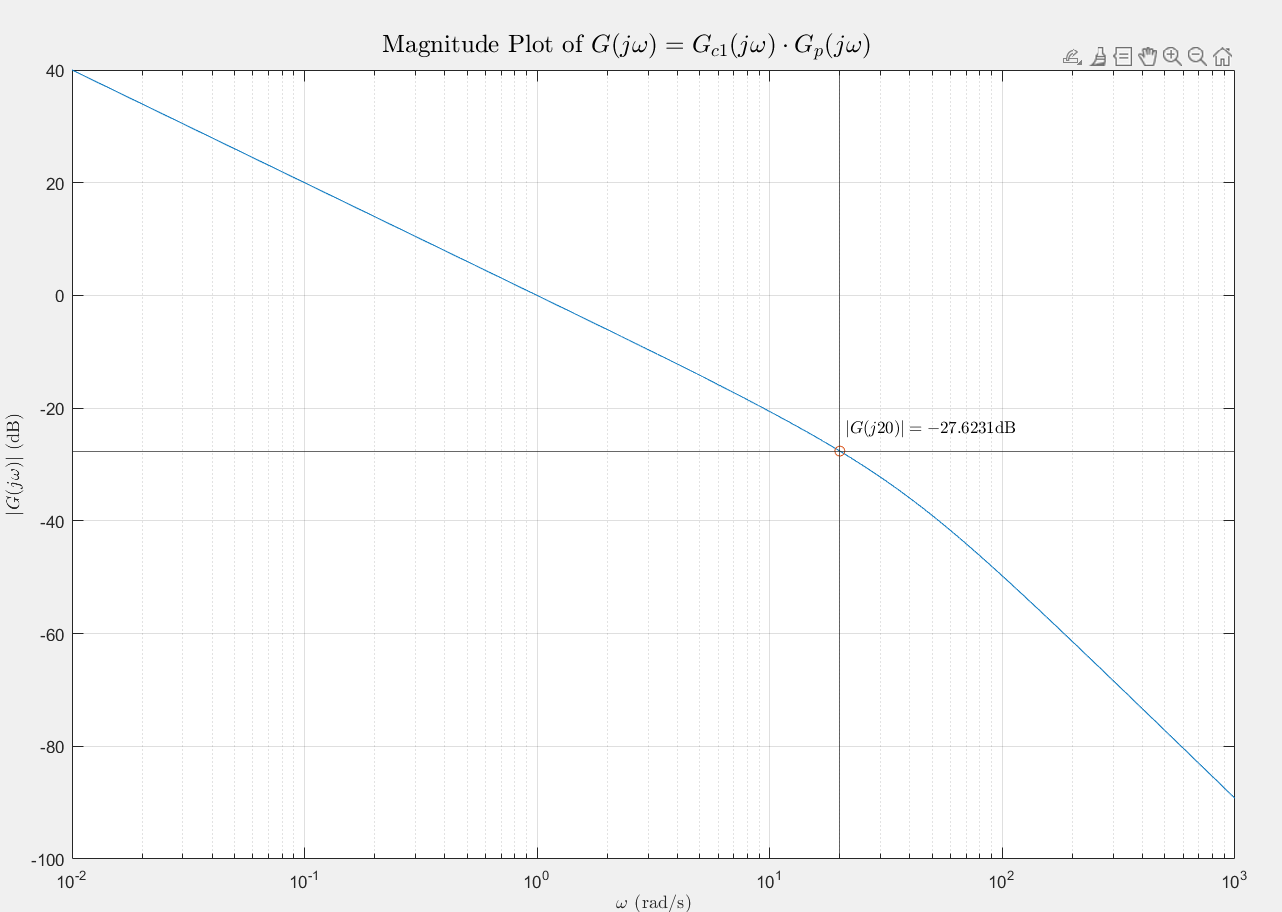
For a lead compensator the controller is assumed to be of form

Where,

From the above plot it can be observed that, uncompensated phase margin is

Therefore, the controller parameters are

|  |  |  |
| --- | --- | --- |
|  |  |  |

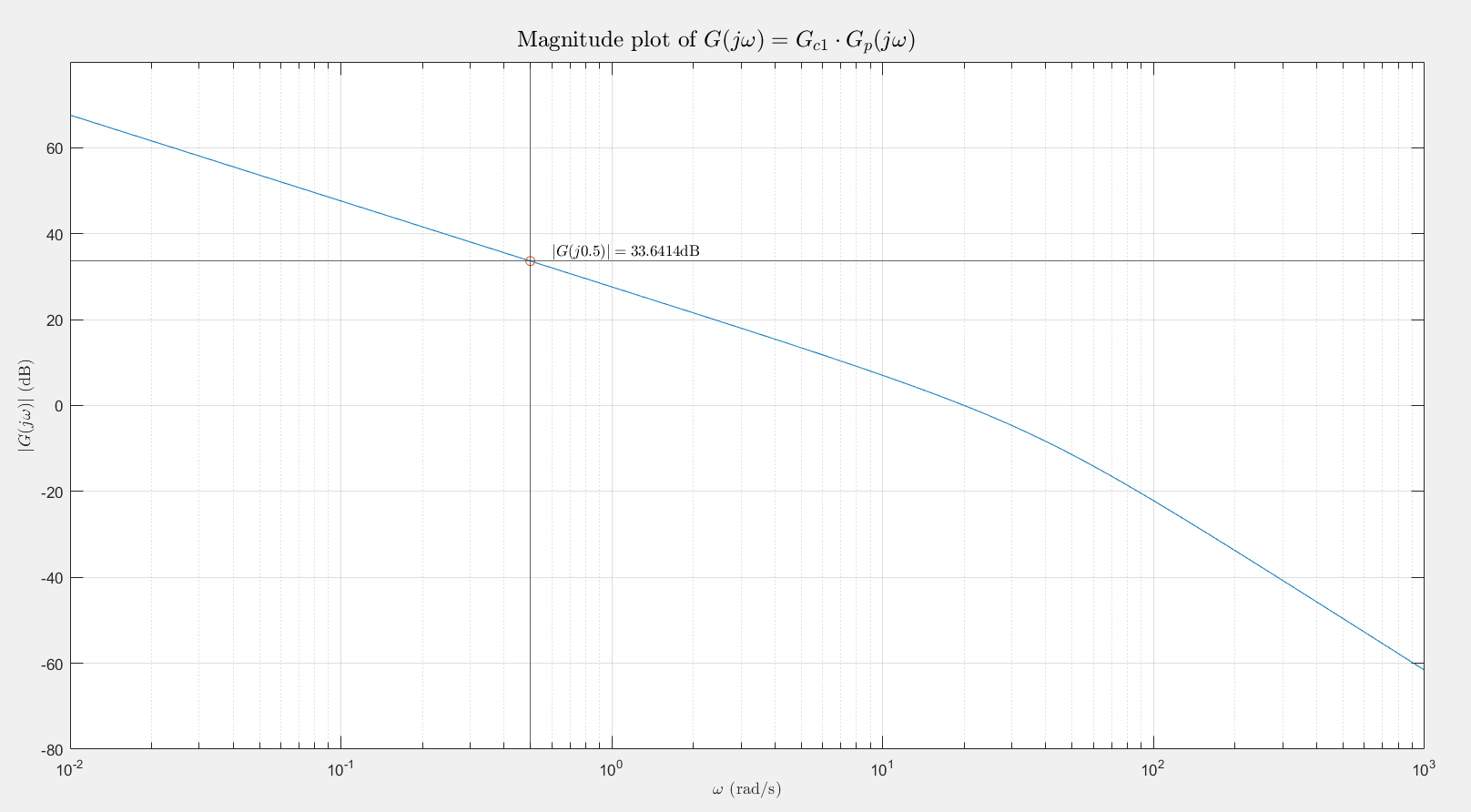


From the graph it can be observed that . Hence to make , the magnitude plot needs to be brought up by . Therefore, our required DC gain is

|  |
| --- |
|  |

# Design of Lag Compensator

For a lag compensator the controlled is assumed to be of form



Where,

Here,

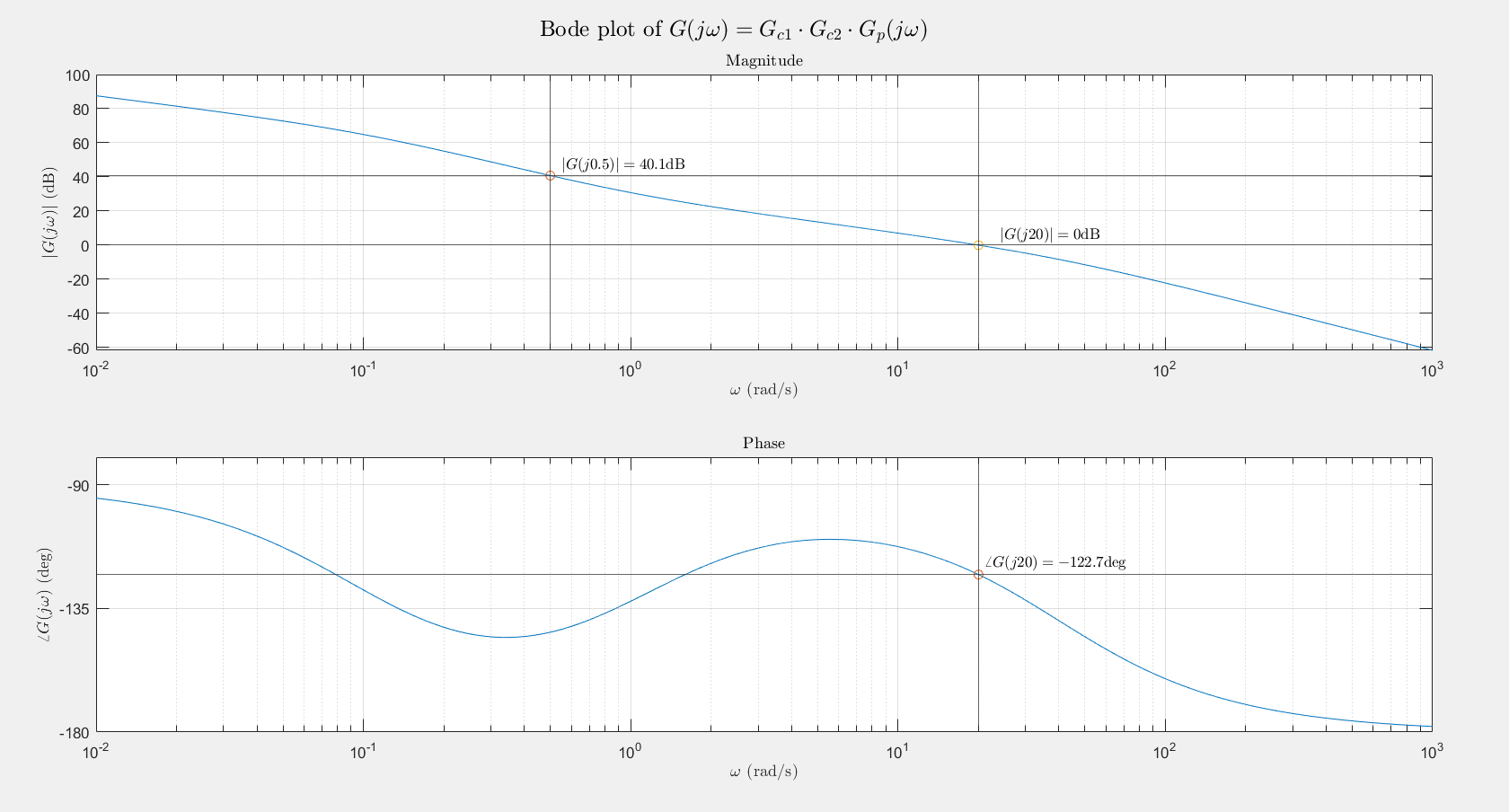
|  |
| --- |
|  |

And from the above plot is observed that . Therefore,

Thus, the controller parameters are

|  |  |
| --- | --- |
|  |  |

# Verification



The compensated system is and from the above plot it can observed that the gain crossover frequency is and the corresponding phase margin is . Also loop gain at as is decreasing in the lower frequencies and .

Thus, the desired specifications are met.