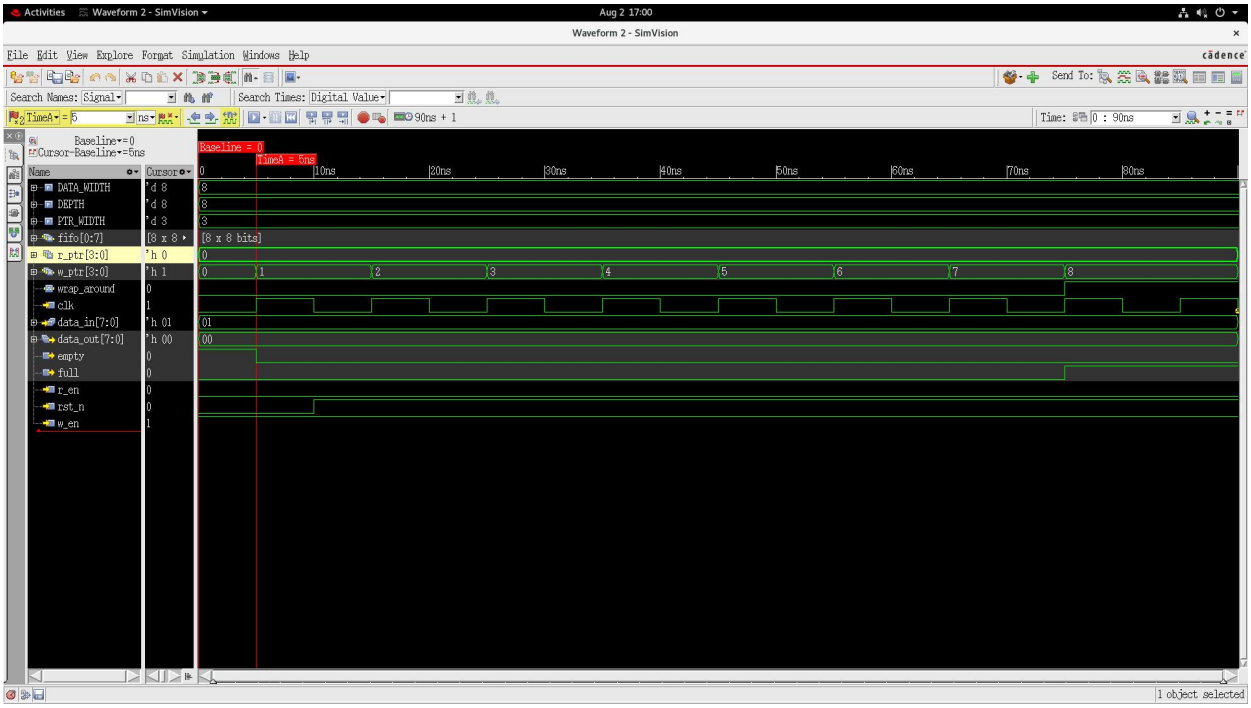
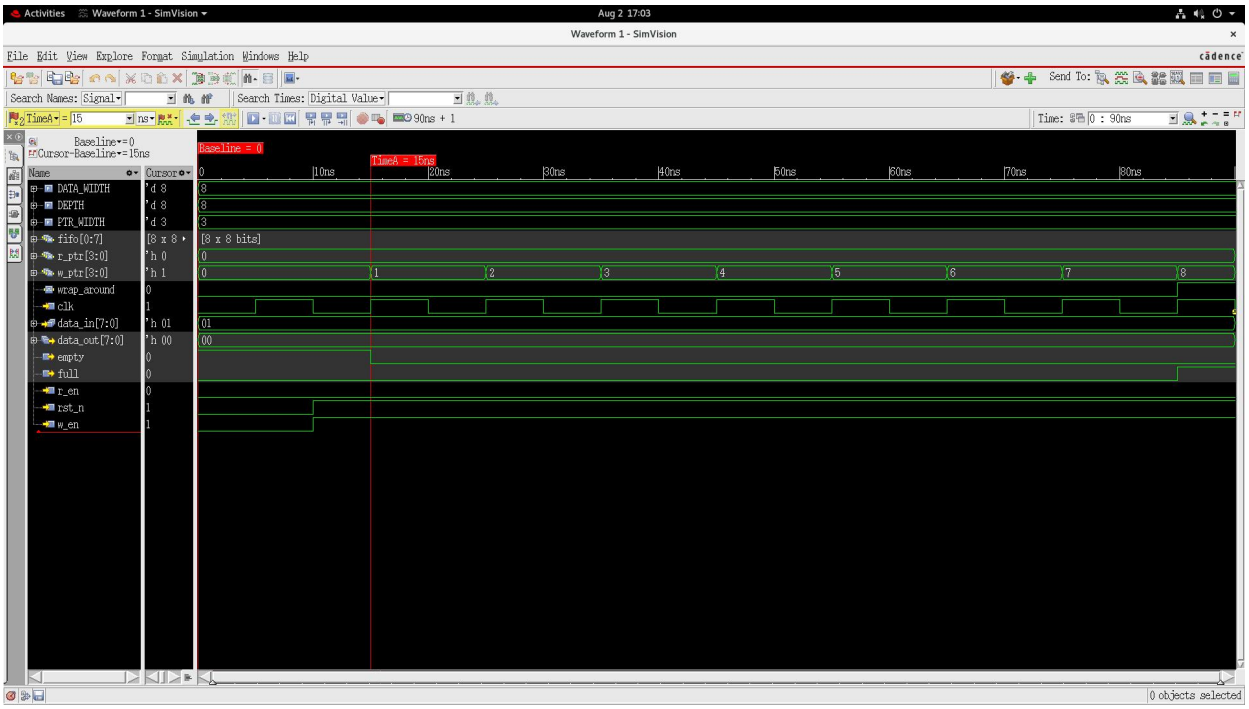
Anis Abid

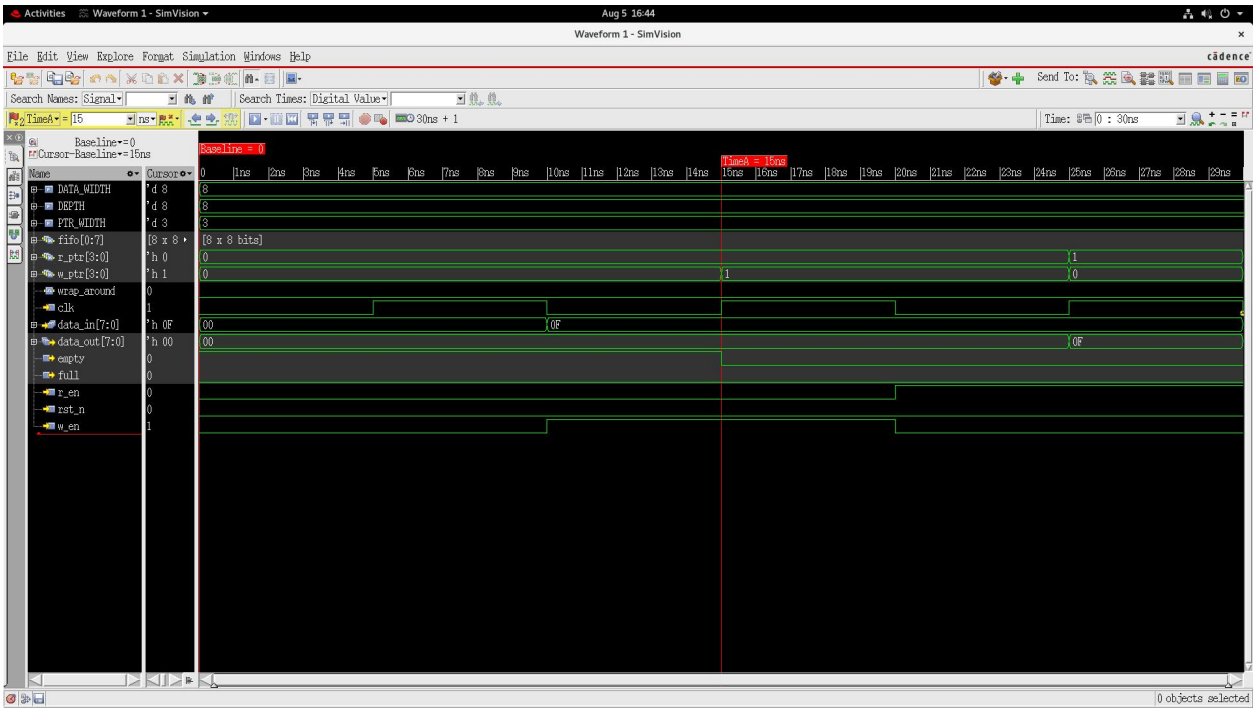
Fifo using layered testbench:

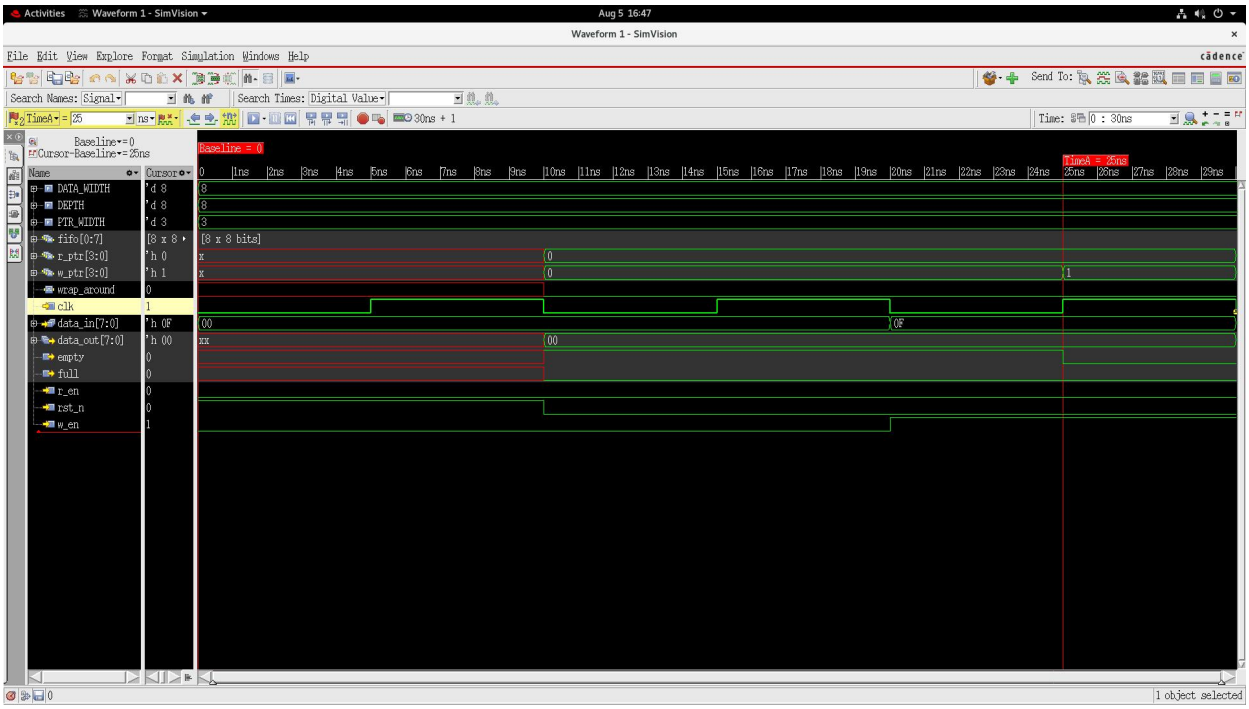
Sr.No.	Test Case	Test Description	Test type	Status	Comments
1.	**FIFO Full**	Writing data into fifo and check fifo full flag on completion. (starts on with reset signal)	Directed	Test Passed	-
2.	**FIFO Empty**	Reading data from the fifo and check the fifo empty flag upon successfully reading all the data.	Directed	Test Passed	Got issues with reset/ fifo in reset state and wr is hardcoded one then empty flag is not working good
3.	**Asynchronous Reset**	Test asynchronous reset behaviour in the middle of reading/writing. Also, it will not depend on clock signal	Directed	Test Failed	Test failed because of the empty flag got high on when reset is asserted and we put wr_en signal along with it
4.	**Read after Write (RAW)**	First write Zero to the fifo and read after writing data.	Directed	Test Passed	-
5.	**Random Data**	Writing random data into the fifo and reading the same data from it.	Random	Test Passed	-
6.	**Depth check**	Write fifo to be greater then the depth and check its flags. Also, read data more then the depth and check if its data is retained or not.	Directed	Test Passed	-

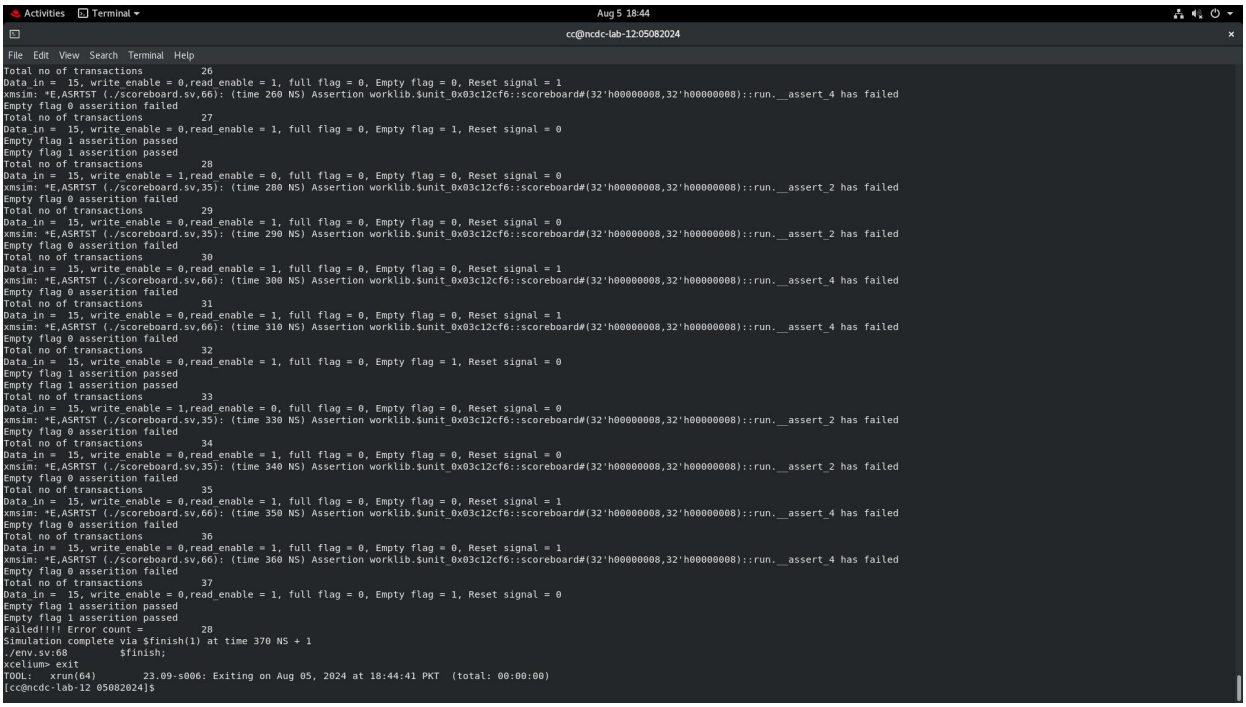
Waveforms

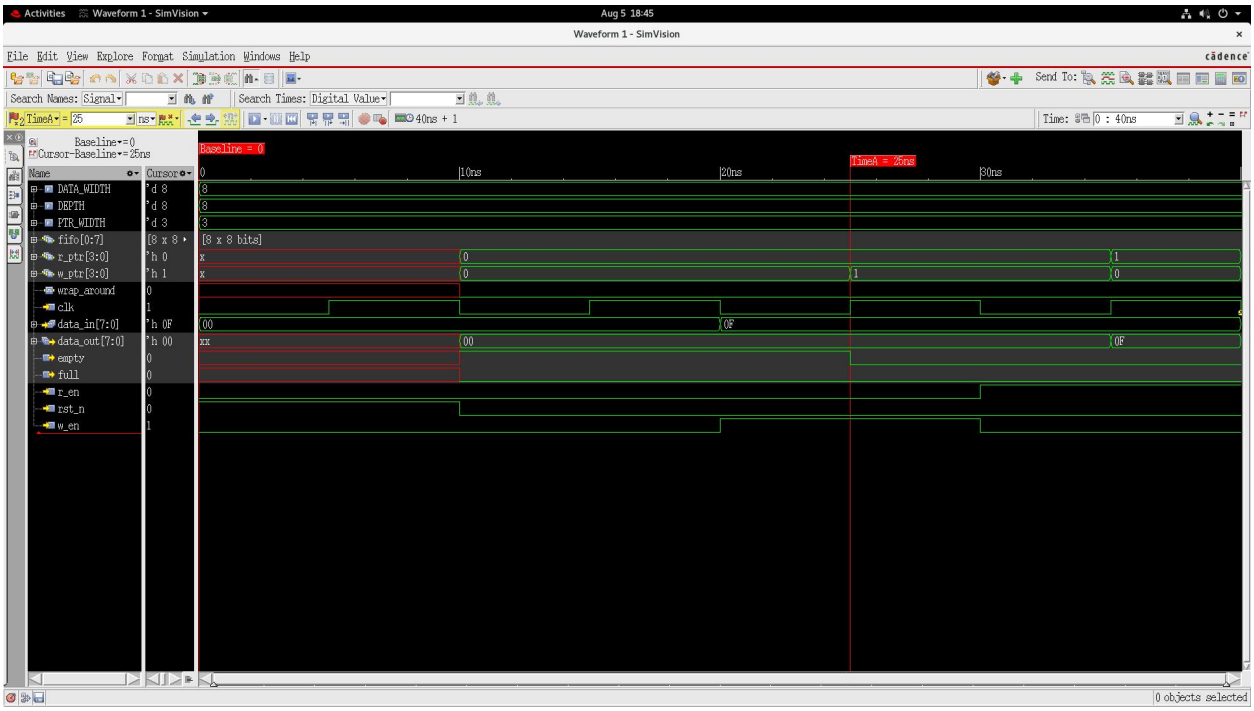

Activities
Waveform 2 - SimVision
Aug 2 17:00
Waveform 2 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Search Names: Signal
Search Times: Digital Value
Send To:
TimeA = 5
ns
90ns + 1
Time: 0 : 90ns
Baseline=0
Cursor-Baseline=5ns
Baseline = 0
TimeA = 5ns
Name
Cursor
DATA_WIDTH
DEPTH
PTR_WIDTH
fifo[0:7]
r_ptr[3:0]
w_ptr[3:0]
wrap_around
clk
data_in[7:0]
data_out[7:0]
empty
full
r_en
rst_n
w_en
'd 8
'd 8
'd 3
[8 x 8 bits]
'h 0
'h 1
'h 01
'h 00
0
1
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
1 object selected


Activities
Waveform 1 - SimVision
Aug 2 17:03
Waveform 1 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Search Names: Signal
Search Times: Digital Value
Send To:
TimeA = 15
ns
90ns + 1
Time: 0 : 90ns
Baseline=0
Cursor-Baseline=15ns
Baseline = 0
TimeA = 15ns
Name
Cursor
DATA_WIDTH
DEPTH
PTR_WIDTH
fifo[0:7]
r_ptr[3:0]
w_ptr[3:0]
wrap_around
clk
data_in[7:0]
data_out[7:0]
empty
full
r_en
rst_n
w_en
'd 8
'd 8
'd 3
[8 x 8 bits]
'h 0
'h 1
'h 01
'h 00
0
1
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
0 objects selected


Activities
Waveform 1 - SimVision
Aug 5 16:44
Waveform 1 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Send To:
Search Names: Signal
Search Times: Digital Value
TimeA = 15
ns
30ns + 1
Time: 0 : 30ns
Baseline=0
Cursor-Baseline=15ns
Baseline = 0
TimeA = 15ns
Name
Cursor
DATA_WIDTH
DEPTH
PTR_WIDTH
fifo[0:7]
r_ptr[3:0]
w_ptr[3:0]
wrap_around
clk
data_in[7:0]
data_out[7:0]
empty
full
r_en
rst_n
w_en
'd 8
'd 8
'd 3
[8 x 8 bits]
'h 0
'h 1
0
1
'h 0F
'h 00
0 objects selected


Activities
Waveform 1 - SimVision
Aug 5 16:47
Waveform 1 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Send To:
Search Names: Signal
Search Times: Digital Value
TimeA = 25
ns
30ns + 1
Time: 0 : 30ns
Baseline=0
Cursor-Baseline=25ns
Baseline = 0
TimeA = 25ns
Name
Cursor
DATA_WIDTH
DEPTH
PTR_WIDTH
fifo[0:7]
r_ptr[3:0]
w_ptr[3:0]
wrap_around
clk
data_in[7:0]
data_out[7:0]
empty
full
r_en
rst_n
w_en
'd 8
'd 8
'd 3
[8 x 8 bits]
'h 0
'h 1
'h 0F
'h 00
0
1
x
xx
1 object selected


Activities
Terminal
Aug 5 18:44
cc@ncdc-lab-12:05082024
File Edit View Search Terminal Help
Total no of transactions 26
Data_in = 15, write_enable = 0,read_enable = 1, full flag = 0, Empty flag = 0, Reset signal = 1
xmsim: *E,ASRTST (./scoreboard.sv,66): (time 260 NS) Assertion worklib.$unit_0x03c12cf6::scoreboard#(32'h00000008,32'h00000008)::run.__assert_4 has failed
Empty flag 0 assertion failed
Total no of transactions 27
Data_in = 15, write_enable = 0,read_enable = 1, full flag = 0, Empty flag = 1, Reset signal = 0
Empty flag 1 assertion passed
Empty flag 1 assertion passed
Total no of transactions 28
Data_in = 15, write_enable = 1,read_enable = 0, full flag = 0, Empty flag = 0, Reset signal = 0
xmsim: *E,ASRTST (./scoreboard.sv,35): (time 280 NS) Assertion worklib.$unit_0x03c12cf6::scoreboard#(32'h00000008,32'h00000008)::run.__assert_2 has failed
Empty flag 0 assertion failed
Total no of transactions 29
Data_in = 15, write_enable = 0,read_enable = 1, full flag = 0, Empty flag = 0, Reset signal = 0
xmsim: *E,ASRTST (./scoreboard.sv,35): (time 290 NS) Assertion worklib.$unit_0x03c12cf6::scoreboard#(32'h00000008,32'h00000008)::run.__assert_2 has failed
Empty flag 0 assertion failed
Total no of transactions 30
Data_in = 15, write_enable = 0,read_enable = 1, full flag = 0, Empty flag = 0, Reset signal = 1
xmsim: *E,ASRTST (./scoreboard.sv,66): (time 300 NS) Assertion worklib.$unit_0x03c12cf6::scoreboard#(32'h00000008,32'h00000008)::run.__assert_4 has failed
Empty flag 0 assertion failed
Total no of transactions 31
Data_in = 15, write_enable = 0,read_enable = 1, full flag = 0, Empty flag = 0, Reset signal = 1
xmsim: *E,ASRTST (./scoreboard.sv,66): (time 310 NS) Assertion worklib.$unit_0x03c12cf6::scoreboard#(32'h00000008,32'h00000008)::run.__assert_4 has failed
Empty flag 0 assertion failed
Total no of transactions 32
Data_in = 15, write_enable = 0,read_enable = 1, full flag = 0, Empty flag = 1, Reset signal = 0
Empty flag 1 assertion passed
Empty flag 1 assertion passed
Total no of transactions 33
Data_in = 15, write_enable = 1,read_enable = 0, full flag = 0, Empty flag = 0, Reset signal = 0
xmsim: *E,ASRTST (./scoreboard.sv,35): (time 330 NS) Assertion worklib.$unit_0x03c12cf6::scoreboard#(32'h00000008,32'h00000008)::run.__assert_2 has failed
Empty flag 0 assertion failed
Total no of transactions 34
Data_in = 15, write_enable = 0,read_enable = 1, full flag = 0, Empty flag = 0, Reset signal = 0
xmsim: *E,ASRTST (./scoreboard.sv,35): (time 340 NS) Assertion worklib.$unit_0x03c12cf6::scoreboard#(32'h00000008,32'h00000008)::run.__assert_2 has failed
Empty flag 0 assertion failed
Total no of transactions 35
Data_in = 15, write_enable = 0,read_enable = 1, full flag = 0, Empty flag = 0, Reset signal = 1
xmsim: *E,ASRTST (./scoreboard.sv,66): (time 350 NS) Assertion worklib.$unit_0x03c12cf6::scoreboard#(32'h00000008,32'h00000008)::run.__assert_4 has failed
Empty flag 0 assertion failed
Total no of transactions 36
Data_in = 15, write_enable = 0,read_enable = 1, full flag = 0, Empty flag = 0, Reset signal = 1
xmsim: *E,ASRTST (./scoreboard.sv,66): (time 360 NS) Assertion worklib.$unit_0x03c12cf6::scoreboard#(32'h00000008,32'h00000008)::run.__assert_4 has failed
Empty flag 0 assertion failed
Total no of transactions 37
Data_in = 15, write_enable = 0,read_enable = 1, full flag = 0, Empty flag = 1, Reset signal = 0
Empty flag 1 assertion passed
Empty flag 1 assertion passed
Failed!!!! Error count = 28
Simulation complete via $finish(1) at time 370 NS + 1
./env.sv:68 $finish;
xcelium> exit
TOOL: xrun(64) 23.09-s006: Exiting on Aug 05, 2024 at 18:44:41 PKT (total: 00:00:00)
[cc@ncdc-lab-12 05082024]$


Activities
Waveform 1 - SimVision
Aug 5 18:45
Waveform 1 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Send To:
Search Names: Signal
Search Times: Digital Value
TimeA = 25
ns
40ns + 1
Time: 0 : 40ns
Baseline=0
Cursor-Baseline=25ns
Baseline = 0
TimeA = 25ns
Name
Cursor
0
10ns
20ns
30ns
DATA_WIDTH
DEPTH
PTR_WIDTH
fifo[0:7]
r_ptr[3:0]
w_ptr[3:0]
wrap_around
clk
data_in[7:0]
data_out[7:0]
empty
full
r_en
rst_n
w_en
'd 8
'd 8
'd 3
[8 x 8]
[8 x 8 bits]
'h 0
'h 1
'h 0F
'h 00
0 objects selected

Coverage of write and read signals, also of data input bins using at least option