Anish **Saxena**

Senior Undergraduate

Indian Institute of Technology Kanpur · Mechanical Engineering

(+91) 7405-80-5164 | anish.saxena@outlook.com | anish-saxena.github.io | Anish-Saxena | Anish-Saxena

Education

Indian Institute of Technology Kanpur — *Kanpur, India*

Bachelor of Technology, Mechanical Engineering/ **CPI: 9.0/10.0** — *2017 - 2021 (exp.)*

- Minor in Computer Systems

St. Kabir School — *Ahmedabad, India*

Central Board of Secondary Education Class XII: **94.4%** | **School Topper** — *2017*

CBSE Class X: **CGPA: 10.0/10.0** | **Certificate of Merit** — *2015*

Honors & Awards

2019 **Semiconductor Research Corporation Student Member**, Indian Research Program — *India*

2017 **Aditya Birla Group Scholarship**, Awarded to 15 students selected from IITs and BITS — *Mumbai*

2017 **All India Rank 1828**, Joint Entrance Examination Advanced, 175,000 students — *India*

2017 **KVPY Fellowship**, Awarded by IISc Bangalore and Government of India — *Bangalore*

Work Experience

Processor Architecture Research Lab — *Intel Labs, India*

Architecture Research Intern — *May 2020 - Sep. 2020*

- Implemented and analyzed research ideas and improved the performance of non-inclusive cache hierarchy.
- Extended a state-of-the-art research simulator, collected memory traces, and performed cache simulations.
- Reduced simulation time by more than 10× and maintained greater than 99% correlation to full simulation.
- Devised efficient implementations to track novel parameters like reuse distance that affect cache policy.
- Developed custom cache policies and examined performance against oracular policies like Belady for workload traces to quantify gains achieved.

CAR3S Group, IIT Kanpur — *Prof. Biswabandan Panda*

Group Member — *Apr. 2019 - Jun. 2020*

- Improved accuracy of attacks that exploit instruction execution latency variation caused by processor caches.
- Identified that Dynamic Voltage and Frequency Scaling (DVFS) and OS scheduling affect execution latency.
- Introduced noise-aware calibration, periodic feedback, and victim profiling to optimize baseline attacks.
- Designed and implemented DABANGG, a novel set of refinements to efficiently incorporate optimizations.
- Conducted experiments, mounted attacks on AES and RSA cryptosystems in OpenSSL and GnuPG libraries.
- First author of the work under submission to the IEEE Symposium on Security and Privacy, 2021; funded by NXP Semiconductors; accessible at iacr://2020/637.

New York Office, IIT Kanpur — *Prof. Manindra Agrawal*

Computer Systems Intern — *May 2018 - Jul. 2018*

- Led a team of 4 to develop the infrastructure stack of a scalable microservice-based web portal.
- Implemented Spinnaker to deploy Docker images continuously and immutably to Kubernetes cluster.
- Configured pipelines auto-triggered by Concourse Continuous Integration (CI) workflow for Spinnaker.
- Integrated Clair static vulnerability analysis tool to flag buggy Docker images and fail the build in CI stage.
- Implemented Amazon S3 authentication-enabled snapshot facility in Elasticsearch-operator.
- Added Canary analysis stage to the pipeline and integrated Locust load testing framework in this stage.

Relevant Coursework

- Advanced Computer Architecture[i]
- Operating Systems[A]
- Programming for Performance[i]
- Computer Architecture[A*]
- Computer Organization[A]
- Introduction to Programming[A]
- Topics in Operating Systems
- Data Structures & Algorithms
- Non Classical Logic

A: grade for exceptional performance* *A: grade* *i: in progress*

Projects

Compression Algorithms for Caches
Project Member

CAR3S Group, IIT Kanpur — *Jul. 2020 - present*

- Mentored by Prof. Biswabandan Panda and funded by Qualcomm Research.
- Improved bandwidth of cache hierarchy in heterogeneous System-on-Chip (SoC).
- Collected Memory Access Traces (MAT) from Android applications and designed compression algorithms.
- Extended QEMU, the emulator used by Android Studio, to collect MAT from Android 9.0 API with x86_64 ABI.
- Modified Valgrind, a memory profiling framework, to collect MAT natively from ARMv8-A based devices.
- Extended ChampSim, a trace-driven simulator, to utilize MAT and run fine-grained memory simulations.

SMA Actuator-based Space Antenna
Prof. Sahil Kalra

Space Technology Cell, IIT Kanpur — *Jan. 2019 - Feb. 2019*

- Developed mechanism for ISRO to allow motion of antenna deployed in satellite with 3 degrees of freedom.
- Utilized motor and integrated State Memory Alloy (SMA) actuator to allow movement of axis of rotation.
- Planned to use ISRO's NavIC chip to allow transmission and reception of signals to control the antenna.

Campus Sustainability Challenge
Team Leader

7TH Inter-IIT Tech Meet, IIT Bombay — *Oct. 2018 - Dec. 2018*

- Led a team of 6 to propose and implement solutions for waste generated on the institute campus.
- Mounted sensors in composting bins, captured Biogas, reduced PNG consumption in hostel messes by 14%.
- Configured E-Waste Management Software, modelled E-waste generation, analyzed disposal frequency, environmental and economic factors, and identified optimal combination of recycling techniques.

E-Waste Management Software
Prof. Indranil Saha

Course Project — *Aug. 2017 - Nov. 2017*

- Given E-waste disposal behavior and constraints on economic and environmental resources, identified the optimal path to safely and efficiently treat the E-waste.
- Modelled the path-finding algorithm from scratch to perform linear optimization of 8 parameters, like amortized cost, subject to 20 constraints, like efficiency, per process.
- Developed in Visual C++ and .NET framework; accessible at github://Anish-Saxena/E-Waste-Management/.

Skills

Programming C++, C, Python, Golang, Java, Bash

Frameworks Pthreads, OpenMP, CUDA, Locust, ANTLR, Valgrind

Utilities Git, Vim, LaTeX, QEMU, ChampSim, GDB, Docker, Kubernetes, Concourse, Spinnaker

Extracurricular Activities

2020 **Systems Reading Group**, Leader — *IIT Kanpur*
Conducted series of talks to discuss basic and advanced topics in systems research.

2019 **Programming Club**, Coordinator — *IIT Kanpur*
Guided a team of 24, conducted workshops, organized hackathons, and delivered lectures.

2019 **HDL & Digital Design**, Programming Club Project — *IIT Kanpur*
Mentored 5 students to develop a 16-bit pipelined processor and synthesized it on FPGA.

2018 **Clean Coder**, Association for Computing Activities Project — *IIT Kanpur*
Developed a filesystem using Go-FUSE to sandbox a guest user on a host filesystem.

Miscellaneous

- Represented CAR3S group in departmental seminars and maintained the group website. *2020*
- Delivered a lecture on DABANG in a graduate-level course on Secure Memory Systems. *2019*
- Delivered talks on ZombieLoad and CLK_{screw} attacks through CAOS reading group. *2019*
- Two-time regional finalist of TCS IT Wiz Quiz. *2014, 2016*