main_fpga_aes_256 Project Status			
Project File:	Main_FPGA.xise	**Parser Errors:**	No Errors
Module Name:	main_fpga_aes_256	**Implementation State:**	Programming File Generated
Target Device:	xc6slx75-3csg484	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	17 Warnings (15 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	X 1 Failing Constraint
Environment:	System Settings	• **Final Timing Score:**	64 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	3,526	93,296	3%	
Number used as Flip Flops	3,526			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	2,742	46,648	5%	
Number used as logic	2,626	46,648	5%	
Number using O6 output only	2,348			
Number using O5 output only	0			
Number using O5 and O6	278			
Number used as ROM	0			
Number used as Memory	0	11,072	0%	
Number used exclusively as route-thrus	116			
Number with same-slice register load	116			
Number with same-slice carry load	0			
Number with other load	0			
Number of occupied Slices	1,473	11,662	12%	
Number of MUXCYs used	92	23,324	1%	
Number of LUT Flip Flop pairs used	4,517			
Number with an unused Flip Flop	1,244	4,517	27%	
Number with an unused LUT	1,775	4,517	39%	
Number of fully used LUT-FF pairs	1,498	4,517	33%	
Number of unique control sets	28			
Number of slice register sites lost to control set restrictions	58	93,296	1%	
Number of bonded IOBs	35	328	10%	
Number of LOCed IOBs	35	35	100%	
IOB Flip Flops	5			
Number of RAMB16BWERs	0	172	0%	
Number of RAMB8BWERs	8	344	2%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	2	16	12%	
Number used as BUFGs	2			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	12	0%	
Number of ILOGIC2/ISERDES2s	0	442	0%	

Number of IODELAY2/IODRP2/IODRP2_MCBs	0	442	0%	
Number of OLOGIC2/OSERDES2s	5	442	1%	
Number used as OLOGIC2s	5			
Number used as OSERDES2s	0			
Number of BSCANs	0	4	0%	
Number of BUFHs	0	384	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	132	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	4	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	6	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	4.94			

Performance Summary [+]

Detailed Reports [+]

Secondary Reports [+]

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