Uvodna vježba iz Digitalne elektronike

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Digitalna elektronika

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- Vježbe će se izvoditi online
- Svaka vježba se boduje i potrebno je da je uradite samostalno
- Na vježbama za koje je potrebno biće postavljen pripremni materijal

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- Za izradu prvog dijela vježbi vježbi koristiće se GHDL softver za kompilaciju i simulaciju VHDL koda
  https://github.com/ghdl/ghdl
- Za izradu drugog dijela vježbi koristiće se Proteus softverski paket
  www.labcenter.com/downloads/

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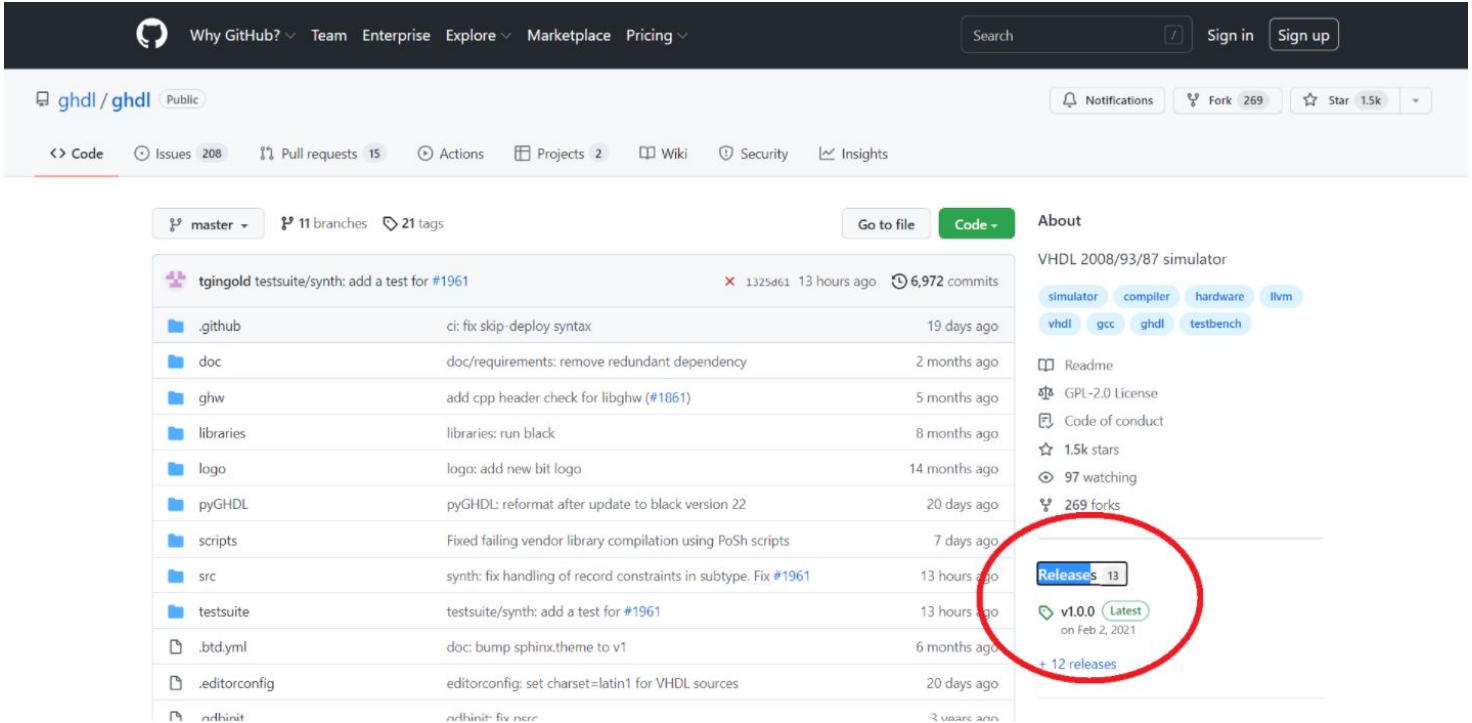
- GHDL softver možete preuzeti sa GitHub stranice:



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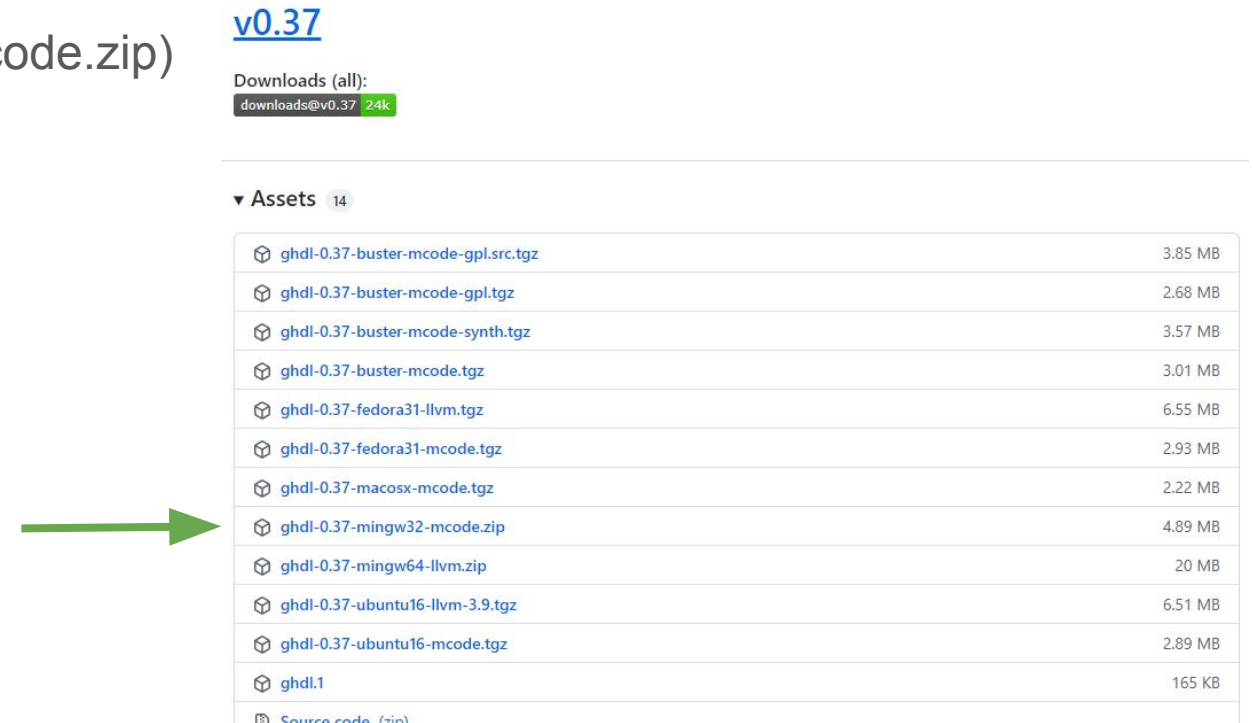
- Otići na releases i zatim preuzeti verziju v0.37

(ghdl-0.37.mingw32-mscode.zip)



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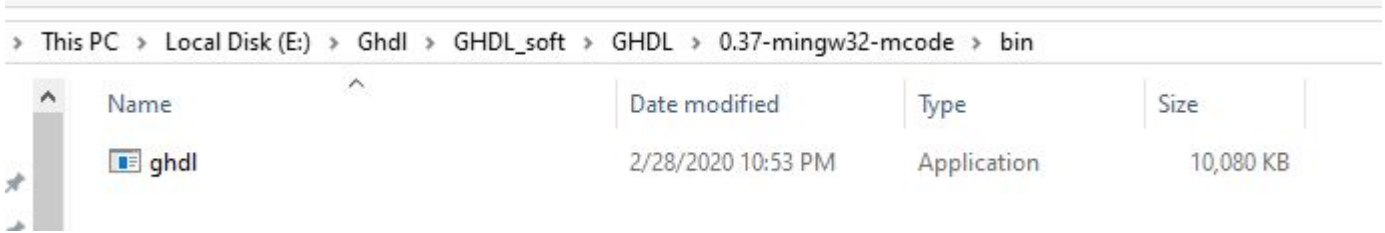
- Preuzete fajlove ekstraktovati u folder po želji

- Putanju (vaša putanja)/bin dodati u Environment Path



(Primjer putanje E:\Ghdl\GHDL_soft\bin)

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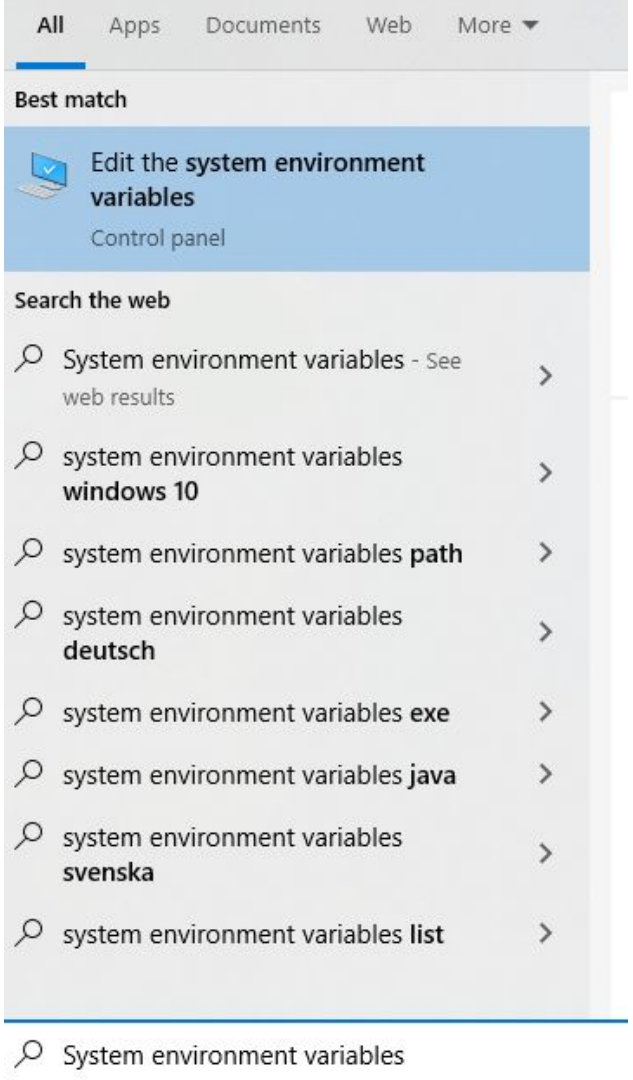
Priskom na *windows* dugme dobijate mogućnost unosa teksta. Tu ćete potražiti System environment variables.



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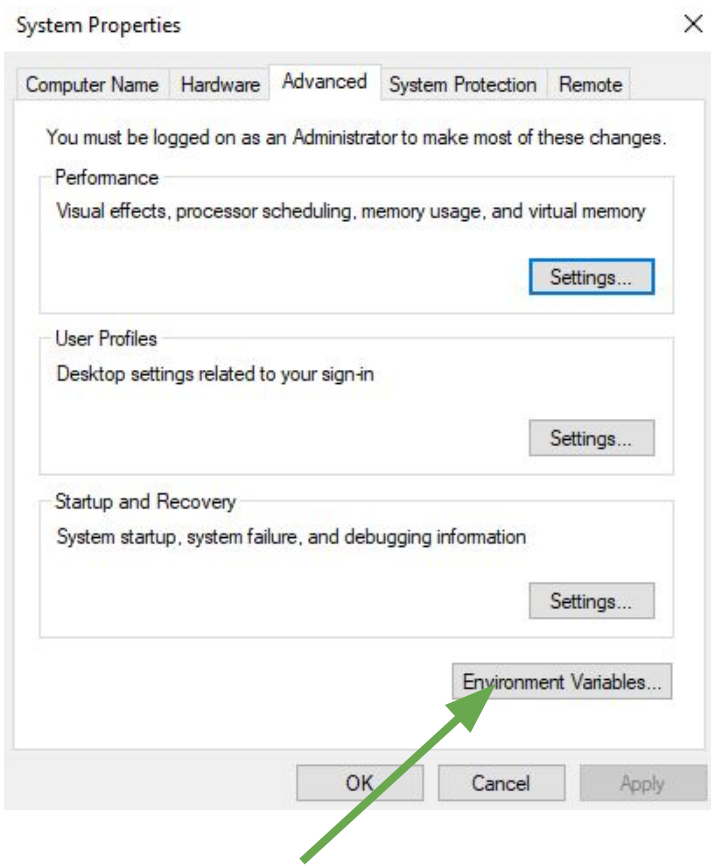
Zatim “Environment Variables”



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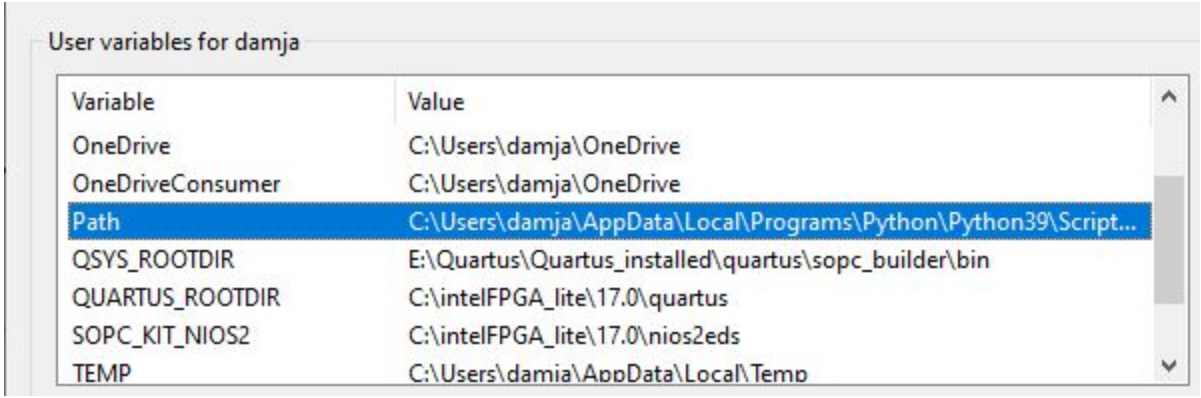
Zatim u PATH varijablu dodati prethodno navedenu putanju.



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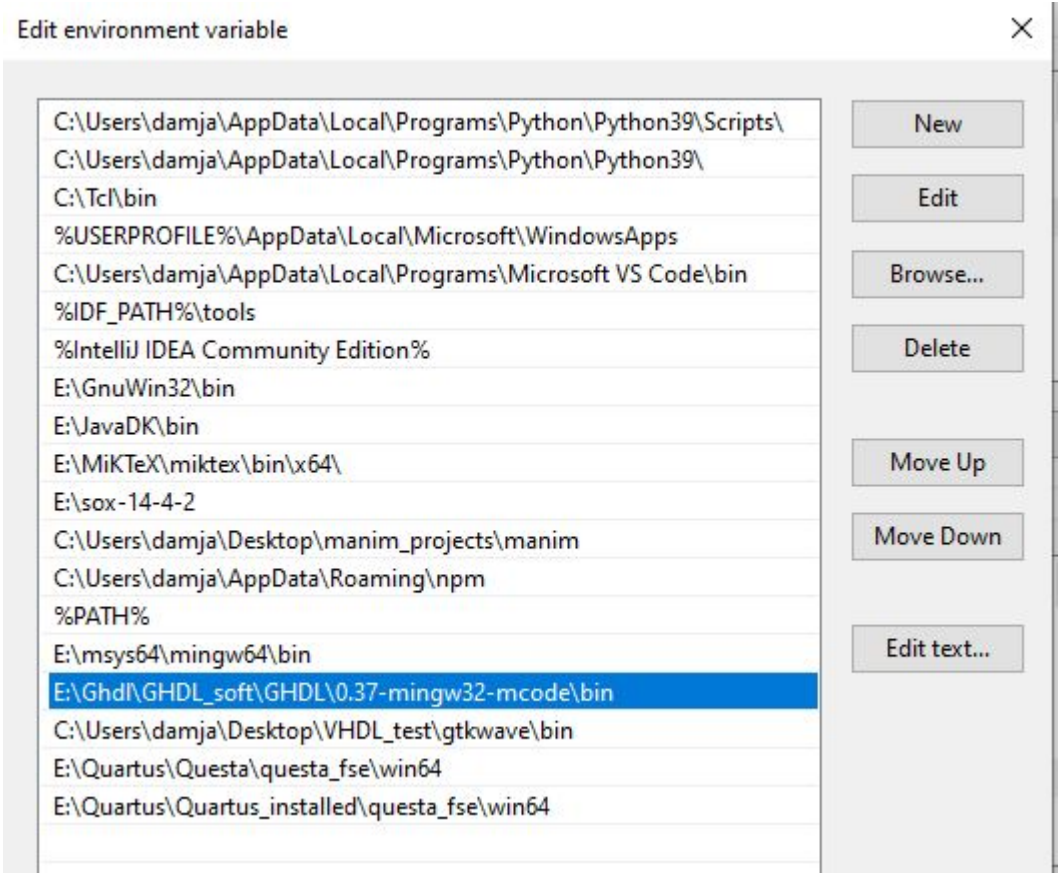

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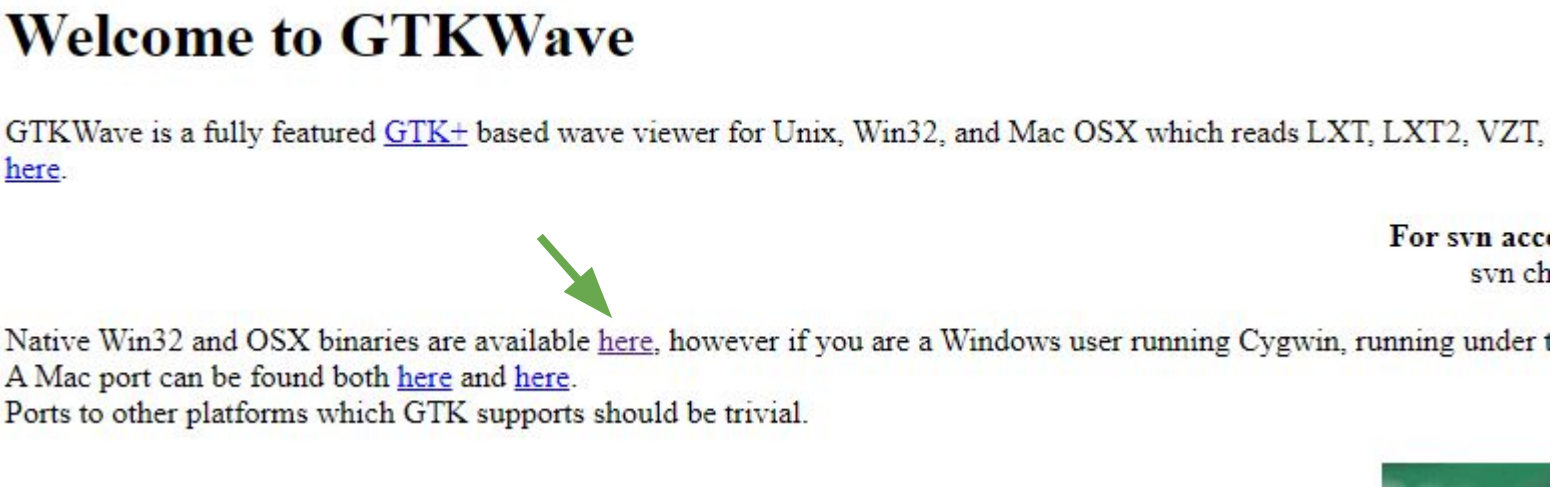
Da bi se mogli vizuelizovati rezultati simulacije, potrebano je preuzeti GTKWave softver.

gtkwave.sourceforge.net/



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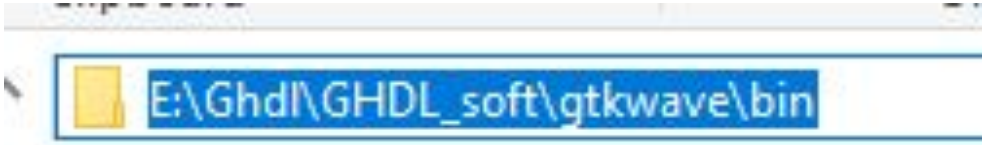
- Ponovo ekstraktujete preuzete fajlove u željeni folder i dodate bin folder od GTKWave softvera u PATH varijablu kao i za GHDL.

Primjer putanje:



E:\Ghdl\GHDL_soft\gtkwave\bin

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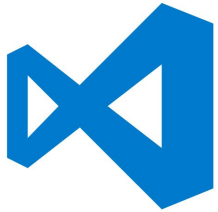
Sada je sve spremno da testirate instalirani softver.

Otvorite editor teksta po izboru. Preporuka: koristite VSC (Visual Studio Code)

code.visualstudio.com



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Napravite novi fajl, pod nazivom prviTest.VHDL i u njega unesite:

```
library IEEE;
use IEEE.std_logic_1164.all;

entity or_gate is
port(
  a: in std_logic;
  b: in std_logic;
  q: out std_logic);
end or_gate;

architecture rtl of or_gate is
begin
  process(a, b) is
  begin
    q <= a or b;
  end process;
end rtl;
```

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Zatim ponovo napravite novi fajl (prviTestTestbench.VHDL) i unjega unesite testbenč za prethodno napisano ILI kolo u prvom testu.

```
library IEEE;
use IEEE.std_logic_1164.all;

entity testbench is
end testbench;

architecture tb of testbench is

component or_gate is
port(
  a: in std_logic;
  b: in std_logic;
  q: out std_logic);
end component;

signal a_in, b_in, q_out: std_logic;

begin

  DUT: or_gate port map(a_in, b_in, q_out);

 process
  begin
    a_in <= '0';
    b_in <= '0';
    wait for 1 ns;
    assert(q_out='0') report "Fail 0/0" severity error;

    a_in <= '0';
    b_in <= '1';
    wait for 1 ns;
    assert(q_out='1') report "Fail 0/1" severity error;

    a_in <= '1';
    b_in <= 'X';
    wait for 1 ns;
    assert(q_out='1') report "Fail 1/X" severity error;

    a_in <= '1';
    b_in <= '1';
    wait for 1 ns;
    assert(q_out='1') report "Fail 1/1" severity error;

    -- Clear inputs
    a_in <= '0';
    b_in <= '0';

    assert false report "Test done." severity note;
    wait;
  end process;
end tb;
```

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Sada kada je VHDL kod i testbenč napisan. Potrebno je kompajlirati kod i izvršiti simulaciju.

Na linku se nalazi detaljno opisan GHDL softver: ghdl.free.fr/ghdl/index.html

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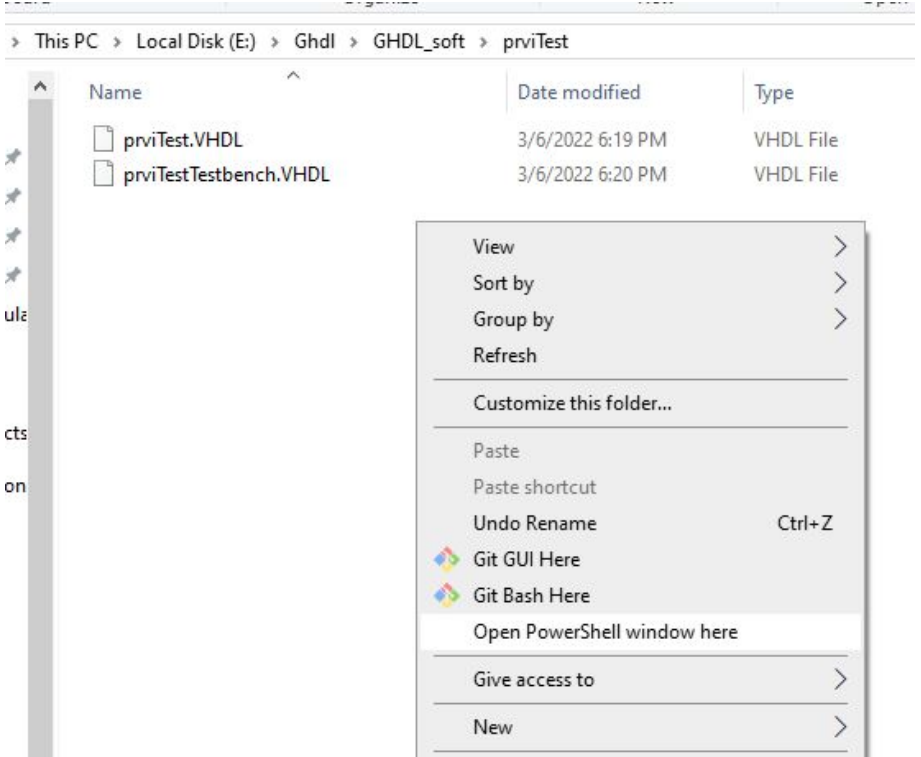
Otvorite command shell ili Power shell i postavite se na mjesto gdje ste sačuvali vaše VHDL fajlove.

Da bi ste dobili opciju
Open PowerShell window here
Potrebno je da držite taster shift
I izvršite desni pritisak miša na
Prazan prostor.



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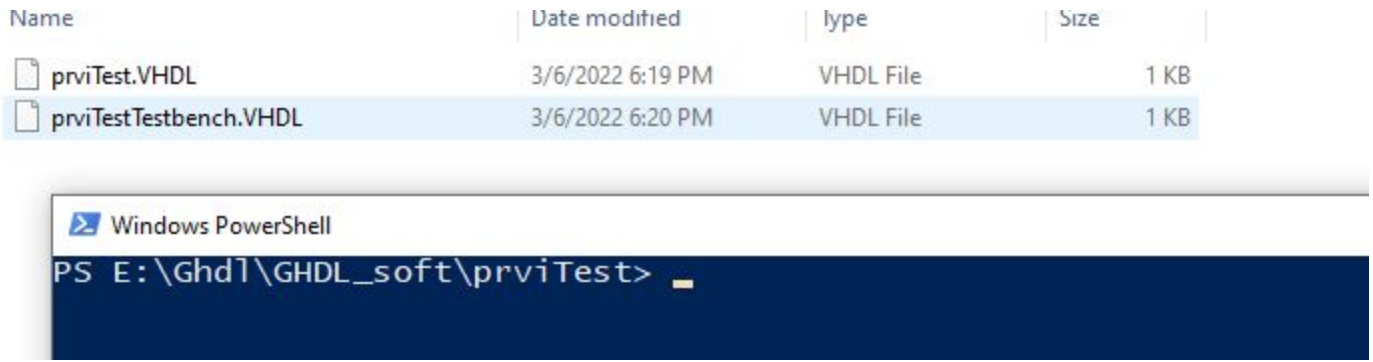
Prikaz dijela prozora PowerShell-a



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Da biste kompajlirai vaš VHDL kod, u powerShell unesite naredbu:

ghdl -a prviTest.vhdl

Izvršenje ove naredbe rezultuje CF File fajlom (npr. work-obj93.cf) ili greškom u slučaju da imate nekih nepravilnosti u VHDL kodu. Kada dobijete cf fajl, to znači da vaš VHDL nema greške u sintaksi.

Isto uraditi i za testbenč.

ghdl -a prviTestTestbench.vhdl

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Nakon toga, napravite izvršni fajl tako što pokrenete testbenč naredbom u powerShell-u

ghdl -e or_gate

(or_gate je naziv komponente koja se testira)

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Za vizuelizaciju signala iz simulacije koristi se GTKWave.

Prije vizuelizacije se izvršava naredba:

ghdl -r or_gate --vcd=prviTest_vcd.vcd

da bi se dobio vcd fajl.

Nakon toga naredbu:

gtkwave prviTest_vcd.vcd

za vizuelizaciju.

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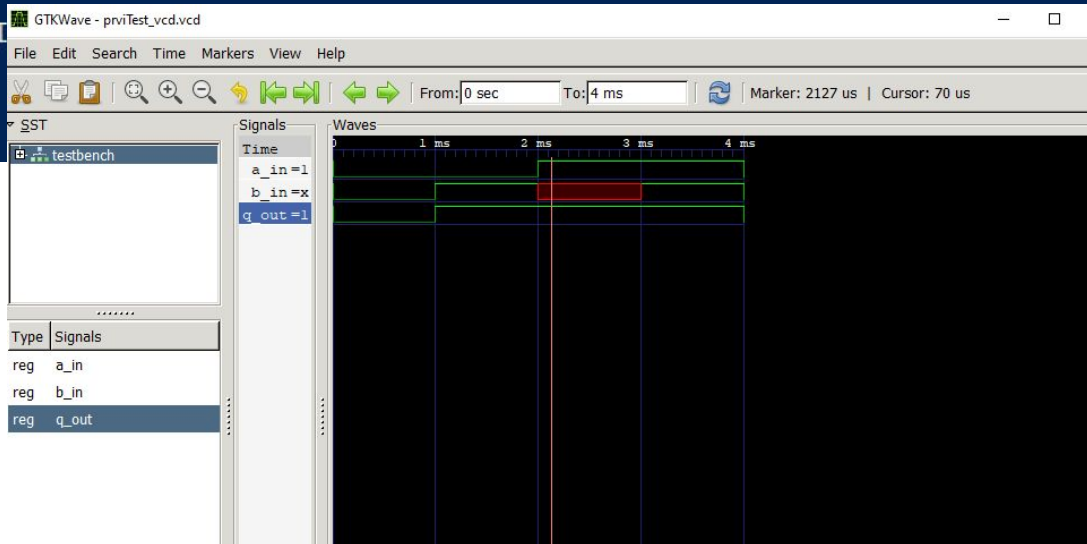
Windows PowerShell

```
PS E:\Ghdl\GHDL_soft\prviTest> ghdl -a prviTest.vhdl
PS E:\Ghdl\GHDL_soft\prviTest> ghdl -a prviTestTestbench.vhdl
PS E:\Ghdl\GHDL_soft\prviTest> ghdl -e tb
E:\Ghdl\GHDL_soft\GHDL\0.37-mingw32-mcode\bin\ghdl.exe: cannot find entity or configuration tb
PS E:\Ghdl\GHDL_soft\prviTest> ghdl -e or_gate
PS E:\Ghdl\GHDL_soft\prviTest> ghdl -r testbench --vcd=prviTest_vcd.vcd
prviTestTestbench.vhdl:50:5:@4ms:(assertion note): Test done.
PS E:\Ghdl\GHDL_soft\prviTest> gtkwave prviTest_vcd.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[40000000000000] end time.
```



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