ECSE 222 (DIGITAL LOGIC) – VHDL Assignment 1

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1. Explain your VHDL code.

In our VHDL code we have 8 .vhd files. There are 4 design files, MUX_Structural.vhd, MUX_Behavioral.vhd, AKroon_BarrelShifter_Struct.vhd, and AKroon_BarrelShifter_Behav.vhd. Each design file has a corresponding testbench, tb_MUX_structural.vhd, tb_MUX_behavioral.vhd, tb_barrel_struct.vhd, tb_barrel_behav.vhd.

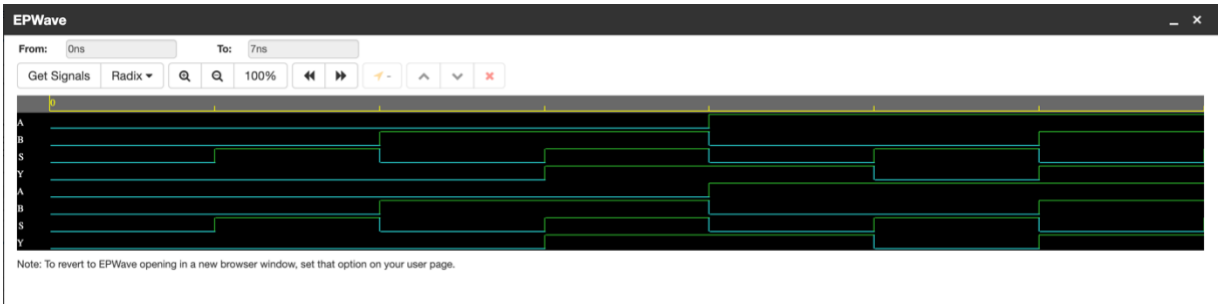
First we wrote the design code for the 2 to 1 MUX. The MUX_Structural.vhd defines the relationship between A,B,S, and Y with 2 ANDs, 1 OR and 1 NOT gate. The MUX_Behavioral.vhd uses a "with -- select" statement to implement the selector function of the multiplexer. The corresponding testbenches for those two design files are nearly identical. The testbenches link the design and test bench files together and go through all the possible input combinations with the three given input variables A,B, and S.

Next, we have the 4 bit barrel shifter. The AKroon_BarrelShifter_Behav.vhd file implements the shift with a "with -- select" statement. The AKroon_BarrelShifter_Struct.vhd file defines 8 multiplexers using the previously designed MUX_Structural.vhd. The inputs of the 8 multiplexers are aligned with the inputs on the diagram given in the assignment. An additional signal must be created to represent the output of the first column of multiplexers/input to the second column of multiplexers. The test benches for the barrel shifters are also nearly identical with only the entity name being different. The testbench defines the component and input signals X_i, Sel_i, and Y_i. Following this, the DUT takes the input signals and transfers them to the corresponding design file. Finally the testbench iterates through the input combinations with two for loops (one nested within the other) to reach all the possible input combinations for both X_i (4 bit) and Sel_i (2 bit).

2. Report the number of pins and logic modules used to fit your designs on the FPGA board.

	2-1 MUX Struct	2-1MUX Behav	4 bit barrel Struct	4 bit barrel Behav
LUTs	1	1	4	4
Total Pins	4	4	10	10

3. Show representative simulation plots of the 2-to-1 MUX circuits for all the possible input values (exhaustive test results). Note that you can simply include snapshots from the waveform that you obtained from EPWave. In order to fully capture all the signals from the waveform, you can adjust the display range using the magnifier icons. Make sure that all signal names and axes are properly visible.



4. Show representative simulation plots of the 4-bit circular shift register circuits for a given input sequence, *e.g.*, “1011” (X = “1011”), for all the possible shift amounts.