

# CSC258 Lab #2 Pre-Lab

## Multiplexers, Design Hierarchy, and HEX Displays

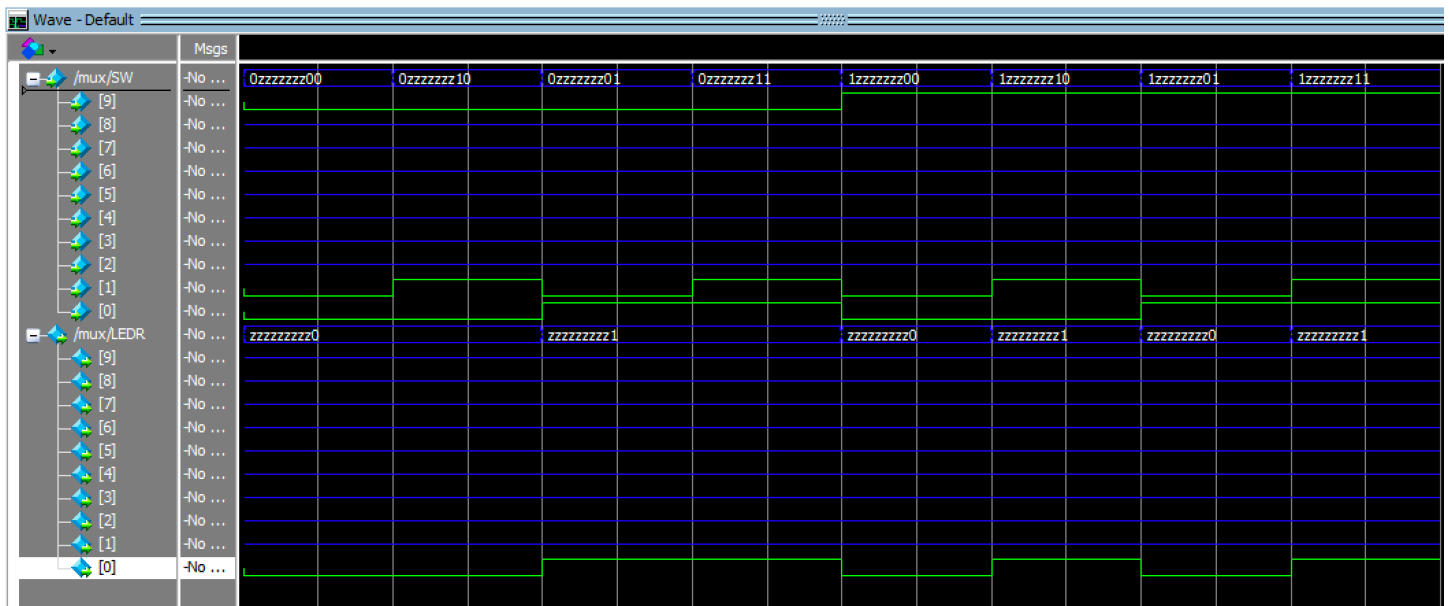
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### Prat I

1.Look at the generated waveform , which is the simulation output, and verify that the provided test-cases work as expected.

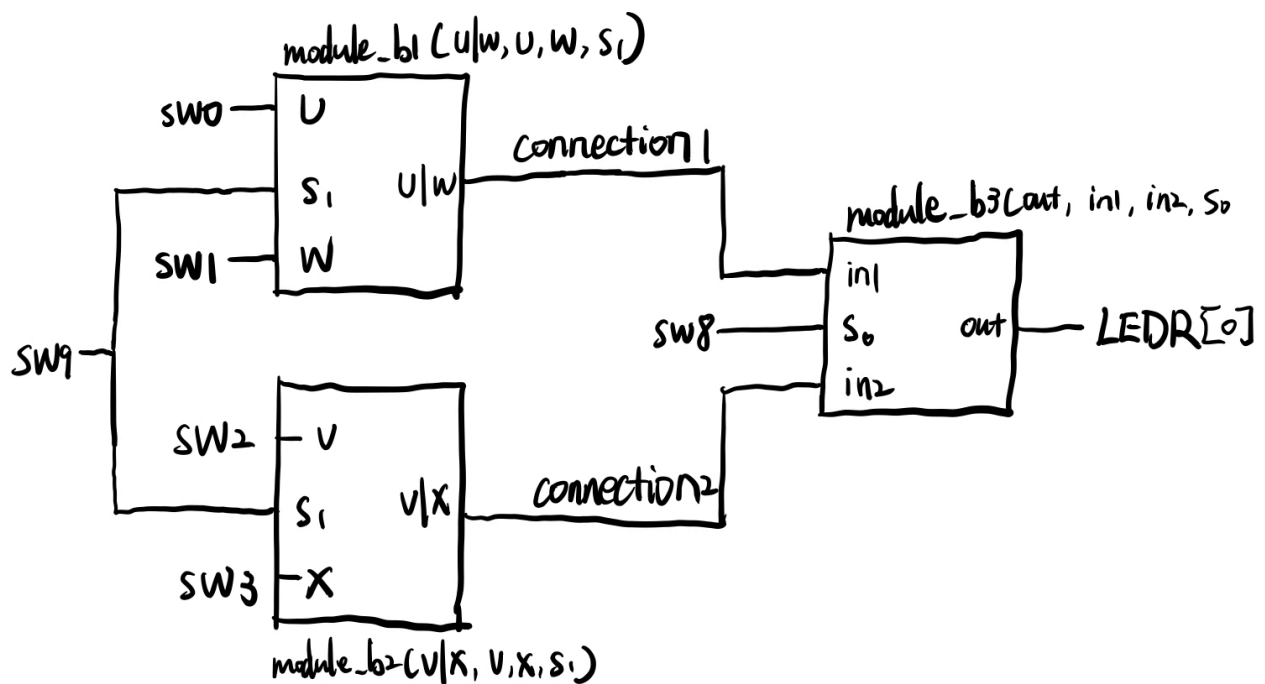
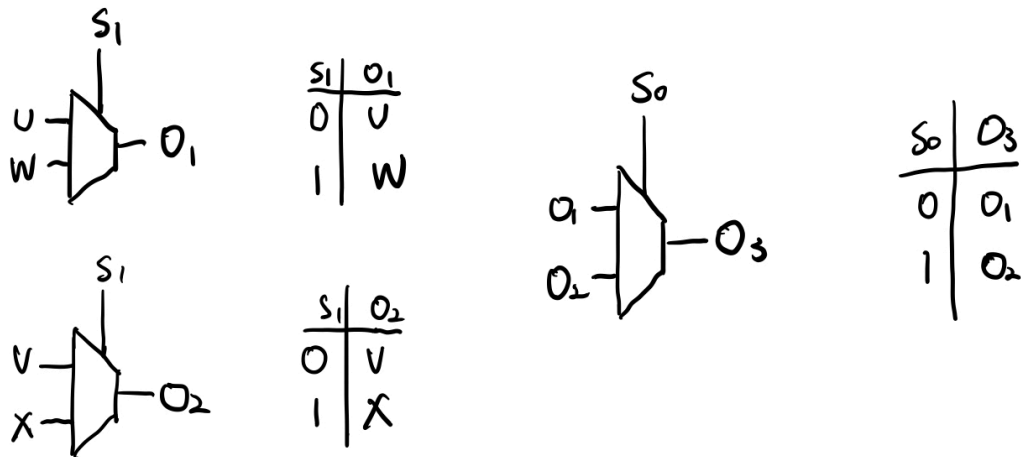


The output is LEDR[0] and the result is as expected. When Sw9 is 0 and Sw0 is 1, what matter Sw1 is, the LEDR[0] is 1. When Sw9 is 1 and Sw0 is 0, if Sw1 is 1, LDER[0] is 1. When three of them are all 1, LEDR[0] is 1.

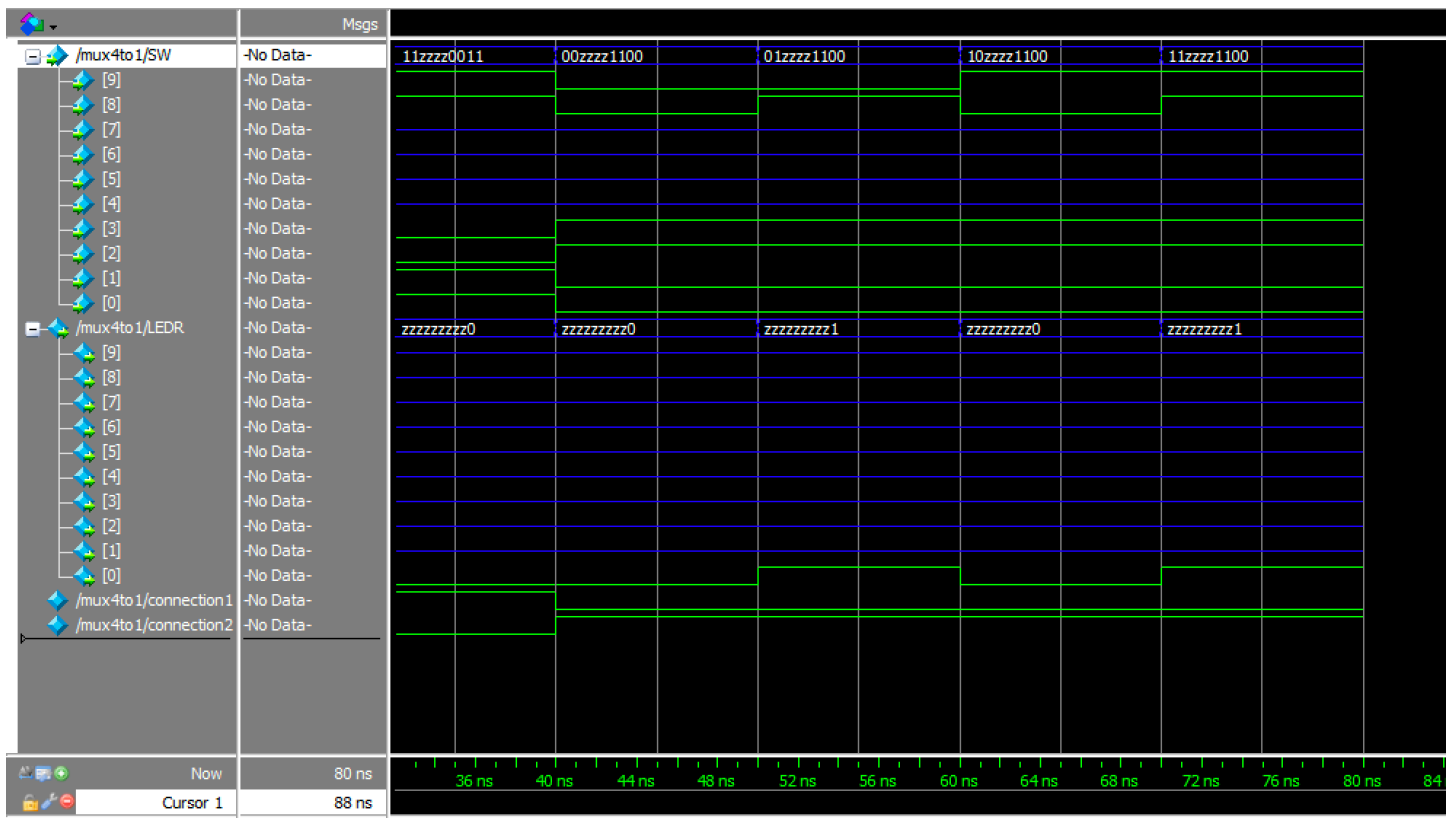
### Part II

1. if the truth table in Table 2 was given in full, how many rows would it have?  
there are 6 inputs in the figure3, therefore, it should have  $2^6=64$  rows.

2. Draw a schematic showing how you will connect the mux2to1 modules to build the 4-to-1 multiplex



3. Create a new Quartus Prime project for your circuit and write the Verilog code  
the Verilog code is in mux4to1.v
4. Simulate your circuit with ModelSim for different values of  $s$ ,  $u$ ,  $v$ ,  $w$  and  $x$
- $SW[0]$  -  $u$      $SW[1]$  -  $w$      $SW[2]$  -  $v$      $SW[3]$  -  $x$      $SW[9]$  -  $s1$      $SW[8]$  -  $s0$



### Part III

1. Write the expressions for seven Boolean functions

HEX[6]

	$\bar{C}_3\bar{C}_2$	$\bar{C}_3C_2$	$C_3\bar{C}_2$	$C_3C_2$
$\bar{C}_3\bar{C}_2$	1	1		
$\bar{C}_3C_2$			1	
$C_3\bar{C}_2$	1			
$C_3C_2$				

$$HEX[6] = \bar{C}_3\bar{C}_2\bar{C}_1 + \bar{C}_3C_2C_1C_0 + C_3C_2\bar{C}_1\bar{C}_0$$

# HEX[0]

	$\bar{C}_1\bar{C}_0$	$\bar{C}_1C_0$	$C_1\bar{C}_0$	$C_1C_0$
$\bar{C}_3\bar{C}_2$		1		
$\bar{C}_3C_2$	1			
$C_3\bar{C}_2$		1		
$C_3C_2$			1	

$$\text{HEX}[0] = \bar{C}_3\bar{C}_2\bar{C}_1\bar{C}_0 + \bar{C}_3\bar{C}_2\bar{C}_1C_0 + \bar{C}_3\bar{C}_2C_1\bar{C}_0 + \bar{C}_3\bar{C}_2C_1C_0 + C_3\bar{C}_2\bar{C}_1\bar{C}_0 + C_3\bar{C}_2\bar{C}_1C_0 + C_3\bar{C}_2C_1\bar{C}_0 + C_3\bar{C}_2C_1C_0$$

# HEX[2]

	$\bar{C}_1\bar{C}_0$	$\bar{C}_1C_0$	$C_1\bar{C}_0$	$C_1C_0$
$\bar{C}_3\bar{C}_2$				1
$\bar{C}_3C_2$				
$C_3\bar{C}_2$	1			1
$C_3C_2$				

$$\text{HEX}[2] = \bar{C}_3\bar{C}_2C_1\bar{C}_0 + \bar{C}_3\bar{C}_2C_1C_0 + C_3\bar{C}_2\bar{C}_1\bar{C}_0 + C_3\bar{C}_2\bar{C}_1C_0$$

# HEX[4]

	$\bar{C}_1\bar{C}_0$	$\bar{C}_1C_0$	$C_1\bar{C}_0$	$C_1C_0$
$\bar{C}_3\bar{C}_2$		1	1	
$\bar{C}_3C_2$	1	1	1	
$C_3\bar{C}_2$				
$C_3C_2$		1		

$$\text{HEX}[4] = \bar{C}_3\bar{C}_2\bar{C}_1 + \bar{C}_3\bar{C}_2C_0 + \bar{C}_3C_2\bar{C}_1 + \bar{C}_3C_2C_0 + C_3\bar{C}_2\bar{C}_1 + C_3\bar{C}_2C_0 + C_3C_2\bar{C}_1 + C_3C_2C_0$$

# HEX[1]

	$\bar{C}_1\bar{C}_0$	$\bar{C}_1C_0$	$C_1\bar{C}_0$	$C_1C_0$
$\bar{C}_3\bar{C}_2$				
$\bar{C}_3C_2$		1		1
$C_3\bar{C}_2$	1			1
$C_3C_2$			1	1

$$\text{HEX}[1] = C_3\bar{C}_2\bar{C}_1\bar{C}_0 + C_3\bar{C}_2\bar{C}_1C_0 + C_3\bar{C}_2C_1\bar{C}_0 + C_3\bar{C}_2C_1C_0 + C_3C_2\bar{C}_1\bar{C}_0 + C_3C_2\bar{C}_1C_0 + C_3C_2C_1\bar{C}_0 + C_3C_2C_1C_0$$

# HEX[3]

	$\bar{C}_1\bar{C}_0$	$\bar{C}_1C_0$	$C_1\bar{C}_0$	$C_1C_0$
$\bar{C}_3\bar{C}_2$		1		
$\bar{C}_3C_2$	1			1
$C_3\bar{C}_2$				1
$C_3C_2$		1		

$$\text{HEX}[3] = \bar{C}_3\bar{C}_2\bar{C}_1\bar{C}_0 + \bar{C}_3\bar{C}_2\bar{C}_1C_0 + \bar{C}_3\bar{C}_2C_1\bar{C}_0 + \bar{C}_3\bar{C}_2C_1C_0 + C_3\bar{C}_2\bar{C}_1\bar{C}_0 + C_3\bar{C}_2\bar{C}_1C_0 + C_3\bar{C}_2C_1\bar{C}_0 + C_3\bar{C}_2C_1C_0$$

# HEX[5]

	$\bar{C}_1\bar{C}_0$	$\bar{C}_1C_0$	$C_1\bar{C}_0$	$C_1C_0$
$\bar{C}_3\bar{C}_2$		1	1	
$\bar{C}_3C_2$	1	1	1	
$C_3\bar{C}_2$				
$C_3C_2$		1		

$$\text{HEX}[5] = C_3\bar{C}_2\bar{C}_1\bar{C}_0 + C_3\bar{C}_2\bar{C}_1C_0 + C_3\bar{C}_2C_1\bar{C}_0 + C_3\bar{C}_2C_1C_0 + C_3C_2\bar{C}_1\bar{C}_0 + C_3C_2\bar{C}_1C_0 + C_3C_2C_1\bar{C}_0 + C_3C_2C_1C_0$$

- Write a Verilog module for the 7-segment decoder  
view the file seven\_seg\_decoder.v
- simulate your 7-segment decoder module with ModelSim  
BA3145 for me, see the figure

