CSC258 Lab #4 Pre-Lab

Latches, Flip-flops, and Registers

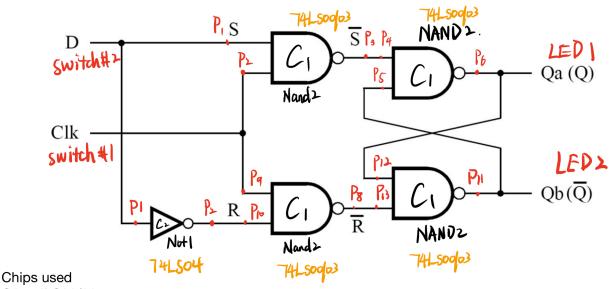
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Prat I

1. draw a schematic of the gated D latch using interconnected 7400-series chips



C1 -74LS00/03 C2 -74LS04

Connected to all chips

PIN#7 - Gnd PIN#14 -Vcc

4. Are there any input combinations of Clk and D that should NOT be the first you test? do not start with the case Clk=0,D=0 or Clk=0, D=1. those two cases will cause two outputs indeterminate.

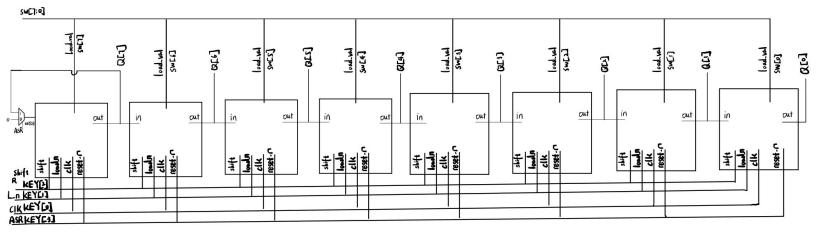
Prat II

- 1. Create a Verilog module for the simple ALU with register see the ALU.v
- 2. Create a Verilog module for the simple ALU with register see the ALU.do and the following figure.

∓ -	-No Data-	1z011z	1010		1z100z1	010		0z100:	1010	1z000z0	001		1z 10 1z0	001		1z110z	0010			1z111z1	10
≖ -	-No Data-	zzz1		zzz0	zzz1		zzz0	zzz1				zzz0	zzz1		zzz0	zzz1		zzz0	7	zzz1	
≖ -/ALU/LEDR	-No Data-	zz111	0101		zz00000	001				zz00000	010		zz00000	100		zz0000	0001		- 2	zz00001	10
ALU/HEX0 ■-	-No Data-	00010	00							1111001						010010	o .			0001000	
≖ -∕• /ALU/HEX4	-No Data-	00011	10		0010010			10000	00				0100100			001100	1			1111001	
ALU/HEX5 ■-	-No Data-	10000	00		0001110			10000	00												
→ /ALU/ALUout	-No Data-	11110	101		0000000	1				0000001	.0		0000010	0		000000	01		(0	0000101	0
≖ – <pre>/ALU/Registerout</pre>	-No Data-	00001	111		1111010	1		00000	000				0000001	0		000001	00		- (000000	1
≖ – ♦ /ALU/temp4	-No Data-				1010010	1		10100	000												
∓ - ∜ /ALU/tempa	-No Data-	1111			0000															0000	
∓ - ∜ /ALU/tempb	-No Data-	0101			0001					0010			0100			0001				1010	
∓ – /ALU/case0	-No Data-	00001	011							0000001	.0										
∓ - ∜ /ALU/case1	-No Data-	00001	111																		
≖ – ∜ /ALU/case5	-No Data-												0000010	0							
≖ - <pre>/ALU/case6</pre>	-No Data-															000000	01				
≖ - ♦ /ALU/case7	-No Data-																			0000101	0

Part III

- 1. What is the behaviour of the 8-bit shift register shown in Figure 6 when Load n = 1 and ShiftRight = 0? The value of the 8-bits register is not going to change, because the two 2-to-1multiplexer ShiftRight and load_n select the output Q of the flip flop to be the input D, so the value of the register is unchanged.
- 2. Draw a schematic for the 8-bit shift register shown in Figure 6 including the necessary connections.



- 3. Starting with the code in Figure 2 for a positive edge-triggered D flip-flop. see the Shifter.v file
- 4. Write a Verilog module for the shift register that instantiates eight instances of one-bit shift register that you created in previous step. see the Shifter.v and Shitfer.do
- 5. Compile your Verilog code and simulate the design with ModelSim.

