CSC258 Lab #4 Pre-Lab

Latches, Flip-flops, and Registers

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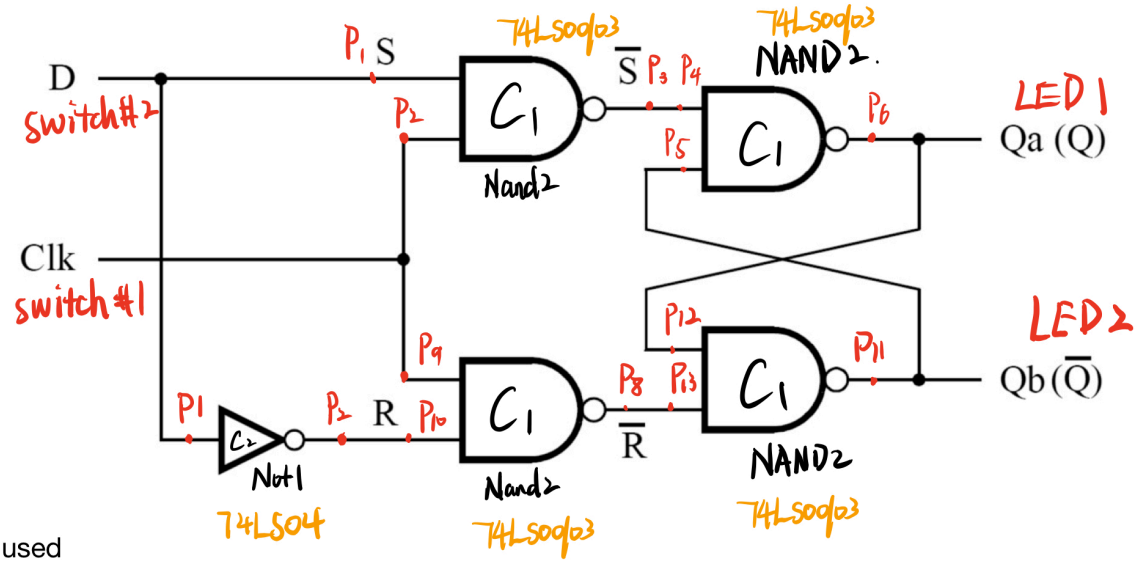
Prat I

1. draw a schematic of the gated D latch using interconnected 7400-series chips



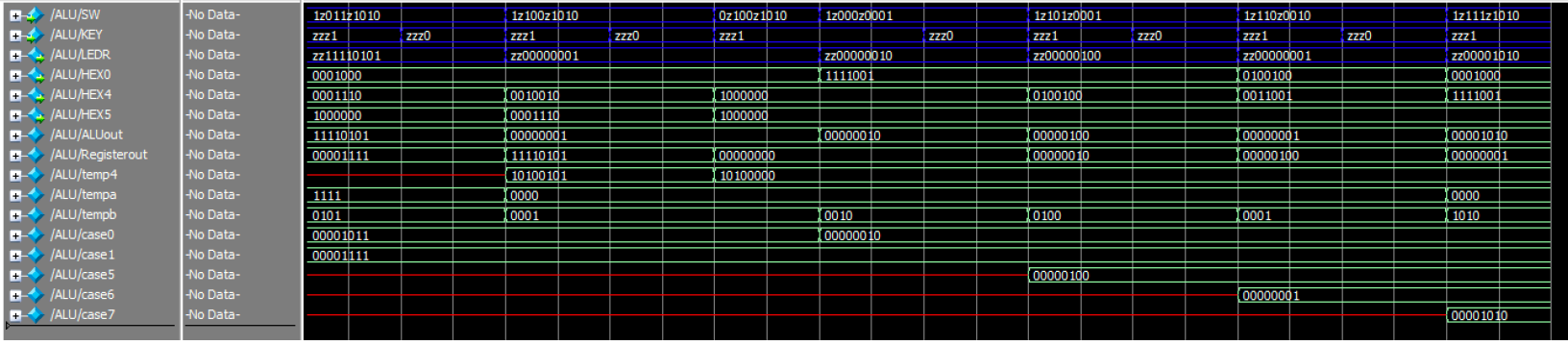
Chips used
C1 -74LS00/03
C2 -74LS04

Connected to all chips
PIN#7 - Gnd
PIN#14 -Vcc

4. Are there any input combinations of Clk and D that should NOT be the first you test?
   do not start with the case Clk=0,D=0 or Clk=0, D=1.
   those two cases will cause two outputs indeterminate.

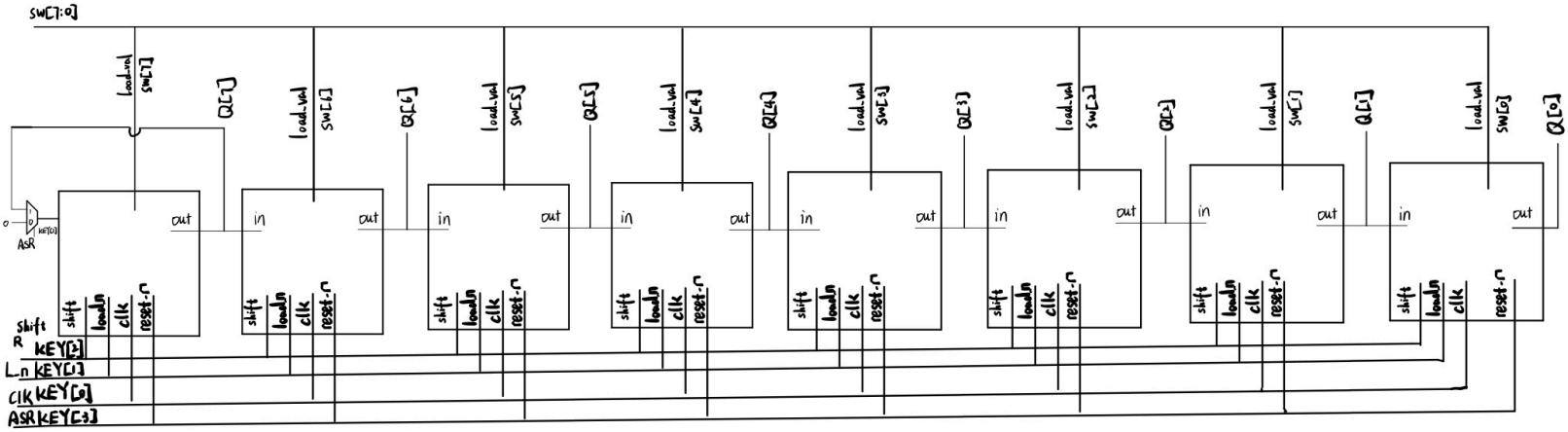
Prat II

1. Create a Verilog module for the simple ALU with register
   see the ALU.v
2. Create a Verilog module for the simple ALU with register
   see the ALU.do and the following figure.



Part III

1. What is the behaviour of the 8-bit shift register shown in Figure 6 when Load n = 1 and ShiftRight = 0?
   The value of the 8-bits register is not going to change, because the two 2-to-1multiplexer ShiftRight and load_n select the output Q of the flip flop to be the input D, so the value of the register is unchanged.
2. Draw a schematic for the 8-bit shift register shown in Figure 6 including the necessary connections.



3. Starting with the code in Figure 2 for a positive edge-triggered D flip-flop.
   see the Shifter.v file
4. Write a Verilog module for the shift register that instantiates eight instances of one-bit shift register that you created in previous step.
   see the Shifter.v and Shitfer.do
5. Compile your Verilog code and simulate the design with ModelSim.