CSC258 Lab #6 Pre-Lab

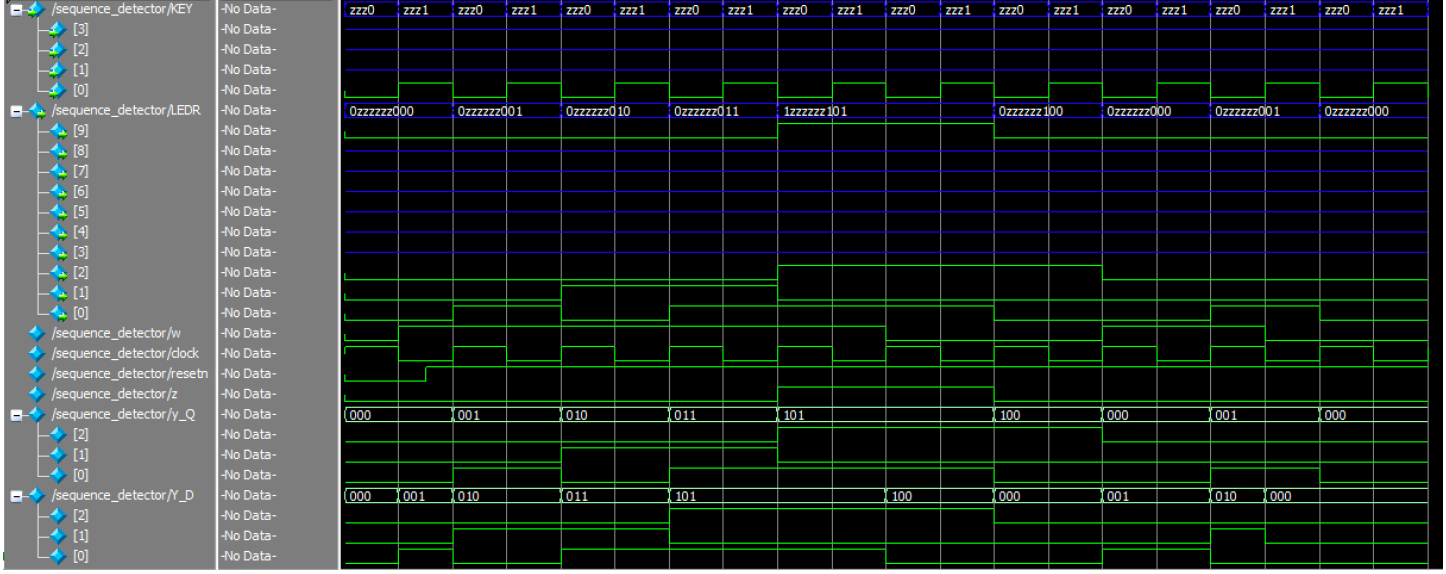
Finite State Machines
Last name: Fan
First name: Yuchen
Student number: 1003800265

Prat I

1. Complete sequence_detector.v
   see the file sequence_detector.v
2. is the resetn signal is an synchronous or asynchronous reset?
   reset is synchronous and active low.
   if I want to reset the state, I need to make sure the clock is on when the reset is enabled.
3. Complete the state table

Present state	Input	Next state	Output
A:000	0	A:000	0
A:000	1	B:001	0
B:001	0	A:000	0
B:001	1	C:010	0
C:010	0	E:100	0
C:010	1	D:011	0
D:011	0	E:110	0
D:011	1	F:101	0
E:100	0	A:000	0
E:100	1	G:110	0
F:101	0	E:100	1
F:101	1	F:101	1
G:110	0	A:000	1
G:110	1	C:010	1

4. Simulate your circuit using ModelSim
   see the file sequence_detector.do

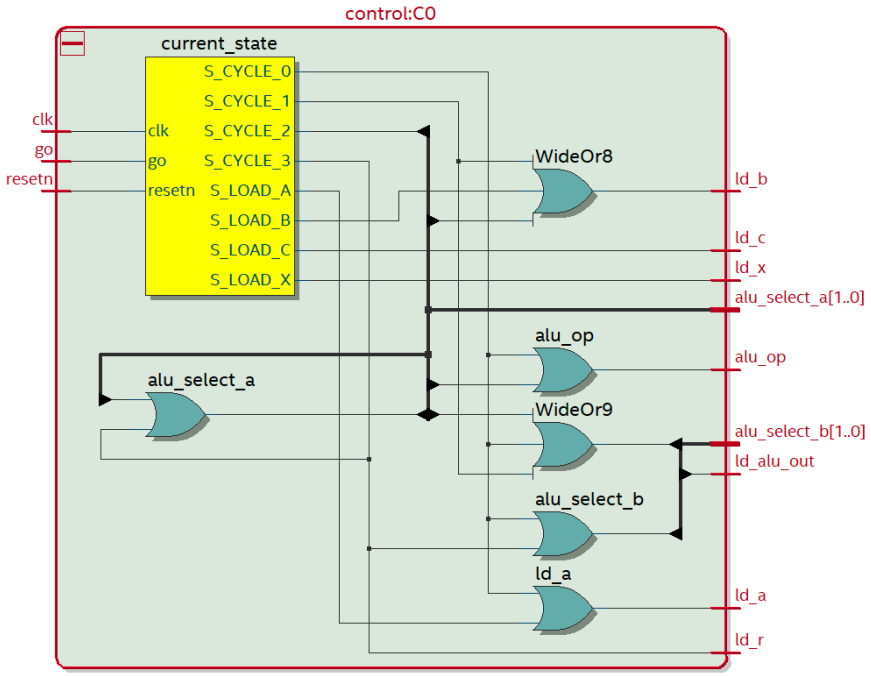


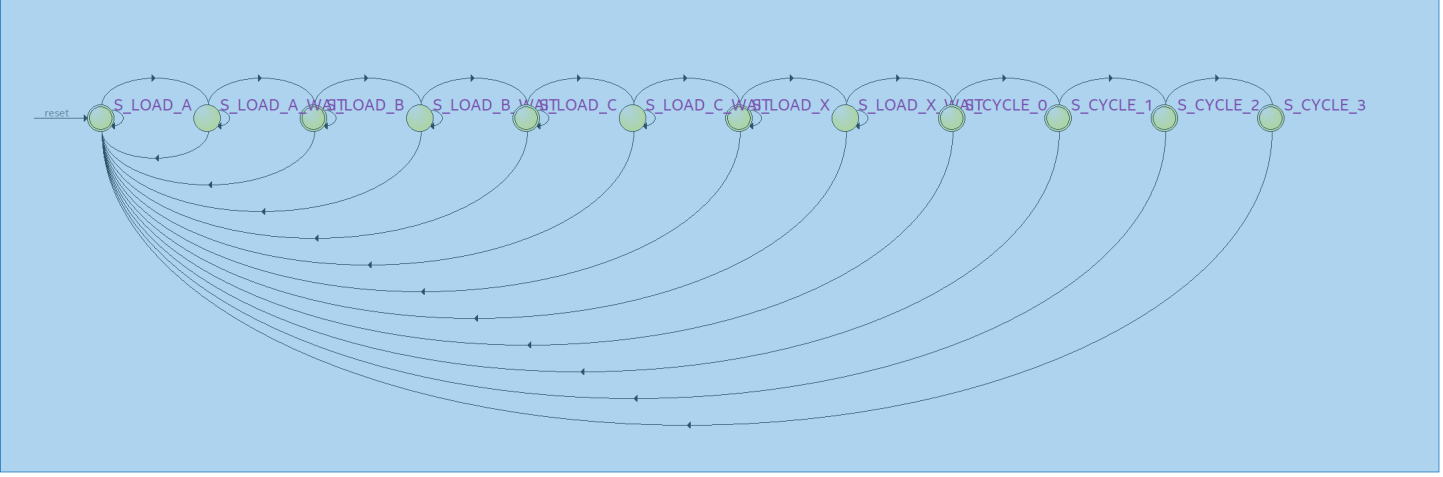
Prat II

1. understand the circuitry
2. draw a table that shows the state of the Registers and control signals for each cycle of your computation

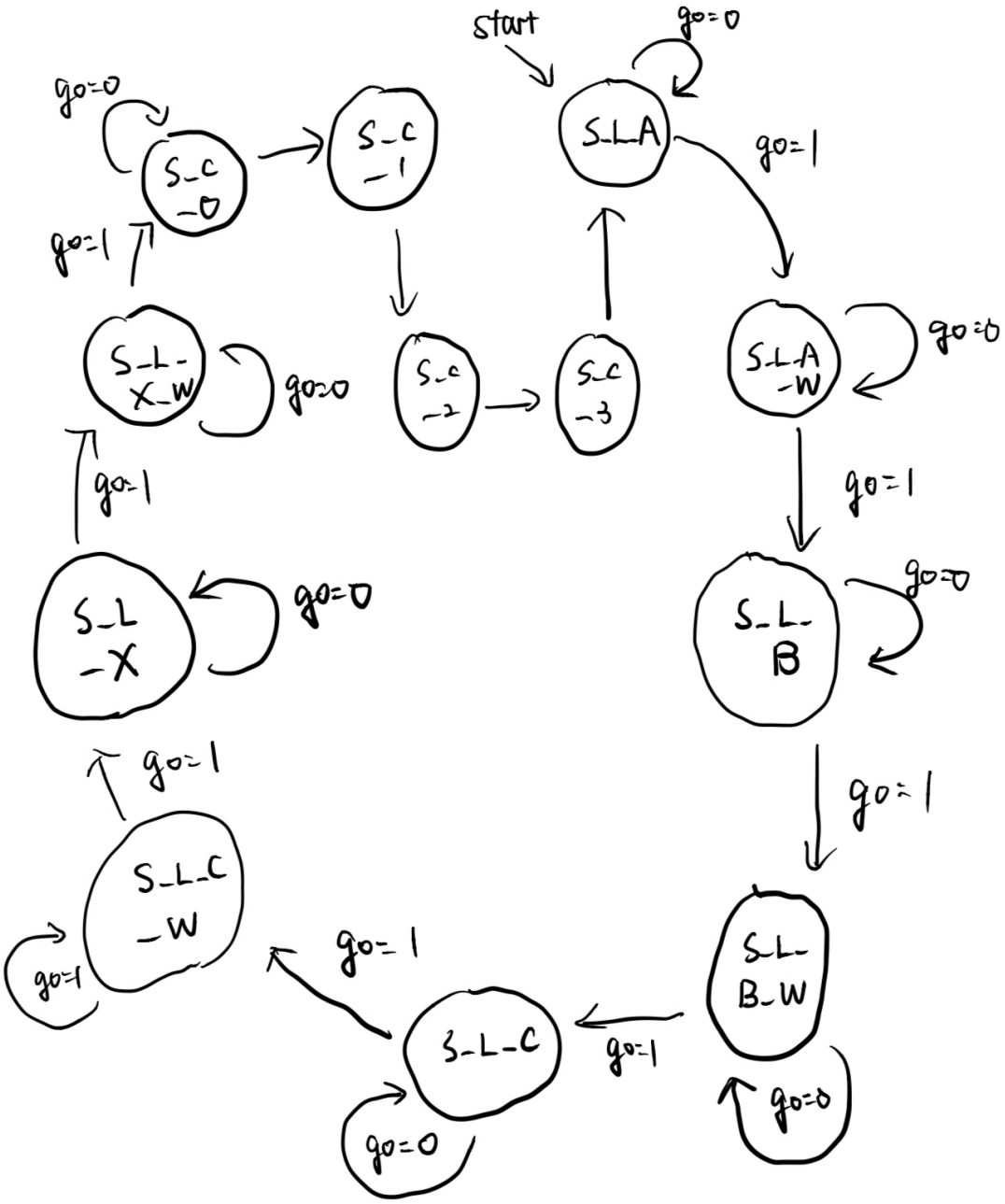
Cycle	Computation	ld_a	ld_b	ld_alu_out	ld_r	alu_select_a	alu_select_b	A	B	R
0	A * X	1	0	1	0	2'b00	2'b11	A * X	B	
1	AX + B	0	1	1	0	2'b00	2'b01	A * X	AX + B	
2	X(AX+B)	0	1	1	0	2'b11	2'b01	A * X	X(AX+B)	
3	X(AX+B)+C	0	0	0	1	2'b01	2'b10	A * X	X(AX+B)	X(AX+B)+C

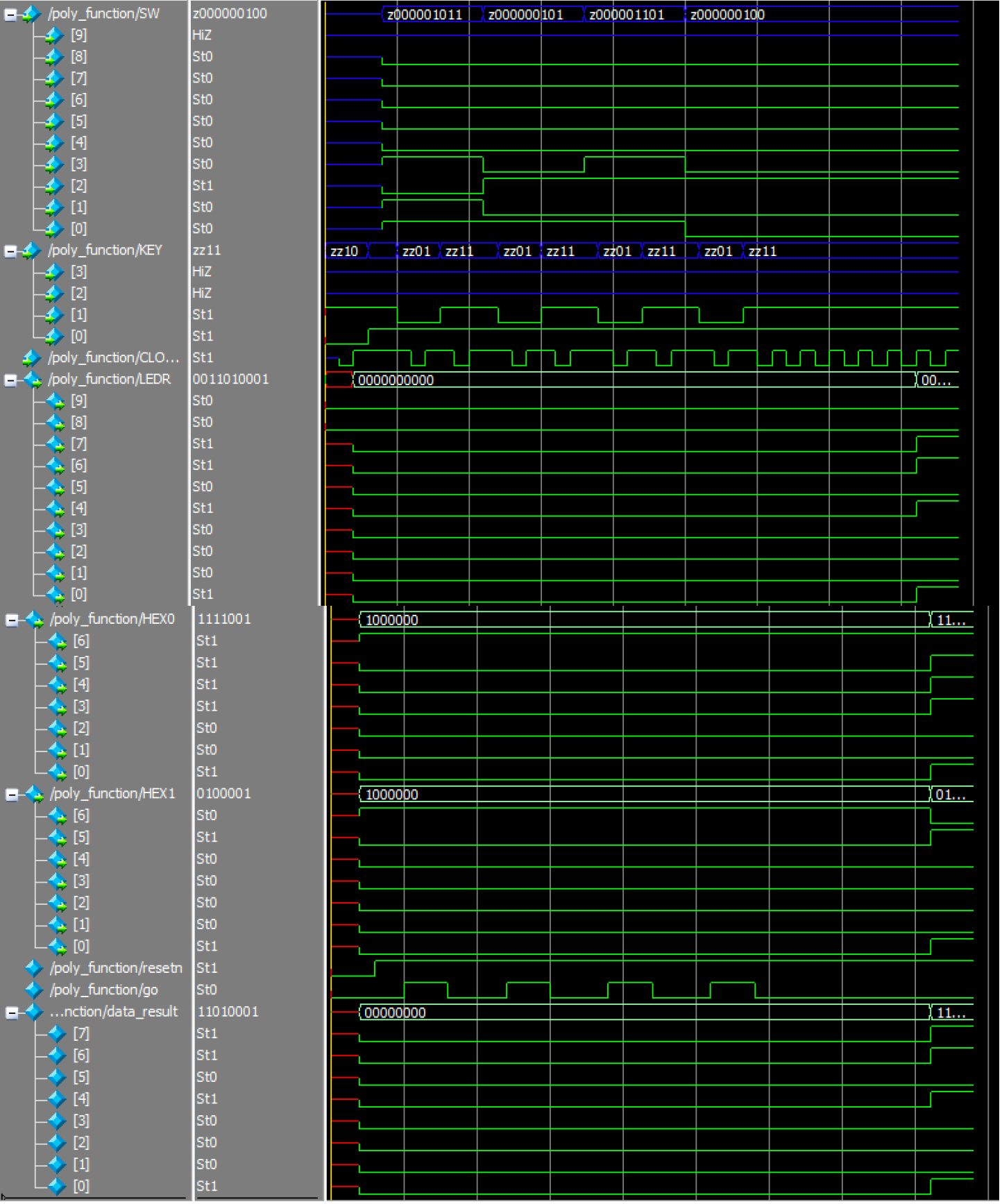
3. Draw a state diagram for your controller
   see the next page
4. Modify the controller part
   see the file poly_function.v
5. examine the circuit





6. Simulate your circuit with ModelSim

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[9]
HiZ
[8]
St0
[7]
St0
[6]
St0
[5]
St0
[4]
St0
[3]
St0
[2]
St1
[1]
St0
[0]
St0
/poly_function/KEY
zz11
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HiZ
[2]
HiZ
[1]
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[0]
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St1
/poly_function/LEDR
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[8]
St0
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[5]
St0
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[3]
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[1]
St0
[0]
St1
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z000000101
z000001101
z000000100
zz10
zz01
zz11
zz01
zz11
zz01
zz11
zz01
zz11
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00...

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[3]
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[2]
St0
[1]
St0
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St1
/poly_function/resetn
St1
/poly_function/go
St0
...nction/data_result
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01...
00000000
11...