CSC258 Lab #5 Pre-Lab

Clocks and Counters

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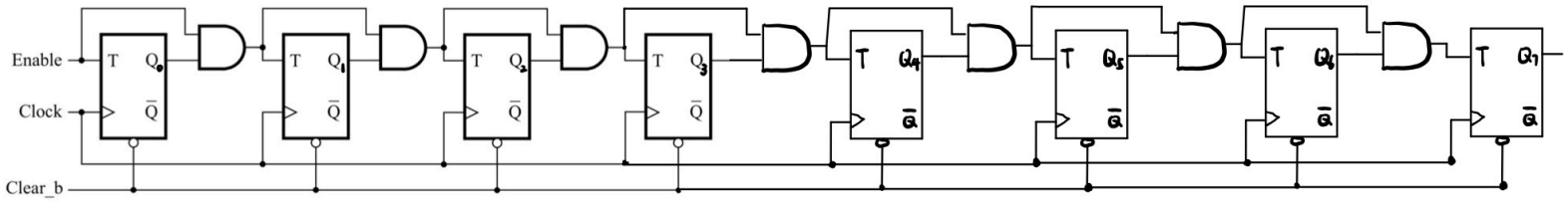
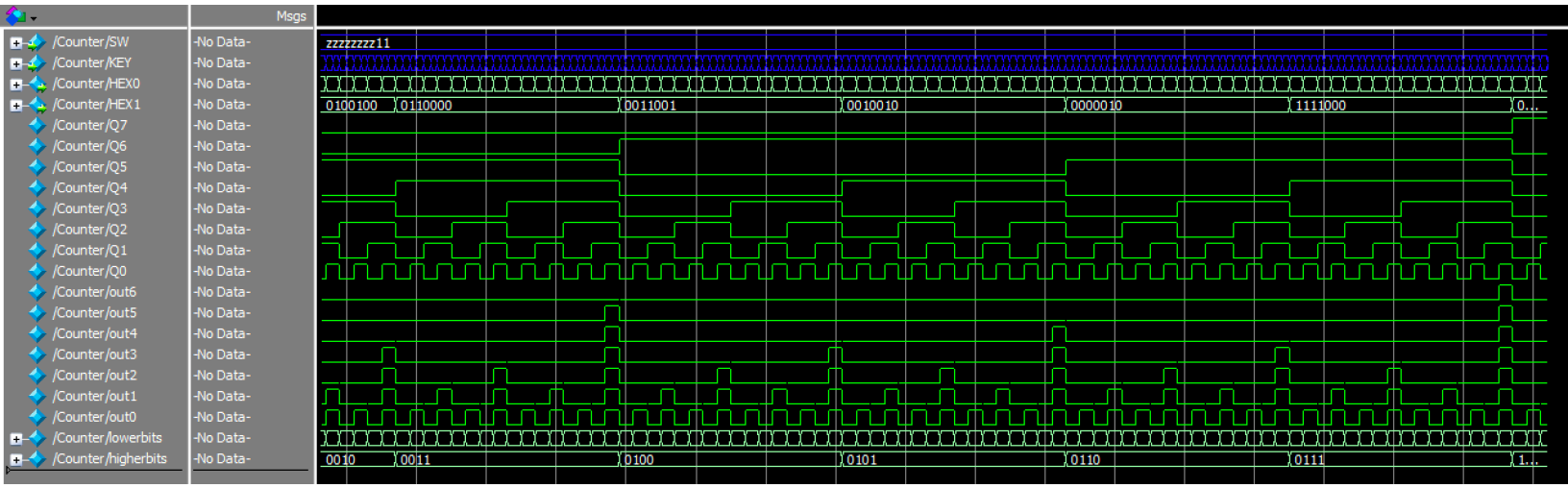
Prat I

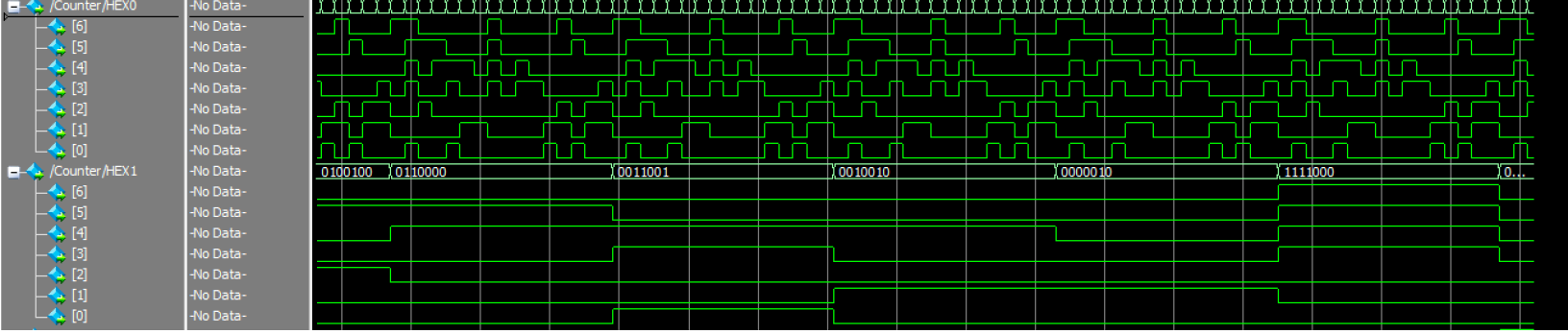
1. Draw the schematic for an 8-bit counter



2. Annotate all Q outputs of your schematic with the bit of the counter (Q7Q6Q5Q4Q3Q2Q1Q0)
   annotate in the above figure
3. Write the Verilog corresponding to your schematic.
   see the Counter.v file
4. Simulate your circuit in ModelSim to verify its correctness.



5. Simulate your circuit to ensure that you have done this correctly



6. Create a new Quartus Prime project
   A. What percentage of FPGA logic resources are used to implement your circuit?

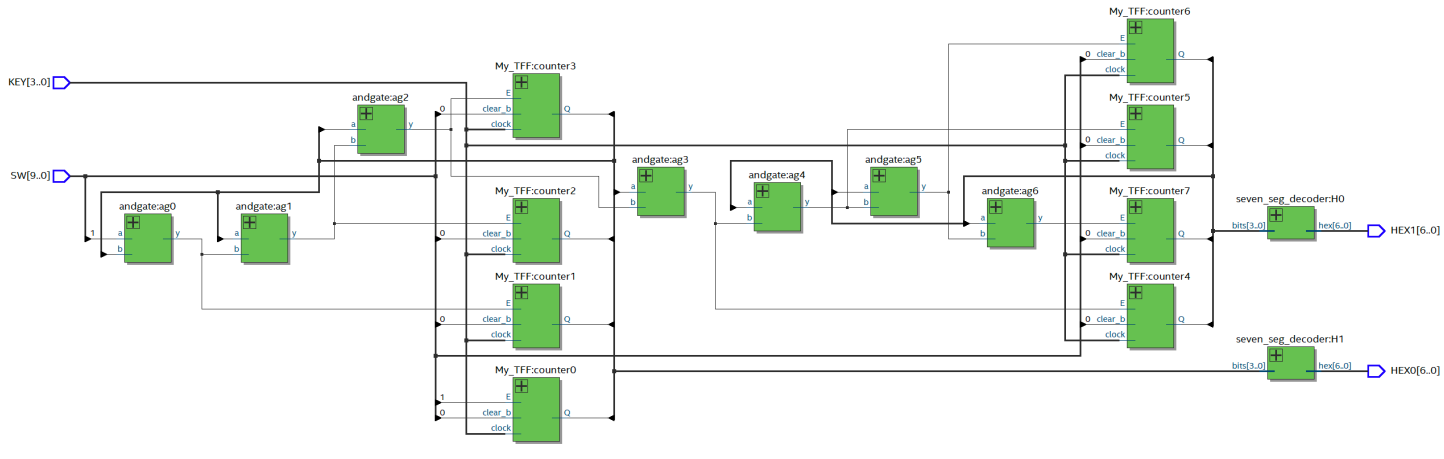
Logic utilization (in ALMs)	13 / 32,070 (< 1 %)
Total registers	8

   B. What is the maximum clock frequency, F_{max}, at which your circuit can be operated?

Slow 1100mV 85C Model

	Fmax	Restricted Fmax	Clock Name	Note
1	643.09 MHz	621.89 MHz	KEY[0]	limit due to low minimu...e width violation (tcl)

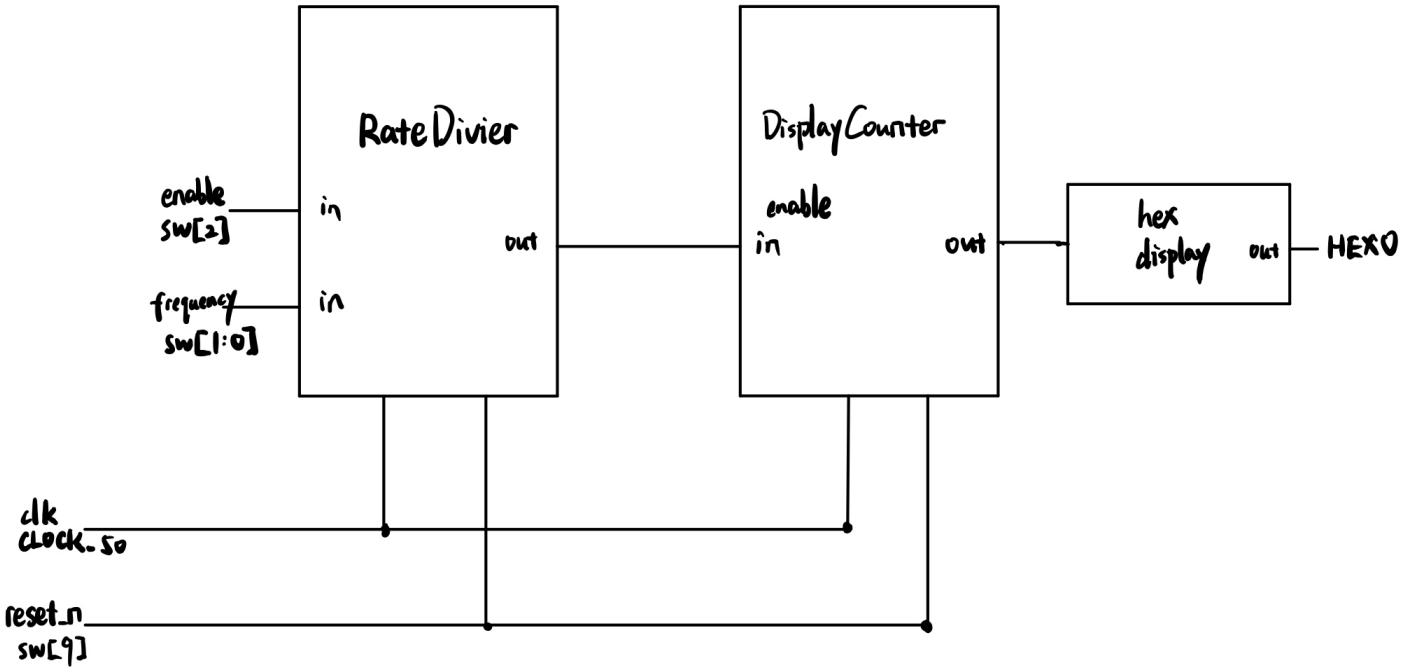
7. Use the Quartus Prime RTL Viewer to see how the Quartus Prime software synthesized your circuit.
   there are two more HEX blocks.



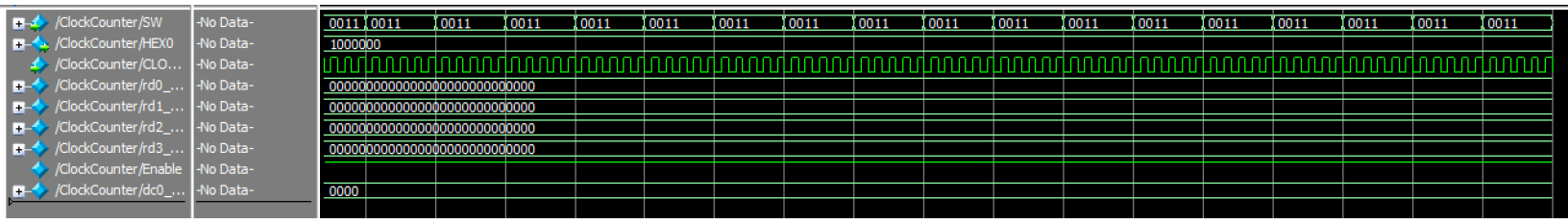
Prat II

A. The check for the maximum value is not necessary in the example above. Why?
   when 4'b1111 + 1'b1, it will be 5'b10000, but there is only 4 bits, therefore, the value will become 4'b0000 which is 0.
B. If you wanted this 4-bit counter to count from 0-9, what would you change?
   if (q == 4'b1111) should change to if (q == 4'b1001)
C. At this speed, what do you expect to see on the display?
   I cannot see the number clearly.

D. How large a counter is required to count 50 million clock cycles?
combine two counters to one counter
E. How many bits would you need to represent such a value?
28bits
1. Draw a schematic of the circuit you wish to build.



2. Write a Verilog module that realizes the behaviour described in your schematic.
see the ClockCounter.v file
3. Simulate your circuit with ModelSim for a variety of input settings

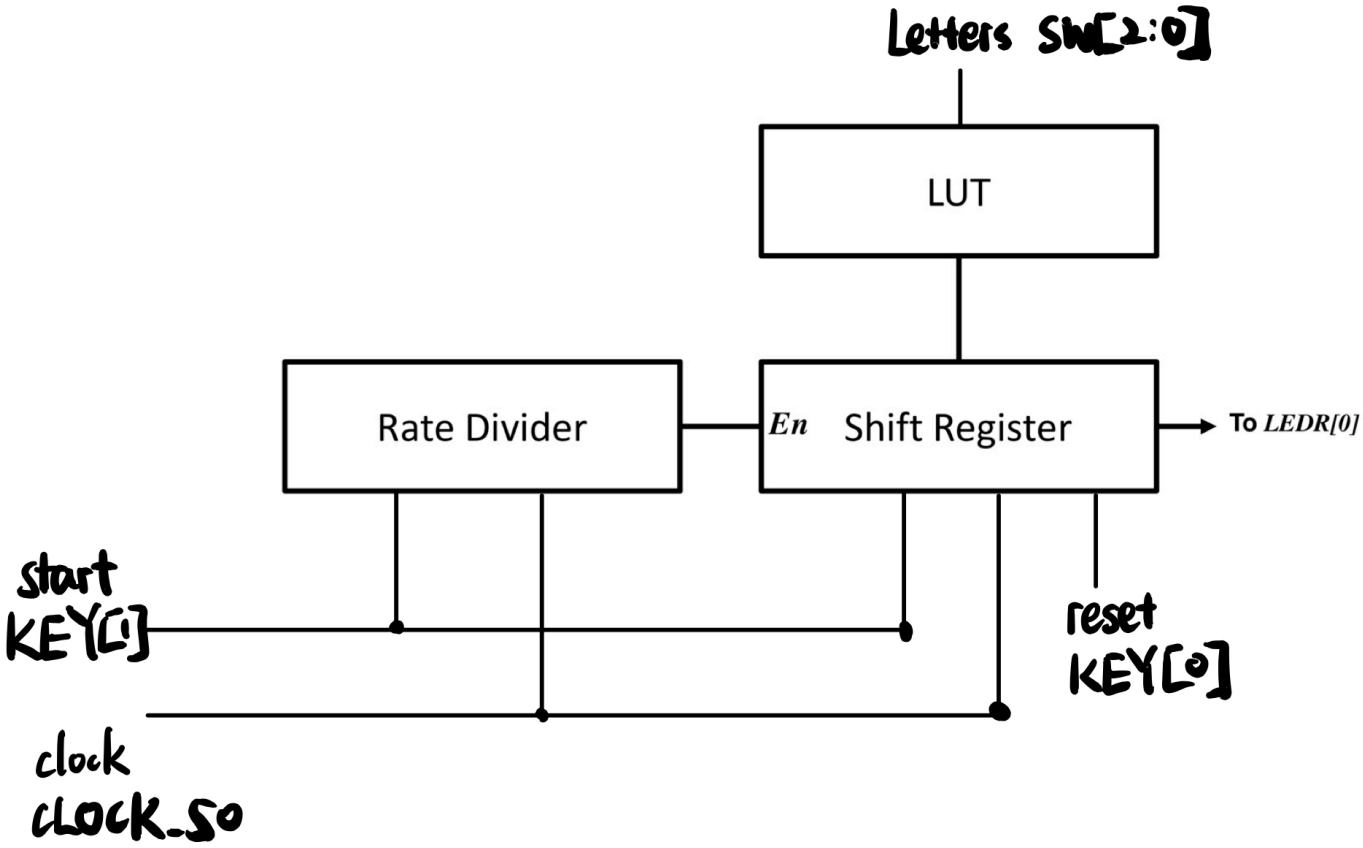


Prat III

1. Morse Pattern Representation with fixed bit-bit-width

Letter	Morse Code	Pattern Representation (pattern length is 14 bits)
S	• • •	10101000000000
T	—	11100000000000
U	• • —	10101110000000
V	• • • —	10101011100000
W	• — —	10111011100000
X	— • • —	111010101110
Y	— • — —	11101011101110
Z	— — • •	11101110101000

2. Design your circuit by first drawing a schematic of the circuit.



3. Write a Verilog module that realizes the behaviour described in your schematic
   see the MorseCoder.v file