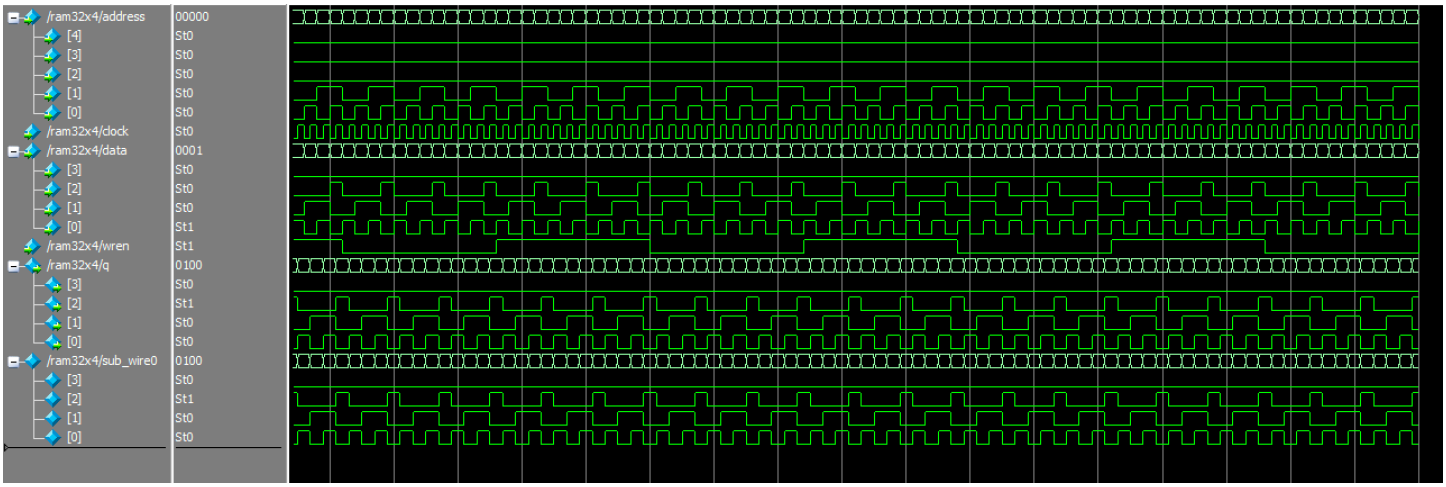
CSC258 Lab #7 Pre-Lab

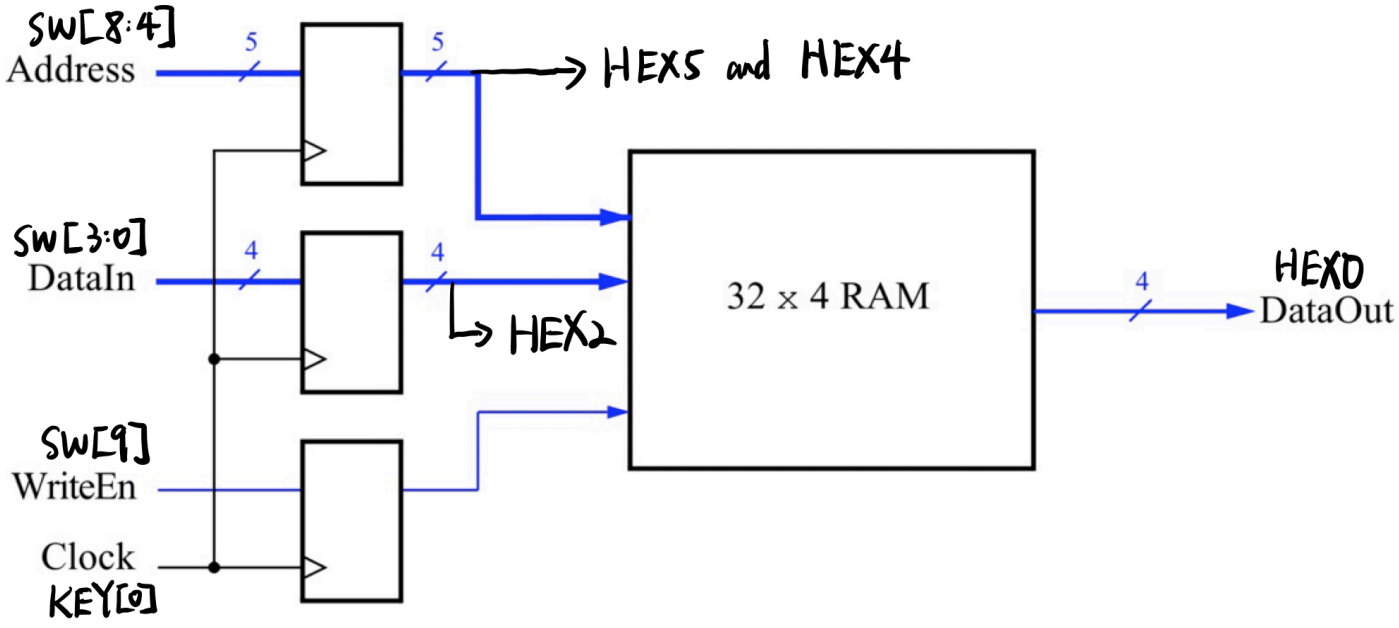
Memory and VGA Display
Last name: Fan
First name: Yuchen
Student number: 1003800265

Prat I

1. Create memory module
   see the file ram32x4.v
2. Simulate the new created Verilog file

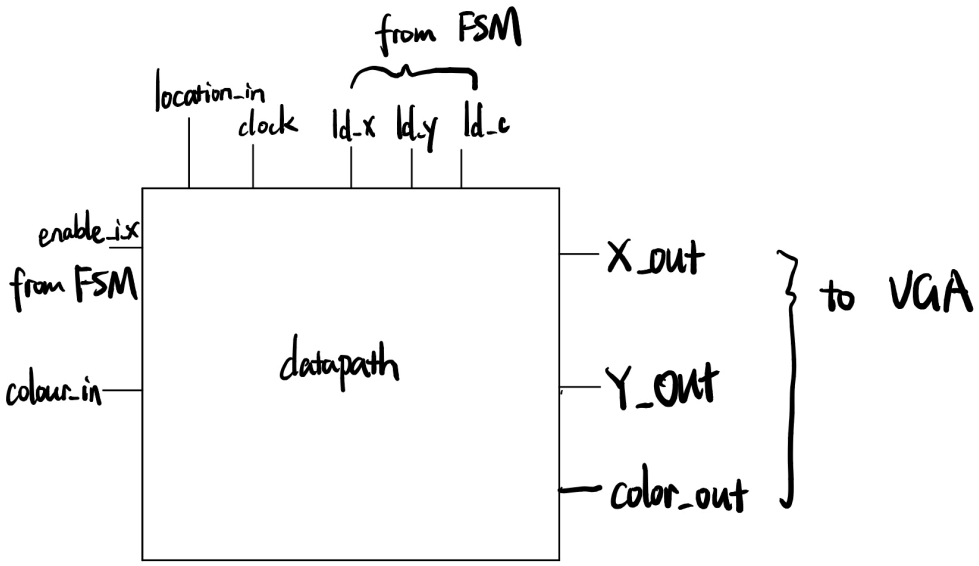


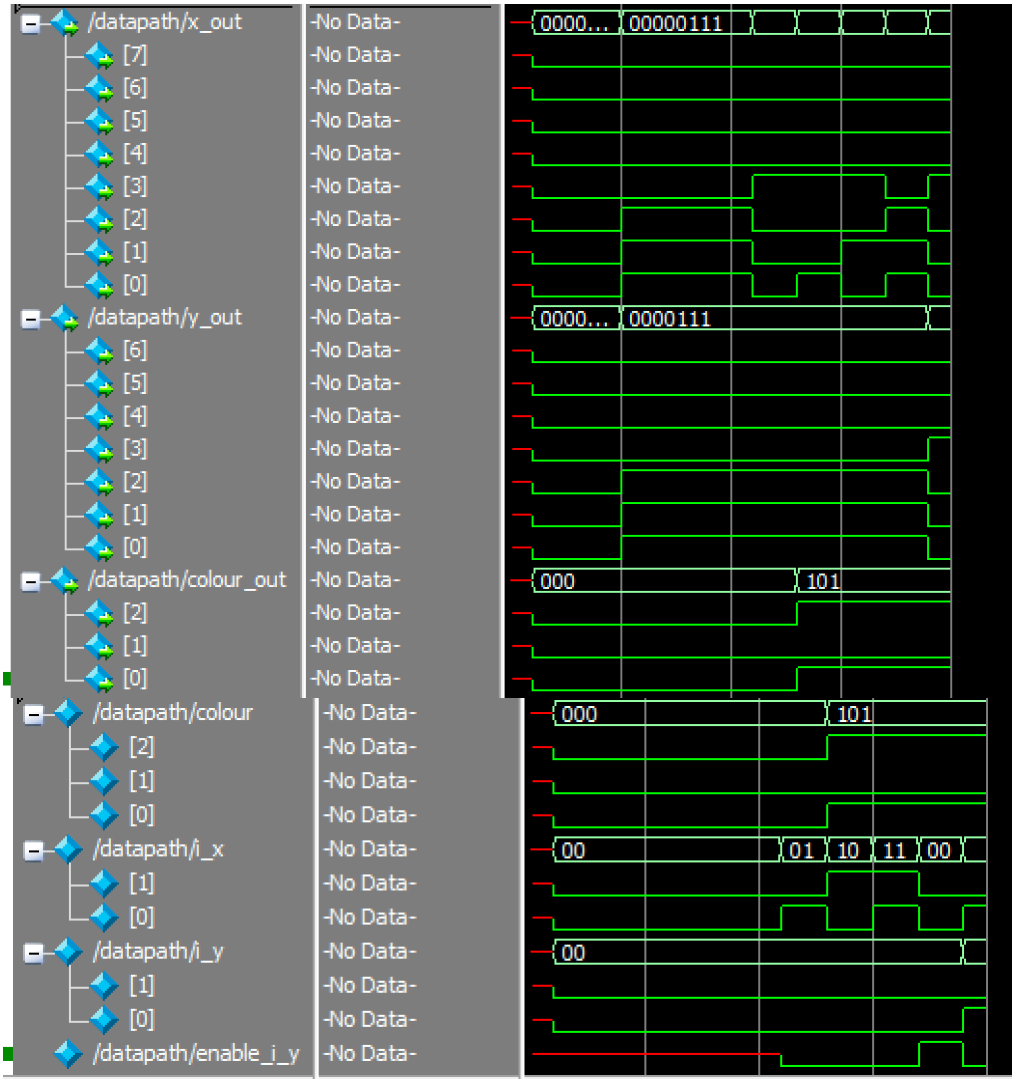
3. Instantiate the ram32x4 module into a top-level Verilog module
   see the file RAM.v
4. Draw a schematic describing the circuit



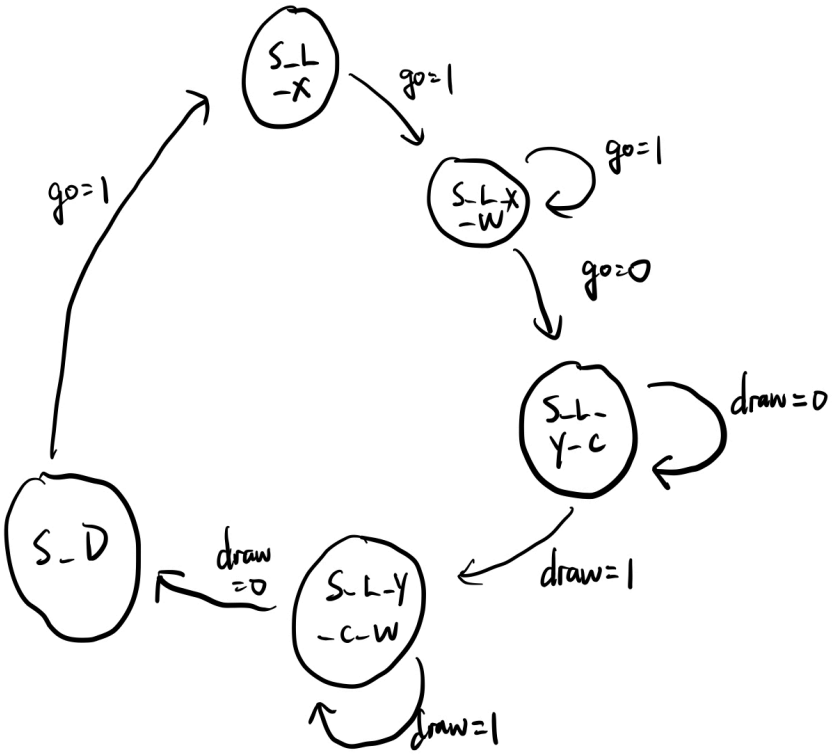
Part II

1. Design and simulate a data_path
   see the file datapath.v

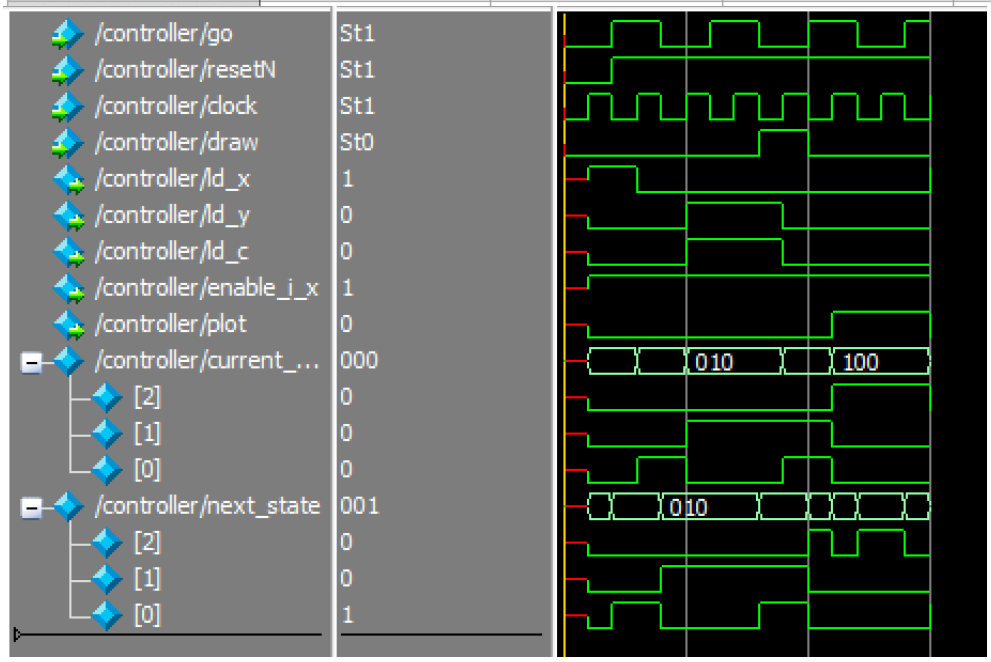




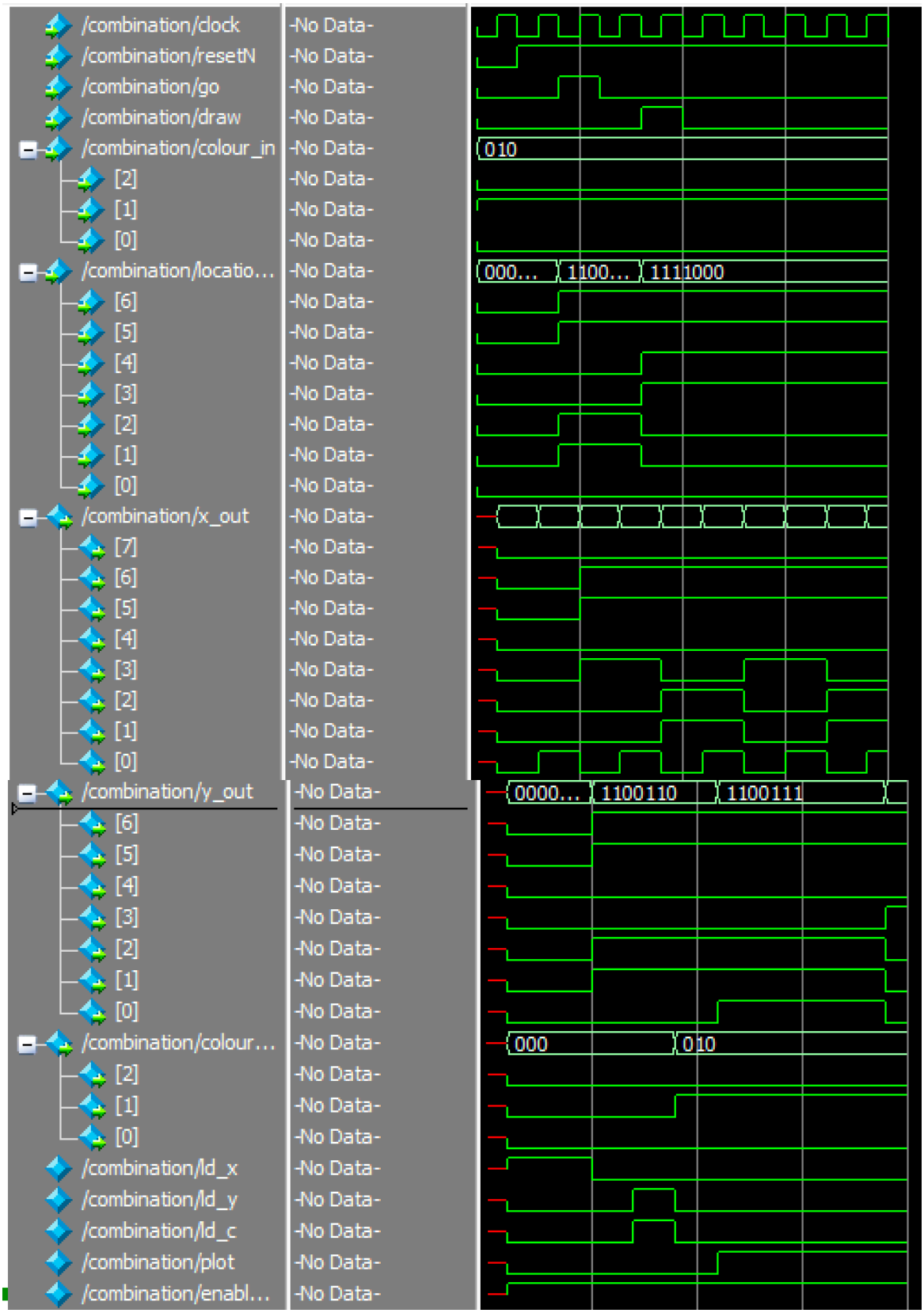
2. Design and simulate FSM
   see the file controller.v



current_state	ld_x	ld_y	ld_c	enable_i_x	Plot
S_Load_x	1	0	0	1	0
S_Load_y_c	1	1	1	1	0
Draw	1	1	1	1	1

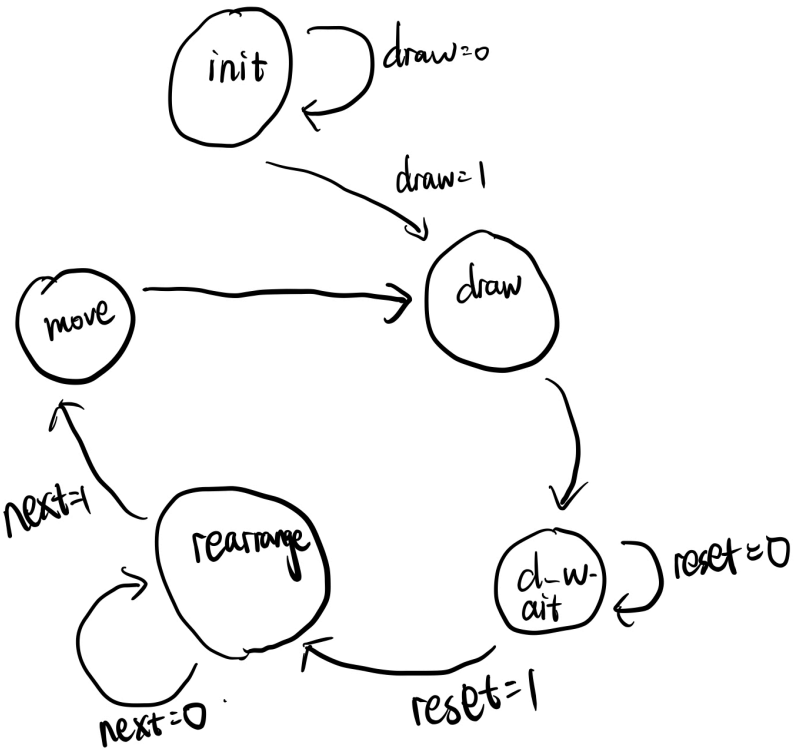


3. Simulate the combination of FSM and data path circuits
   see the file combination.v



Prat III

1. draw the schematic and state table



current_state	Draw	Reset	Next	next_state
Init	0	0	0	Init
Init	1	0	0	Draw
Draw	1	0	0	draw_wait
draw_wait	1	0	0	draw_wait
draw_wait	1	1	0	Rearrange
Rearrange	1	1	0	Rearrange
Rearrange	1	1	1	Move
Move	1	1	1	Draw