CSC258 Lab #3 Pre-Lab

The case statement, Adders and ALUs

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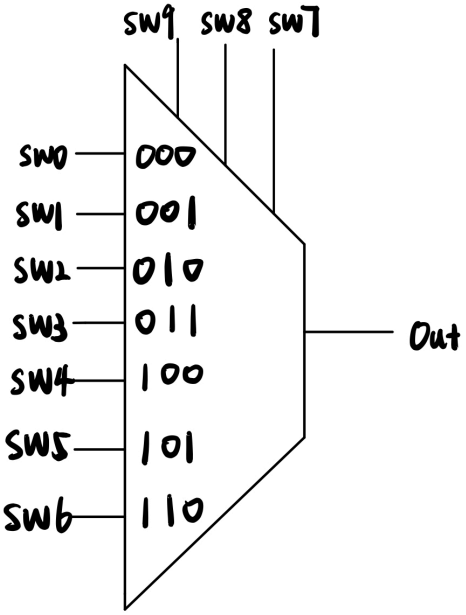
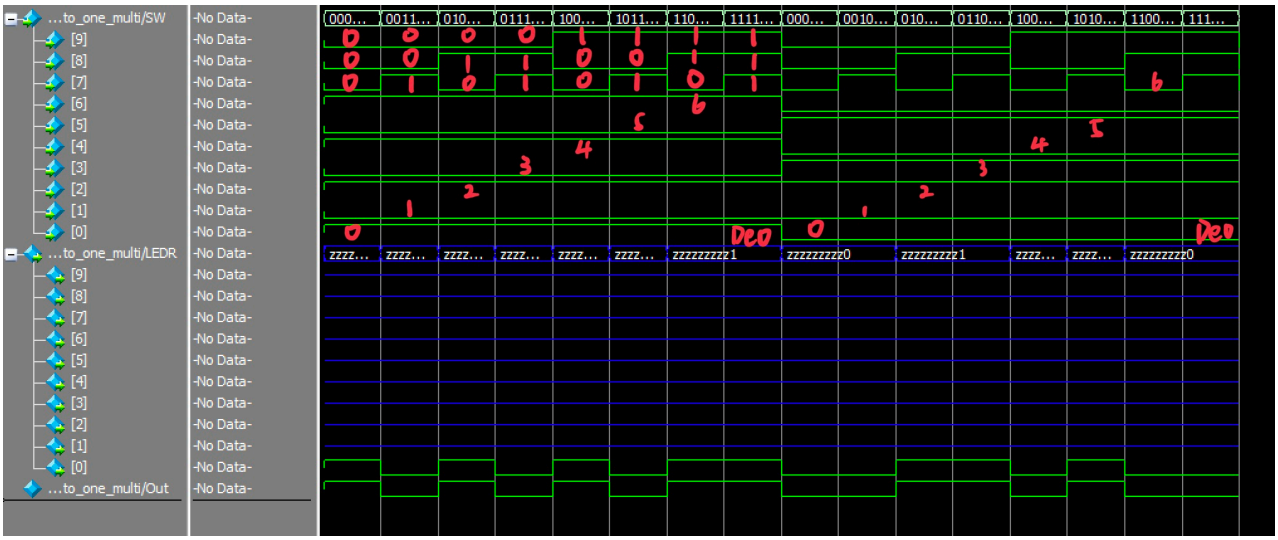
Prat I

1. Draw a schematic showing your code structure

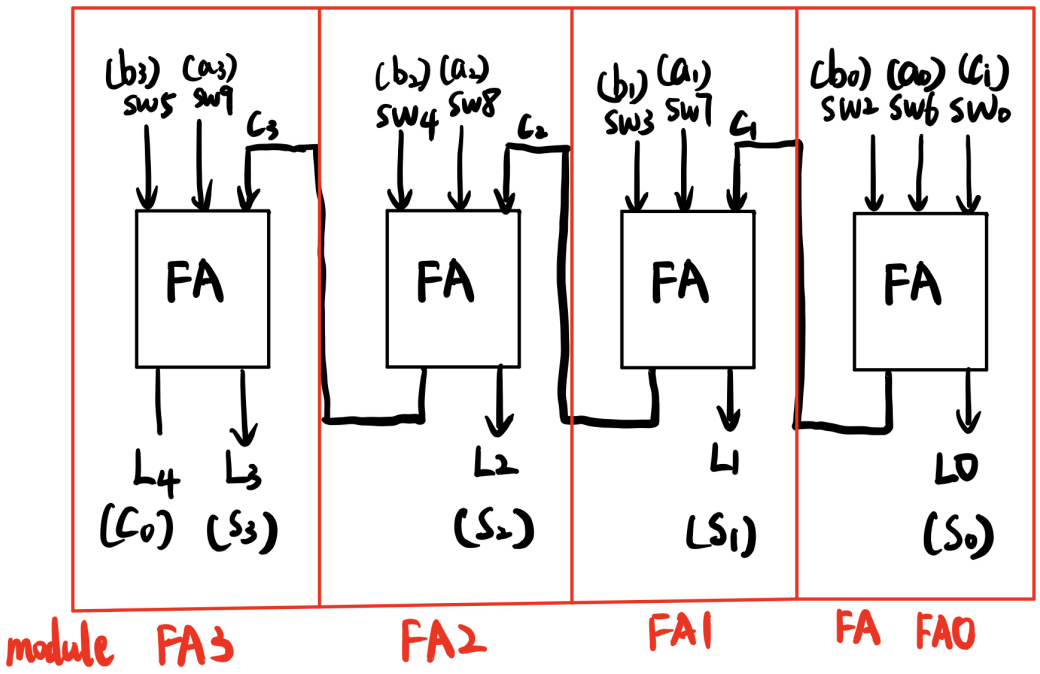


2. Write Verilog code for a 7-to-1 multiplexer
   see seven_to_one_multi.v
3. Simulate your circuit with ModelSim for different values of MuxSelect and Input

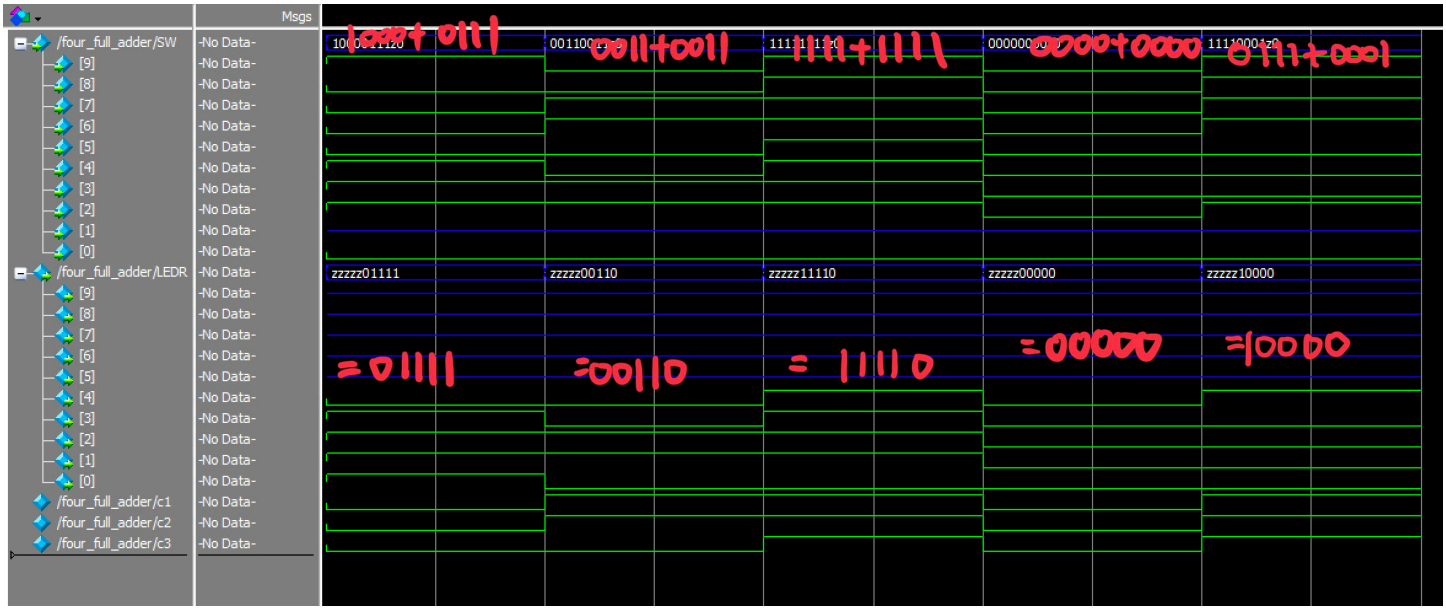


Prat II

1. Draw a schematic showing your code structure

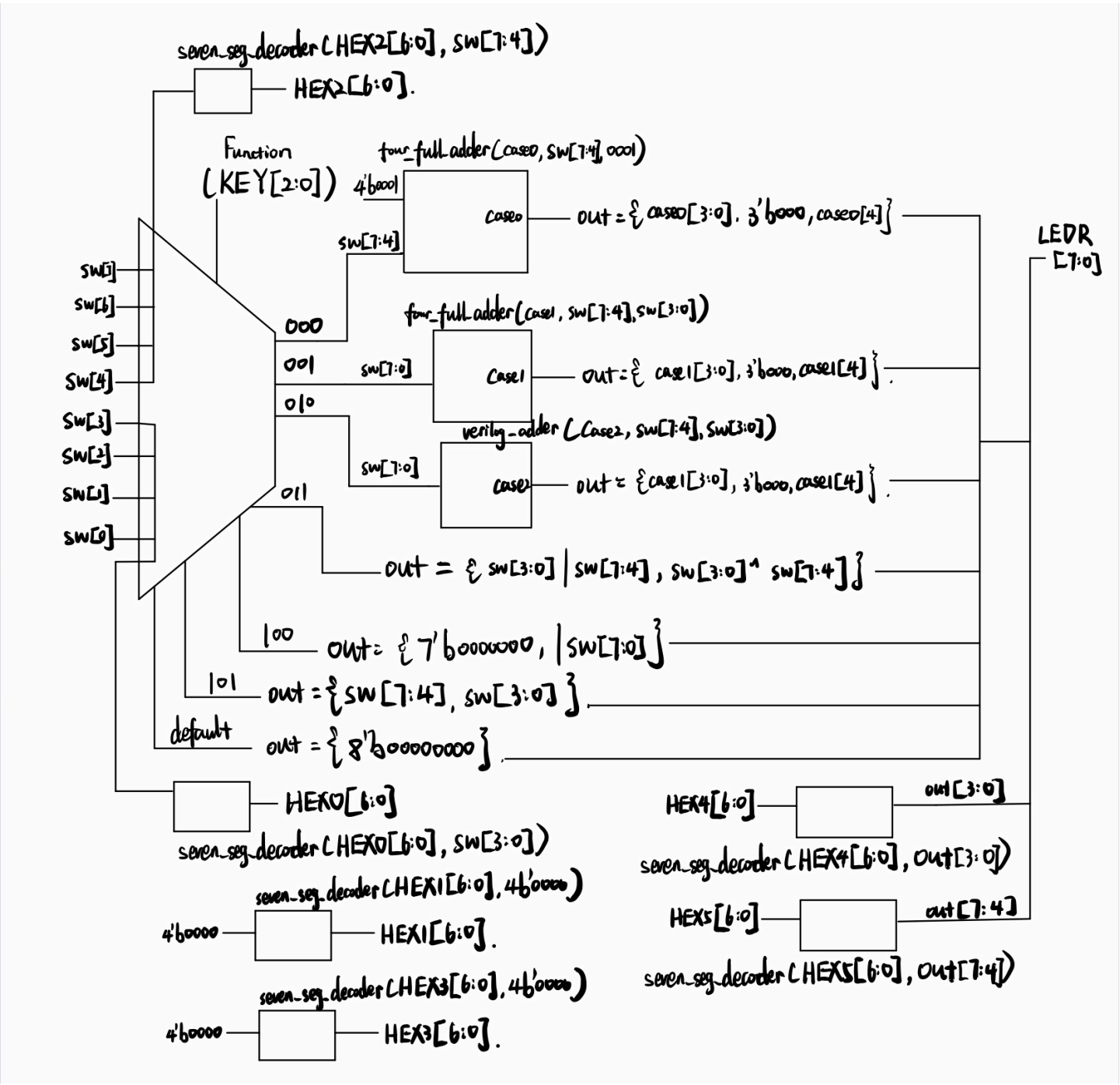


2. Write a Verilog module for the full adder subcircuit and write another Verilog module that in- stantiates four instances of this full adder.
   see four_full_adder.v
3. Simulate your 4-bit ripple-carry adder with ModelSim

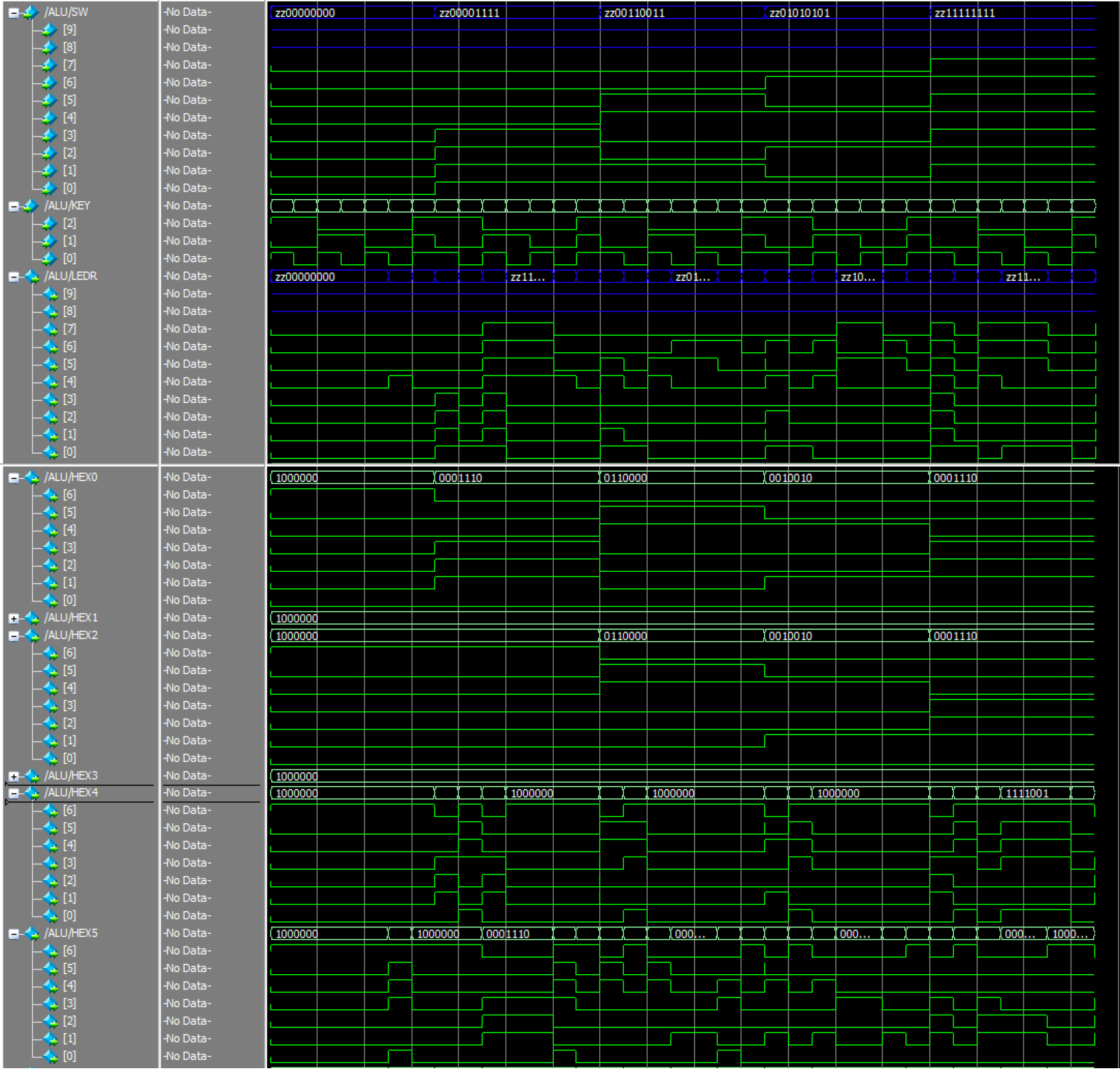


Part III

1. Draw a schematic showing your code structure



2. Write a Verilog module for the ALU including all inputs and outputs
   see ALU.v
3. Simulate your circuit with ModelSim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/ALU/LEDR
/ALU/HEX0
/ALU/HEX1
/ALU/HEX2
/ALU/HEX3
/ALU/HEX4
/ALU/HEX5
-No Data-
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zz00001111
zz00110011
zz01010101
zz11111111
zz11...
zz01...
zz10...
1000000
0001110
0110000
0010010
1111001
000...
1000...