In a system inverted page table is used. Each entry of the inverted page table stores process id and page number. Logical address is 40 bit, physical memory size is 64 GB and page size is 8 KB. Process id is represented by 8 bit. Determine size of the inverted page table.

Page Size 8 KB = 2^{13} B

Page # (27)	Offset (13)
40	

Logical Addr.

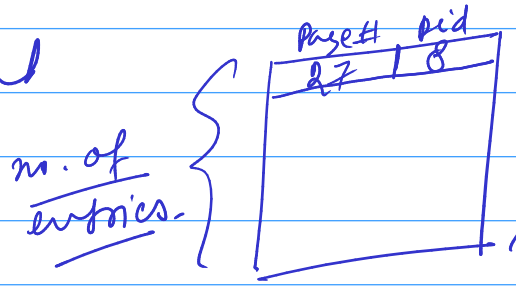
Frame #	offset
23	13

36 Physical Addr

Physical Mem = 64 GB

$= 2^{36}$.

Phy mem Addr. = 36 bit



IPT

8 X 5 = 40 bits

35 bits =

Size of IPT = 40×2^{23} B

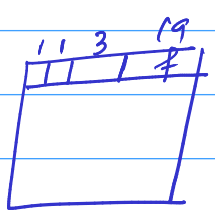
$= 5 \times 8 \times 2^{23}$ B

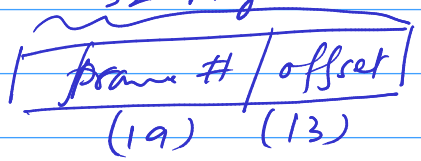
$= 5 \times 2^{26}$ B

$= 320$ MB

A computer system uses 8 kilobyte pages and a 32-bit physical address. Each page table entry contains a valid bit, a dirty bit, three permission bits, and the frame number. If the maximum size of the page table of a process is 24 megabytes, determine the length of the logical address supported by the system.
Now, if multi level page table is implemented then determine number of levels of the page table required. Determine the division of bits of the logical address that is required to address each levels of the multi level page table. Also determine the size of the multilevel page table.
Assume that, A TLB with hit ratio of 90% and access time 1 nanosecond, is introduced to cache recently used page table entries. Compare the effective memory access time of the single level and multi level paging scheme with TLB. Physical memory access time is 10 nanoseconds.

Page size = 8 KB = 2^{13} B

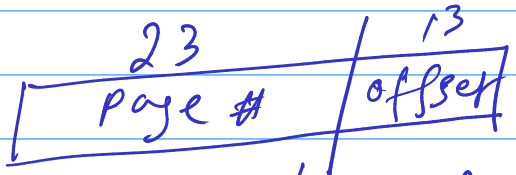




Size of each PT entry = (1 + 1 + 3 + 19) bits = 24 bits = 3 B

PT size = 24 MB = 24×2^{20} B

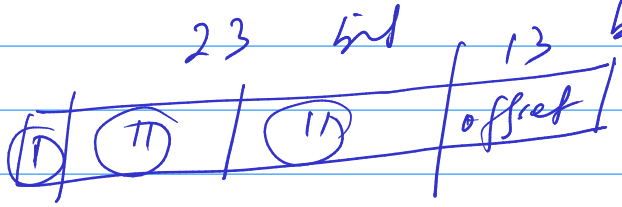
No. of pages = No. of entries in PT = $\frac{\text{size of PT}}{\text{size of each PT entry}}$ = $\frac{24 \times 2^{20}}{3}$ = $8 \times 2^{20} = 2^{23}$



Logical Addr. = 36 bit

Page size = 2^{13} B

No. of entries / page = $\frac{2^{13}\text{ B}}{3\text{ B}} \approx 2^{11}$



3 levels.

$m_a = 10$ ns.
$t_a = 1$ ns

$\alpha = 90\%$.

Single Level PT - with TLB.

$$EMA = \alpha(t_a + m_a) + (1-\alpha)(t_a + 2m_a)$$

$$= (0.9 \times 11 + 0.1 \times 21)\text{ ns}$$

$$= (9.9 + 2.1)\text{ ns}$$

$$= 12.0 \text{ ns}.$$

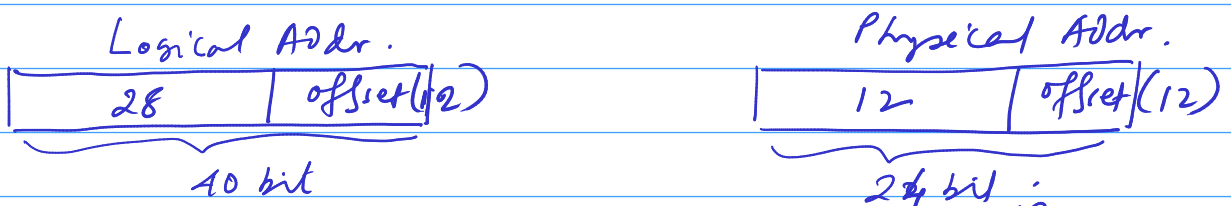
3 Level PT with TLB

$$EMA = \alpha(t_a + m_a) + (1-\alpha)(t_a + 4m_a)$$

$$= 0.9 \times 11 + 0.1 \times 41$$

$$= 9.9 + 4.1 = 14 \text{ ns}.$$

Consider a paging system with 40 bit logical address and 24 bit physical address. Page size is 4 KB and size of each page table entry is 2 bytes. Determine the size of page table if single level page table is used. Now, assume that you want to implement a multi level page table. Determine how many levels of page table is required if you need to store each page of the page table possibly in non contiguous frames in physical memory. Determine the division of bits of the logical address that is required to address each levels of the multi level page table. If physical memory access time is 10 nanoseconds, compare the effective memory access time of the single level and proposed multi level paging scheme.

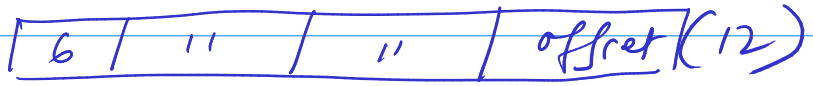


Page Size = 4 KB = 2^{12} B.

PT Size = No. of entries × Size of each entry

= $2^{28} \times 2$ B = 2^{29} B = 512 MB

No. of entries per page = $\frac{2^{12}}{2} = 2^{11}$



Logical Addr.

Single Level PT Size. 2^{29} B

No. of pages of 1st Level PT

= $\frac{2^{29}}{2^{12}} = 2^{17}$

No. of entries in 2^{nd} level PT

= No of pages of 1st Level PT

= 2^{17}

Size of 2^{nd} Level PT = $2^{17} \times 2 = 2^{18}$ B

No. of pages of 2^{nd} Level PT = $\frac{2^{18}}{2^{12}} = 2^6$

No. of entries in 3^{rd} Level PT = No of pages of 2^{nd} Level PT

= 2^6

In a system inverted page table is used. Size of the inverted page table is 16 MB. Each entry of the inverted page table stores pid, page number and some protection information. Logical address space is 32GB, physical memory size is 16 GB and page size is 4 KB. Process pid is represented by 8 bit. Determine the maximum number of bits that can be used for storing protection information in each entry of the inverted page table.

Page size = 4 KB
$= 2^{12}$

Entry of IPT

page #	pid	protection
23	(8)	1

page #	
23	12

35

frame #	
22	12

34 bit.

No. of entries in IPT $= 2^{22}$

Size of each entry of IPT $= \frac{2^{24}}{2^{22}} = 2^2$
$= 4$ B
$= 32$ bit