RULES:

- **Please try to work on your own. Discussion is permissible, but identical submissions are unacceptable!**
- **Please show all <u>intermediate</u> steps: a correct solution without an explanation will get <u>zero</u> credit.**
- **Please submit on time. <u>NO late submission will be accepted</u>.**
- **Please <u>prepare your submission in English only</u>. No Chinese submission will be accepted.**

1. [6%] Apply the node-analysis by-inspection method to generate the node voltage matrix for the circuit in Fig 1.

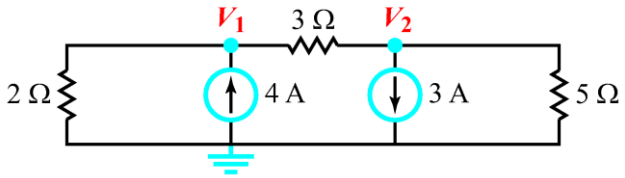

Fig 1.

2. [6%]
   A) Use the node-voltage method to find v_0 and the power delivered by the 2A current source in the circuit in Fig 2. Use node a as the reference node.
   B) Repeat part (A), but use node b as the reference node.
   C) Compare the choice of reference node in (a) and (b). Which is better, and why?

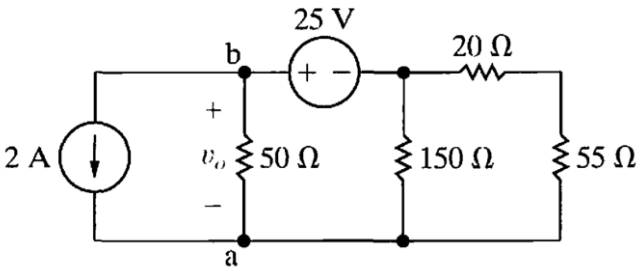

Fig 2

3. [6%] Use the node-voltage method to find the power developed by the 20V source in the circuit in Fig 3.

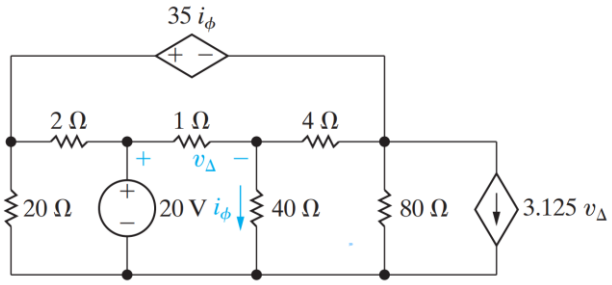

Fig 3

4. [6%] Find percentage of the total power developed in the circuit is delivered to R_o when R_o is set for maximum power transfer in Fig 4?

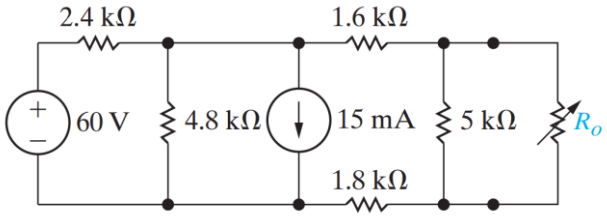

Fig 4

5. [6%] Use Mesh-Current method to find the power developed by the 50V source in Fig 5.

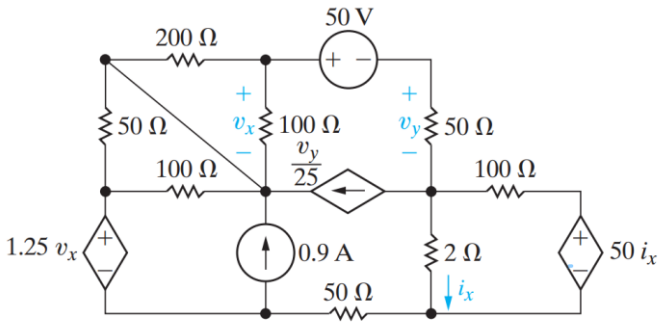

Fig 5

6. [6%]
   a) Use the mesh-current method to determine which sources in the circuit in Fig. 6 are generating power.
   b) Find the total power dissipated in the circuit.

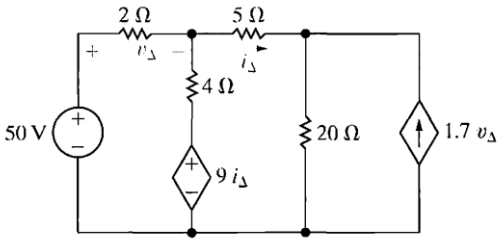

Fig 6

7. [5%] Use the mesh-current method to find the power developed in the dependent voltage source in the circuit in Fig 7.

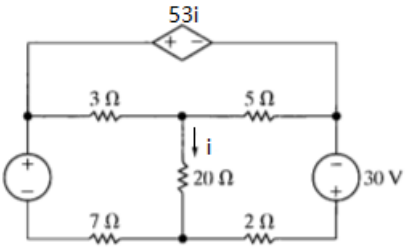

Fig 7

8. [7%]
   (a) Would you use the node-voltage or mesh-current method to find the power absorbed by the 20V source in the circuit below? Explain your choice.
   (b) Use the method you selected in (a) to find the power.

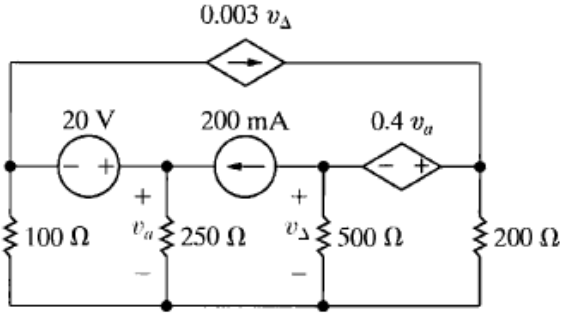

Figure 8

9. [7%] Use the inspection method to obtain a mesh-current matrix and solve i_1, i_2, i_3. In the circuit below, $V_1 = 12V$, $V_2 = 8V$, $V_3 = 6V$.

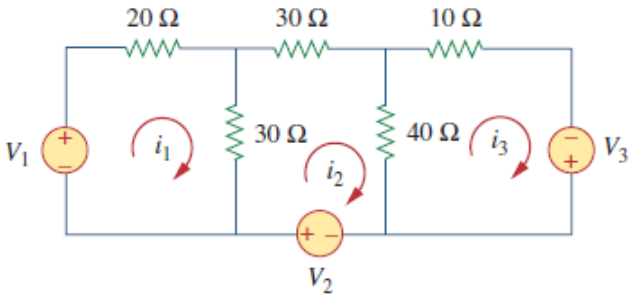

Figure 9

10. [45%] Programming Assignment

In the class you have learned how to use the nodal analysis and mesh analysis by inspection to analyze a complicated circuit. A simple example is showed as below.

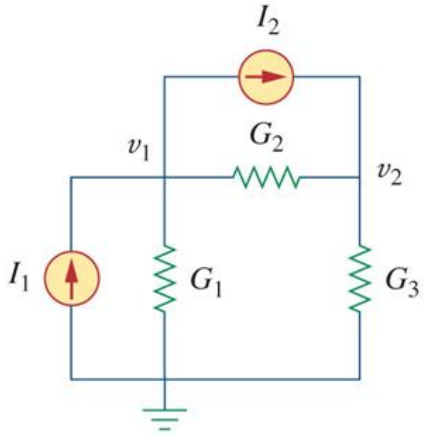

Figure 10

By inspection, we obtain

$$\begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_2 + G_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} I_1 - I_2 \\ I_2 \end{bmatrix}$$

where

$$G = \begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_2 + G_3 \end{bmatrix}$$

is the system conductance matrix created by mapping all the resistors in the circuit in a special manner.

In this assignment, you are asked to build the system conductance matrix G for a realistic circuit in power grid design:

1) Read the reference paper [1], especially Section VI, to see how to model a power grid as a resistor network.

2) Extract all the resistors in both metal layer M1 and metal layer M2 of the small example circuit shown in Figure 4, by analzing the SPICE code in Section VI of [1].
3) Refer to paper [2], use the stamping approach shown in Table I to build the system conductance matrix *G*.

Note that

1) the via resistance between two adjacent nodes in M1 and M2 layers is assumed to be zero in the spice file. So in your system matrix, you can merge the two end nodes connected by a via into one single node. For exmaple, nodes 'n0_25_25' and 'n2_25_25' of via 'V56' can be merged into one single node.
2) You only need to build the *G* matrix for the 'VDD' net.
3) You should write a Matlab srcipt to parse the spice code, and then build the *G* matrix in Matlab.
4) Finally, please submit both your Matlab code and the G matrix you got for this example circuit. You can attach the code and the matrix to your homework submission.

References for Problem 10

[1] Sani R. Nassif. "Power grid analysis benchmarks". In *Proceedings of the Asia and South Pacific Design Automation Conference*, pp. 376-381, 2008.

[2] Chung-Wen Ho, A. Ruehli and P. Brennan, "The modified nodal approach to network analysis," in *IEEE Transactions on Circuits and Systems*, vol. 22, no. 6, pp. 504-509, Jun 1975.