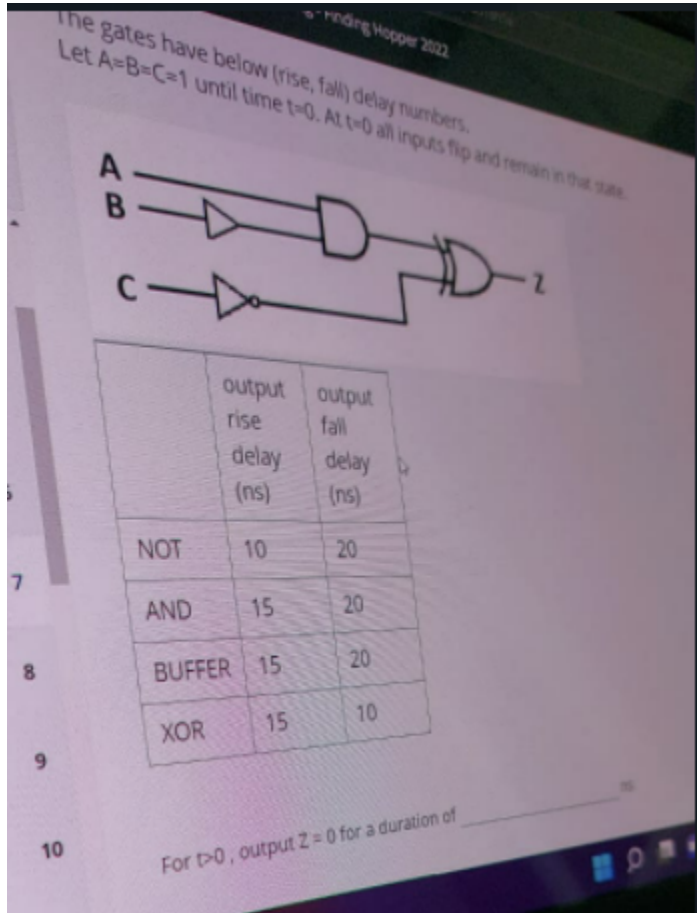- No introduction asked
- What are you passionate about?
- Where do you see yourself after Btech?
- First question was from the Digital Electronics section of the written round that I had answered incorrectly back then.

The gates have below (rise, fall) delay numbers.
Let A=B=C=1 until time t=0. At t=0 all inputs flip and remain in that state.

	output rise delay (ns)	output fall delay (ns)
NOT	10	20
AND	15	20
BUFFER	15	20
XOR	15	10

For t>0, output Z = 0 for a duration of _____

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- Second question was about DFS traversal. They once again showed a question from the written round where they had asked me to state the traversal path.
- A question on computer architecture that could be solved without prior knowledge of the same.
- What do you know about Full Adders?
- What logic gates can you implement using Full adders? (I was unable to answer this right away)
- Implement AND Gate using Full Adder (Hint: Make Cin =1)
- Implement OR Gate using Full Adder
- Some VLSI numericals