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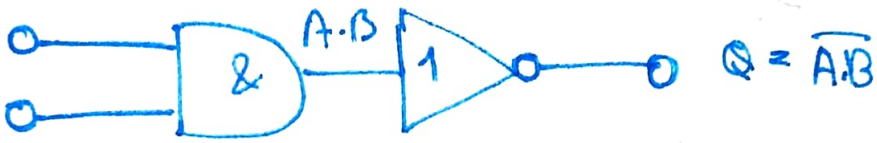
Course - MCA 1 A
Subject - Computer organization

Logical NAND gate

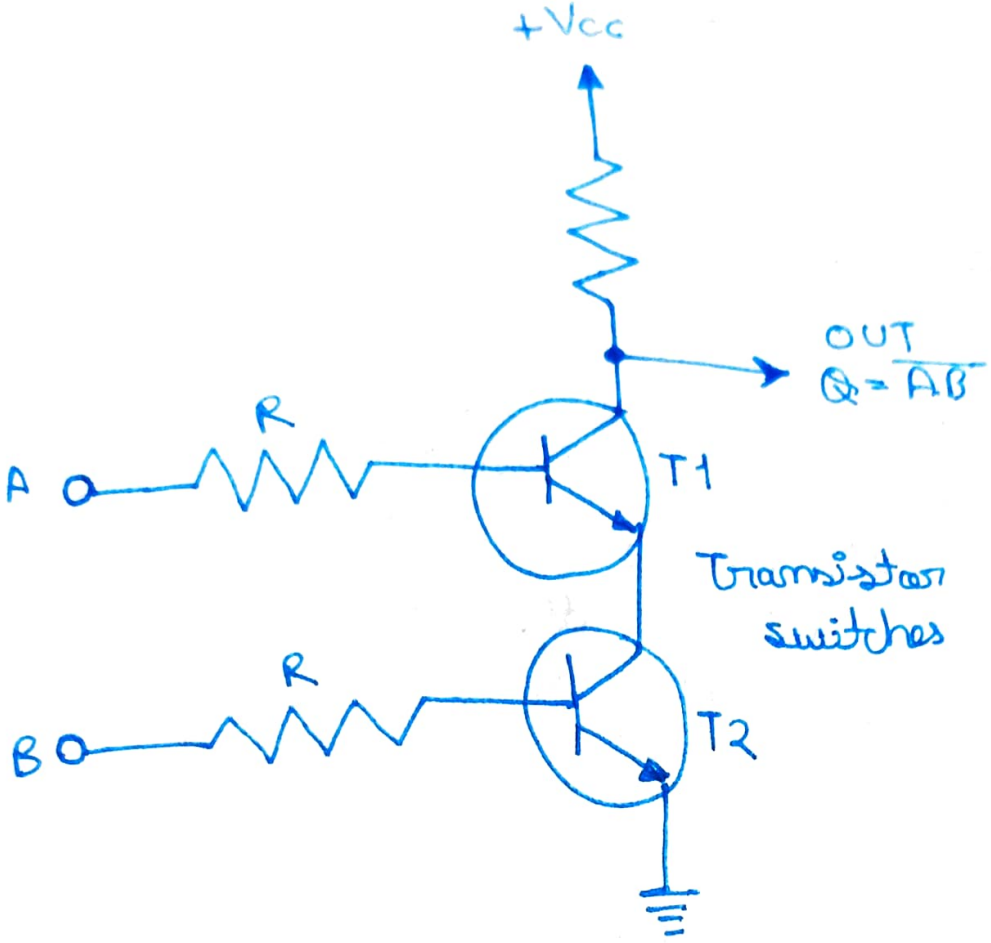
The NAND (Not-AND) gate has an output that is normally at logic level 1 "& only goes "low" to logic level "0" when ALL of its inputs are at logic level "1". The logic NAND gate is the reverse or "complementary" form of the AND gate we have seen previously.



Transistor NAND Gate :-

A simple 2-input logic NAND gate can be constructed using RTL Resistor-transistor switches connected together as shown below with the inputs connected directly to the transistor bases. Either transistor must be cut-off "OFF" for an output at Q.

Vjaiswal



Truth Table :-

B	A	OUT
0	0	1
0	1	1
1	0	1
1	1	0