Enroll no
PV-21010184

Graphic Era Hill University, Dehradun
(Answer Sheet for Online Examination Feb. 2022)

Please tick (√) your campus: (DEHRADUN/BHIMTAL/HALDWANI)

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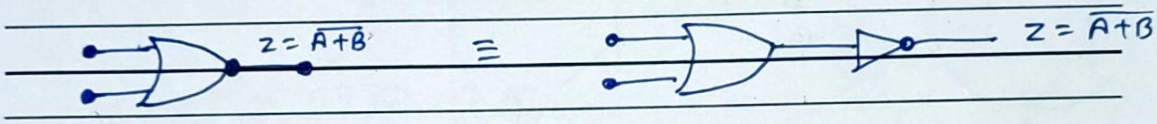
Date: 27/3/22 Course: MCA Branch: Sem.: 1 Section: B
Subject Name: COA ~~paper~~ mid Sem Subject Code: Page No.

NOR Gate

The term NOR is contraction of NOT-OR and implies an OR function with inverted output. The output of this gate is high only when all input voltages are low. A standard logic symbol for a 2-input NOR gate and the equivalent OR gate followed by and INVERTOR are shown in below figure.

Standard NOR Gate logic Symbol.



The operation of this gate ~~is~~ OR gate Z' is

$$Z' = A+B+C+ \ldots\ldots N$$

and the output of NOT gate is

$$Z = \overline{Z'} = \overline{A+B+C- \ldots N}$$

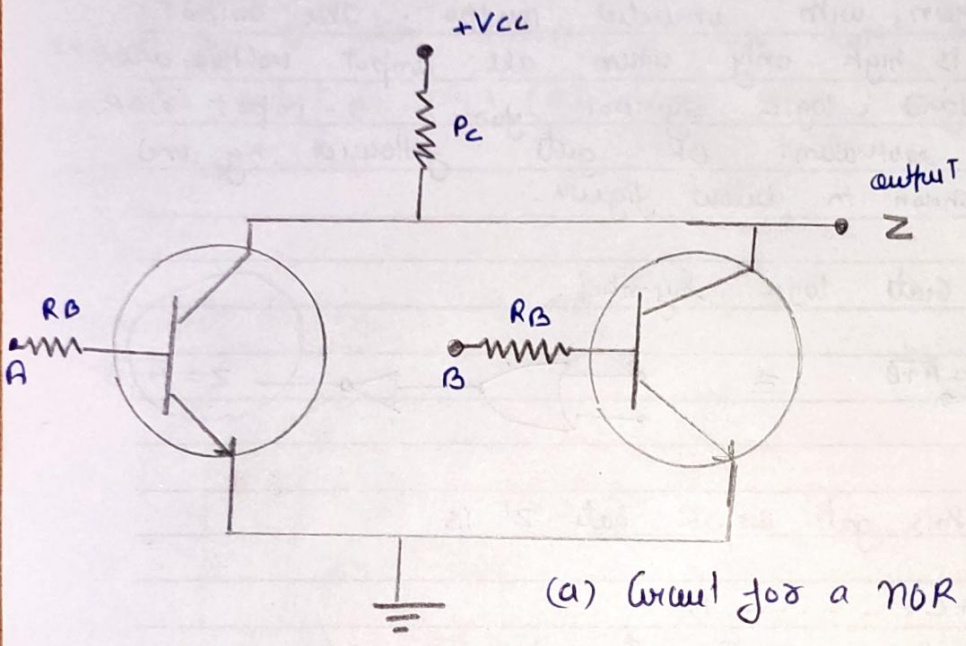
Truth Table for NOR gate is

Input		output Z
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

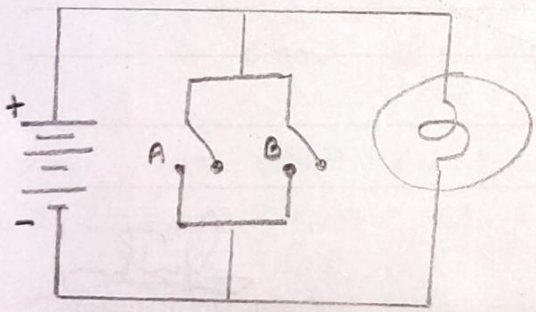
Signature of Student

From table we find the NOR gate output is exact inverse of OR-gate output for all possible input conditions.
whereas an OR-gate output ~~for all high~~ goes high when any input is high, the NOR gate output goes low when any input is high.

Circuit diagram for NOR gate.



(a) Circuit for a NOR gate

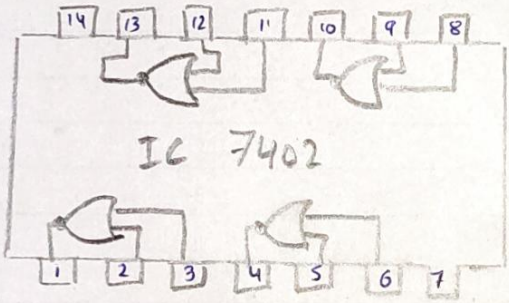


(b) Electrical Analog of NOR gate.

The electrical circuit and electrical analog of NOR gate are shown in diagram. As seen from (a) the output Z is L only when both transistor are cut off. i when A = 0 and B = 0 for any other condition of input such as A=1 B=0 or A = 0, B = 1 or A = 1 B = 1, one or both transistor operates in saturation and as a result the output Z is low.

From diagram (b) it is evident that lamp does not glow the output is 0 when either of two ~~lamp~~ input A or B is high. The output is high (the lamp glow) only when both of input are low.

Standard Package IC 7402



pinout diagram for NOR gate

The above figure depicts the pinout diagram of IC 7402. a TTL quad 2 input NOR gate. This IC contains 4 2-pin 2 input NOR gates inside a 14-pin dual in line package (DIP).