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Q1:- **Nand Gate:-** The NAND gate is a special type of logic gate in the digital logic circuit. The NAND gate is the universal gate. It means all the basic gates such as AND, OR and NOT gate can be constructed using a NAND gate. The NAND gate is the combination of NOT-AND gate. The o/p state of NAND gate will be low only when all the i/p are high. Simply, this gate returns the complement result of the AND gate.

The logic or boolean expression for the NAND gate is the complement of logical multiplication of i/p denoted by a full stop on a single dot as -

$(A \cdot B)' = Y$

The value of Y will be true when any one of the i/p is set to 0.

The 2-input NAND gate:- This is the simple formation of the NAND gate. In this type of NAND gate, there are only two i/p values and an o/p value. There are $2^2 = 4$ possible combinations of i/p. The truth table and

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Circuit diagram are following:-

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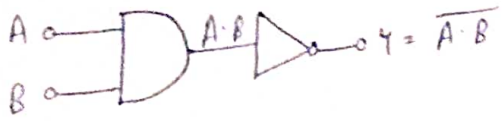

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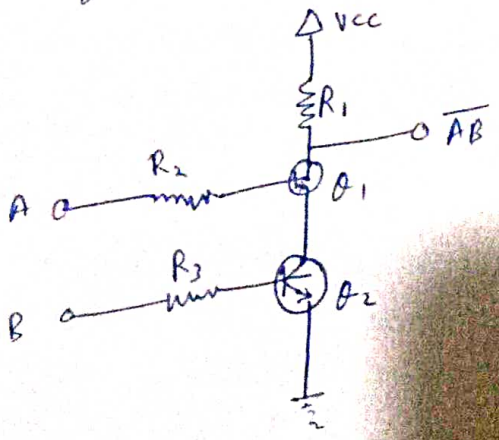
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Circuit diagram:- Simple 2 i/p logic NAND gate can be constructed using transistors connected together as below with i/p connected directly to the transistors base. Either of the transister must be cut off 'off' for o/p to be logic high. This means if both the i/p are cut logic high making both the transister 'on' the resultant o/p is Low (0).



A	B	Q_1	Q_2	o/p
0	0	off	off	1
0	1	off	on	1
1	0	on	off	1
1	1	on	off	0