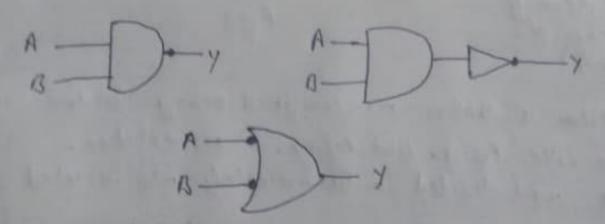
Mane: Shano Komer UNIV. Roll - 2101196 Sem - Ist Course- MCA - Stetien - D

Qui Any The NAND gate has an outlet that is normally at light high and only goes to logic low when all of its in Pot are at logic high. The Logic NAND hate is the revorce or complementary design of the AND gate. Through this article on NAND gates, you will bear about the symbol that that table of two and three input gates, along with the boolen expression, circuit diagram and representation of various other gates using NAND gates.

The NAND gate is AND gate succeeded by Not gate.

Thus one can understand the NAND gate as Not - AND gate also. A NAND gate constitutes one of more in Poss with a single output. The NAND gate is reprotented by a symbol whose shape matches the AND gate with a circle followed, after Identified as an invention circle. Below is the symbolic representation of NAND gate.



*NANDgate = subbled OR gate +

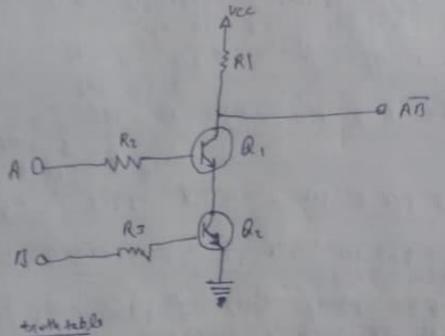
NAND Gate Truth table

7= A.B = A +B

Indus		OUTROT	
0	0	1	1
0	1	1	1
1	0	T'	1
)	1 1 1	0	
4 3 5 5 3	31.75		

NAND hate circuit Diagram

A simple two-input lopic NAND gate can be constructed using transistary connecrated together as shown below with the invote connected directly to the transistant most be even off off for out but to be logic high. This means that if both the invote are at losic high making both the transistant "our the resultant output is low 16".



0	5	Q,	Q2	OUTPUT
~	0	OFF	OFF	1
_	1	off	ON)
D	0	ON	OFF	1
1	-	ON	ON	
1	1			0