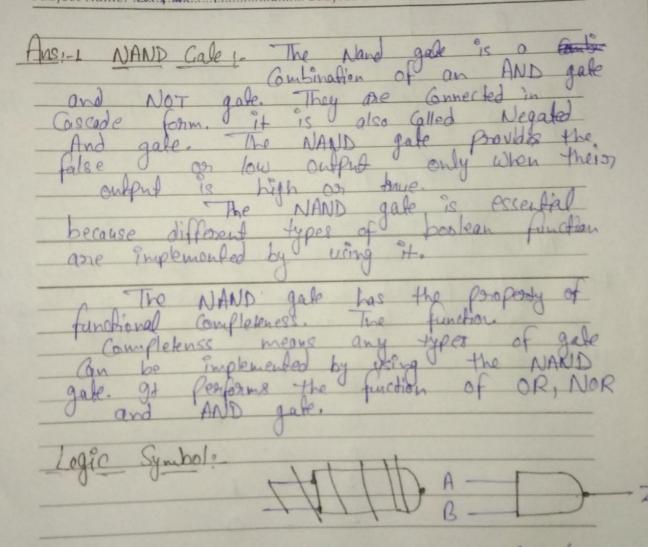
Father names Devendra Singh

Graphic Era Hill University, Dehradun (Answer Sheet for Online Examination Feb. 2022)

Name: Gauges Singh Univ.Roll No. 2101261 Student ID 21711290
Date: 22103/2022Course: MCH Branch: Sem. 15t Section: D
Subject Name: Computer Architecture. Subject Code: TMC 102 Page No. C1

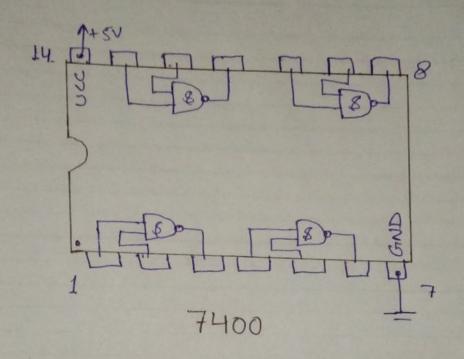


Signature of Student

Page vo 1 02 The logic Circuit of the NAND gale is Shown below: from the Logic Circuit, the output Can be expnessed as: Z = A.B The equation is nead as "Z equels NOT A AND B". Since the logic Circuit involves an AND gate followed by an invertex. The output can only be low when both the input are high. Thuth table :-A

Sgrature

Ans 1 Poll no! - ST university no: 2101261 Page no: 03



NAND GATE ON'IC 7400'

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