COA ASSIGNMENT-2 (Solution)

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1. How is redundancy achieved in a RAID system?

Redundancy means that your system contains duplicate copies of file. In the event of a failure you have another available copy to work with which is great if you can't afford to lose any of your files. Redundancy is achieved by "striping", "mirroring" or a mix of "striping and parity".

RAID 0 is the only RAID configuration that does not provide redundancy, it provides a speed boost but if a drive fails you're out of luck.

RAID 1 achieves redundancy by having identical copies of a disk which is known as data mirroring.

RAID 2 uses data striping with error correcting code to achieve redundancy.

RAID 3 uses parity information to achieve redundancy.

RAID 5 matches striping and parity to achieve data redundancy.

RAID 6 uses striping and double parity across drives to achieve redundancy.

2. Consider a 4-Drive, 200 GB-per-drive RAID array. What is the available data storage capacity for each of the RAID levels 0, 1, 3, 4, 5 and 6?

Number of disk = 4

Capacity per drive = 200 GB

Total storage capacity= 200 x 4 = 800 GB

RAID 0→ (4) x 200 = 800 GB

RAID 1→ (4/2) x 200 = 400 GB

RAID 3→ (4-1) x 200 = 600 GB

RAID 4 → (4-1) x 200 = 600 GB

RAID 5→ (4-1) x 200 = 600 GB

RAID 6 → (4-2) x 200 = 400 GB

3. Explain the CD-ROM block format.

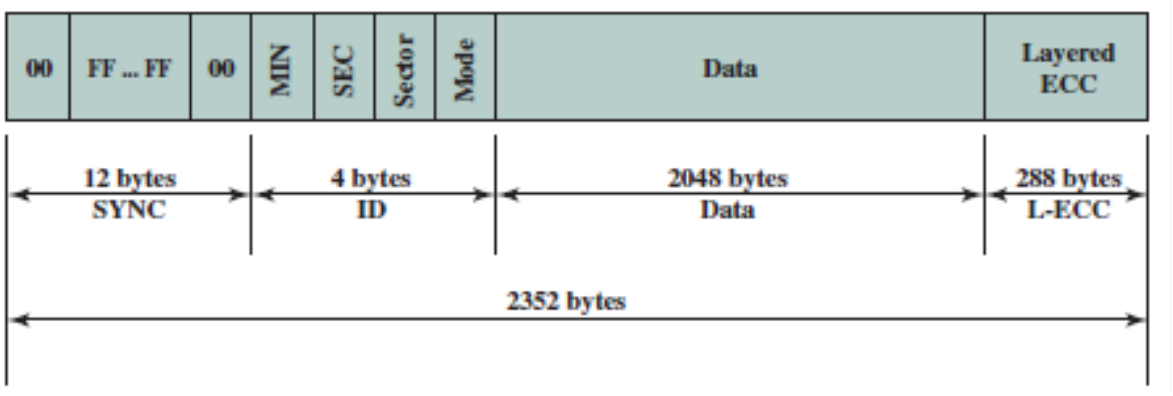
It consists of the following fields:

•**Sync:** The Sync field identifies the beginning of a block. It consists of a byte of all 0s, 10 byte so fall 1s, and a byte of all 0s.

•**Header:** The header contains the block address and the mode byte. **Mode 0** specifies a blank data field; **mode1** specifies the use of an error-correcting code and 2048 bytes of data; **mode 2** specifies 2336 byte so fuser data with no error-correcting code.

•**Data:** User data.

•**Auxiliary:** Additional user data in mode 2. In mode1, this is a 288-byte error-correcting code.



4. How the information is retrieved from a CD or CD-ROM?

To read a CD-ROM a laser light is thrown in the disc surface and the light reflection gives the data. In case of audio CD's, audio player simply traverses the grooves, thus decoding the information and sending this digitized information to digital-to-analogue converter.

5. Discuss the advantages and disadvantages of CD-ROM.

Advantage of CD-ROM:

- The optical disk is removable, allowing the disk itself to be used for archival storage.
- The optical disk together with the information stored on it can be mass replicated inexpensively unlike magnetic disk.

Disadvantage of CD-ROM:

- In the phase change optical disks, the material eventually and permanently loses its desirable property.
- It is read-only and cannot be updated.

6. Consider a 4-Drive, 200 GB-per-drive RAID array. What is the available data storage capacity for each of the RAID levels 0, 1, 3, 4, 5 and 6?

Same as Solution no. -> 2

7. What is the difference between memory- mapped I/O and isolated I/O?

Difference between Isolated I/O and Memory-Mapped I/O are:

ISOLATED I/O	MEMORY MAPPED I/O
Memory and I/O have separate address space	Both have same address space
All address can be used by the memory	Due to addition of I/O addressable memory become less for memory
Separate instruction control read and write operation in I/O and Memory	Same instructions can control both I/O and Memory
In this I/O address are called ports.	Normal memory address are for both
More efficient due to separate buses	Lesser efficient
Larger in size due to more buses	Smaller in size
It is complex due to separate separate logic is used to control both.	Simpler logic is used as I/O is also treated as memory only.

8. When a DMA module takes control of a bus, and while it retains control of the bus, what does the processor do?

When the DMA controller takes over the bus, the processor responds with a HLDA signal and remains on hold until the DMA controller executes its task of transferring data from/to periferal devices to/from main memory. When the data transfer complete DMA gives out HRQ signal thus returning the control of bus back to processor. Throughout the process of data transfer processor remains idle.

9. A system is based on an 8-bit microprocessor and has two I/O devices. The I/O controllers for this system use Separate control and status registers. Both devices handle data on a 1- byte-at-a-time basis. The first device has two status lines and three control lines. The second device has three status lines and four control lines.

(a) How many 8-bit I/O control module registers do we need for status reading and control of each device?

(b) What is the total number of needed control module registers given that the first device is an output-only devices?

(c) How many distinct addresses are needed to control the two devices?

(a) The first device has 2 status lines and 3 control lines.3 control line can generate 8 control signals. So, 1 eight bit register is enough to control 1st device. The second device has 3 status lines and 4 control lines. 4 control lines can generate 16 control signals and for that we need 2 eight bit registers.

(b) If one device is output-only device then control register is not needed for that device. So only one control register is required to control the other device.

(c) 8 bit microprocessor. Each 4 bit can generate 1 memory addresses by 4 bit we can generate 2^4 addresses.

Then by 8 bit we can generate 2^8 addresses.

10. What is the difference between a process and a program?

Difference between **Process** and **Program** are:-

Process	Program
An executing part of a program is called a process.	A program is a group of ordered operations to achieve a programming goal.
The process is an instance of the program being executing.	The nature of the program is passive, so it's unlikely to do to anything until it gets executed.
The resource requirement is quite high in case of a process.	The program only needs memory for storage.
Processes have considerable overhead.	No significant overhead cost.
The process has a shorter and very limited lifespan as it gets terminated after the completion of the task.	A program has a longer lifespan as it is stored in the memory until it is not manually deleted.
New processes require duplication of the parent process.	No such duplication is needed.

11. Consider a fixed partitioning scheme with equal- size partitions of 2^{16} bytes and a total main memory size of 2^{24} bytes. A process table is maintained that includes a pointer to a partition for each resident process. How many bits are required for the pointer?

Partition size = 2^{16} bytes

Total main memory size = 2^{24} bytes

Bits = 2^{24} / 2^{16} = 2^{8}

Therefore, 8 bits are required for the pointer.

12. What is the purpose of swapping?

The purpose of swapping, Is to access data being stored in hard disk and to bring it into the RAM so that it can be used by the application program. Swapping is only necessary only when that data is not already in the RAM.

13. List the difference between RISC and CISC.

Difference between **RISC** and ***CISC*** are:-

CISC	RISC
A large number of instructions are present in the architecture.	Very fewer instructions are present. The number of instructions are generally less than 100.
Some instructions with long execution times. These include instructions that copy an entire block from one part of memory to another and others that copy multiple registers to and from memory.	No instruction with a long execution time due to very simple instruction set. Some early RISC machines did not even have an integer multiply instruction, requiring compilers to implement multiplication as a sequence of additions.
Variable-length encodings of the instructions. **Example:** IA32 instruction size can range from 1 to 15 bytes.	Fixed-length encodings of the instructions are used. **Example:** In IA32, generally all instructions are encoded as 4 bytes.
Multiple formats are supported for specifying operands. A memory operand specifier can have many different combinations of displacement, base and index registers.	Simple addressing formats are supported. Only base and displacement addressing is allowed.
CISC supports array.	RISC does not supports array.

14. What are the beneficial features and the limitations of a bus organization?

Beneficial features:-

- It is easy to connect a device to the network.
- It is cheaper.
- No hubs or switches are required.
- Extensions can be to the network.

Limitations:-

- Additional devices slows the network down.
- Size limitations are always present.
- Maintenance cost is high.
- Security option is limited.

15. What is the difference between software and hardware cache coherent schemes?

Software cache coherence schemes attempt to avoid the need for additional hardware circuitry and logic by relying on the compiler and operating the system to deal with the problem.

In hardware schemes, the cache coherence logic is implemented in hardware.

16. Summarize the differences among simple instruction pipelining, superscalar, and simultaneous multithreading.

Difference between Pipelining, Superscalar and Simultaneous Multithreading are:-

Simple instruction pipelining	Superscalar	simultaneous multithreading
In each stage only one instruction is executed	By using the execution resources multiple pipelines are constructed	Multiple threads are executed in multiple pipelines.
Efficiency is poor compared to other two techniques given	Improved efficiency compared to simple instruction pipeline	Efficiency is good
One instruction is executed at each stage	Uses instruction level parallelism	Uses thread level parallelism
Has only one pipelined functional unit	Has more than one pipelined functional unit	Has more than one pipelined functional unit
Resources are not replicated since instructions are executed in sequential order	Execution resources are replicated to construct multiple pipelines	Register banks are replicated to execute multiple threads using pipeline concept.

17. Consider the following loop:

S: = 0; for K: =1 to 100 do S: =S - K; A straightforward translation of this into a generic assembly language would look something like this:

```
     LD     R1, 0          ;keep value of S in R1
     LD     R2,1           ;keep value of K in R2
LP   SUB    R1, R1, R2     ;S:=S − K
     BEQ    R2, 100, EXIT  ;done if K = 100
     ADD    R2, R2, 1      ;else increment K
     JMP    LP             ;back to start of loop
```

A compiler for a RISC machine will introduce delay slots into this code so that the processor can employ the delayed branch mechanism. The JMP instruction is easy to deal with, because this instruction is always followed by the SUB instruction; therefore, we can simply place a copy of the SUB instruction in the delay slot after the JMP. The BEQ presents a difficulty. We can't leave the code as is, because the ADD instruction would then be executed one too many times. Therefore, a NOP instruction is needed. Show the resulting code.

To show the resulting code simply copying SUB instruction and making use of NOP instruction:

As per the requirements given in the question, below code is given:

Steps	Instructions	Comments
1	LD R1, 0	keep value of S in R1
2	LD R2, 1	keep value of K in R2
3	LP SUB R1, R1, R2	S: = S – 1
4	LP1 BEQ R2, 100, EXIT	done if K = 100
5	NOP	
6	ADD R2, R2, 1	else increment K
7	JMP LP1	back to start of loop
8	SUB R1, R1, R2	Execution of SUB in JMP delay slot

18. What are the chief characteristics of an SMP?

The chief characteristics of **SMP** are as listed below;

- There are two or more similar processors of comparable capability.
- These processors share the same main memory and I/O facilities and are interconnected by a bus or other internal connection scheme, such that memory access time is approximately the same for each processor.
- All processors share access to I/O devices, either through the same channels or through different channels that provide paths to the same device.
- All processors can perform the same functions (hence the term symmetric).
- The system is controlled by an integrated operating system that provides interaction between processors and their programs at the job, task, file, and data element levels

19. Represent the following decimal numbers in both binary sign/magnitude and twos complement using 16 bits: + 512; - 29.

Sign Magnitude:-

- 512 = 0000 0010 0000 0000
- -29 = 1000 0000 0001 1101

Two's Compliment:-

- 512 = 0000 0010 0000 0000
- -29 = 1111 1111 1110 0011

20. An address field in an instruction contains decimal value 25. Where is the corresponding operand located for a) immediate addressing? b) Direct addressing? c) Indirect addressing? d) Register addressing? e) Register indirect addressing?

(a) Operand A, the address field

(b) EA=A=25, memory location 25

(c) EA= (A) =25, the memory location whose address is in memory location 25

(d) ER=R=25, register 25

(e) EA=(R) =25, the memory location whose address is in register 25

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