EXPT. NO.

NAME:

Workshop:-1 [CMOS Inverter Design]

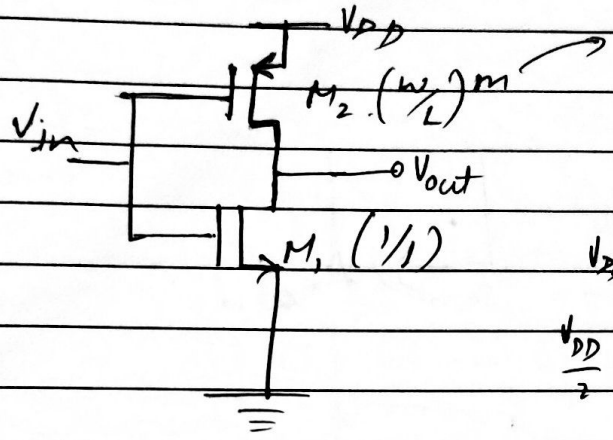
Page No.:

Date:

YOUVA

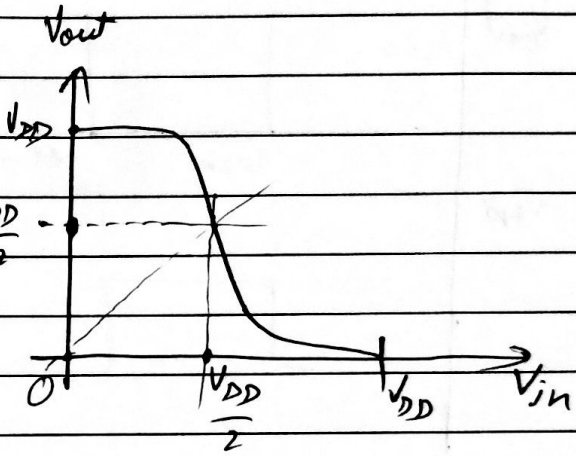
M T W T F S S

Switching Threshold → $V_{TH} = \frac{V_{DD}}{2}$



→ we'll change m = 1, 2, 3, 4, 5 ---

So, we'll get $V_{in} = \frac{V_{DD}}{2}$



For mid-point both PMOS & NMOS will be in saturation.

$$(I_D)_p = (I_D)_n$$

$$\frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_p \left[V_{GS} - |V_{tmp}|\right]^2 = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[V_{GS} - V_{tmn}\right]^2$$

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\mu_n}{\mu_p} \frac{\left(V_{GS} - (V_{tn})_n\right)^2}{\left(V_{GS} - |V_{tmp}|\right)^2}$$

For 180nm technology

$(V_{th})_n = 0.3075V$

$(V_{th})_p = -0.455V$

$\mu_n = 314 \text{ cm}^{-2}/\text{Vs}$

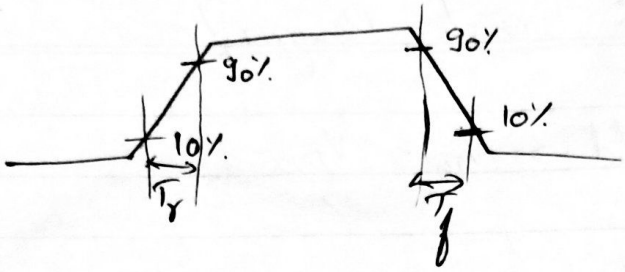
$\mu_p = 114 \text{ cm}^{-2}/\text{Vs}$

After substitution:-

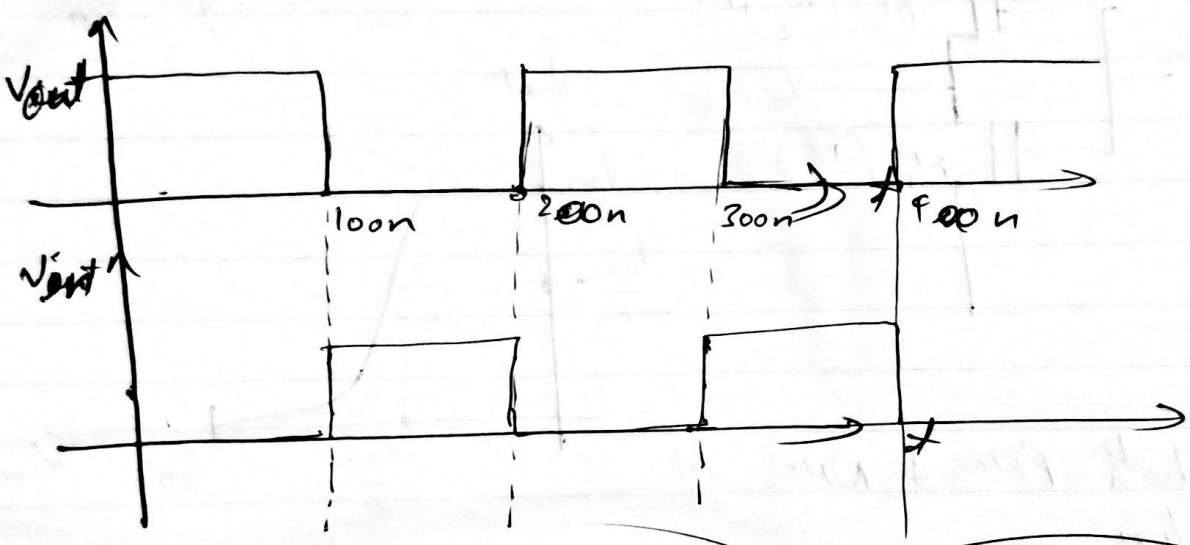
$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \text{₹}$$

Teacher's Signature:

Rise time & Fall time



90% of 1.8V = 1.62V
10% of 1.8V = 0.18V



$T_r = 100$ ns

$T_f = 459.5$ ps
$= 0.459$ ns

$T_f = 661.15$ ps
$= 0.661$ ns.

$V_{mid} = 0.89$ V