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Struktur

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2. Architektur
3. Layers
    a. Physical Layer
        - Datenübertragung
    b. Data Link Layer
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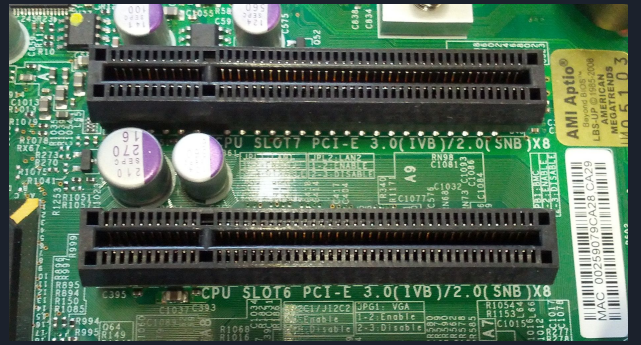
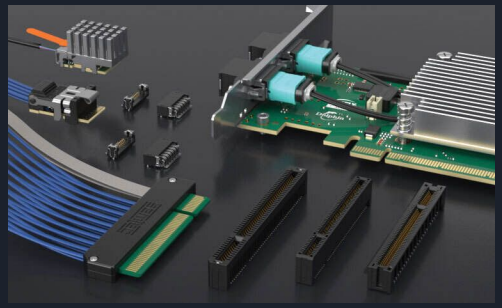
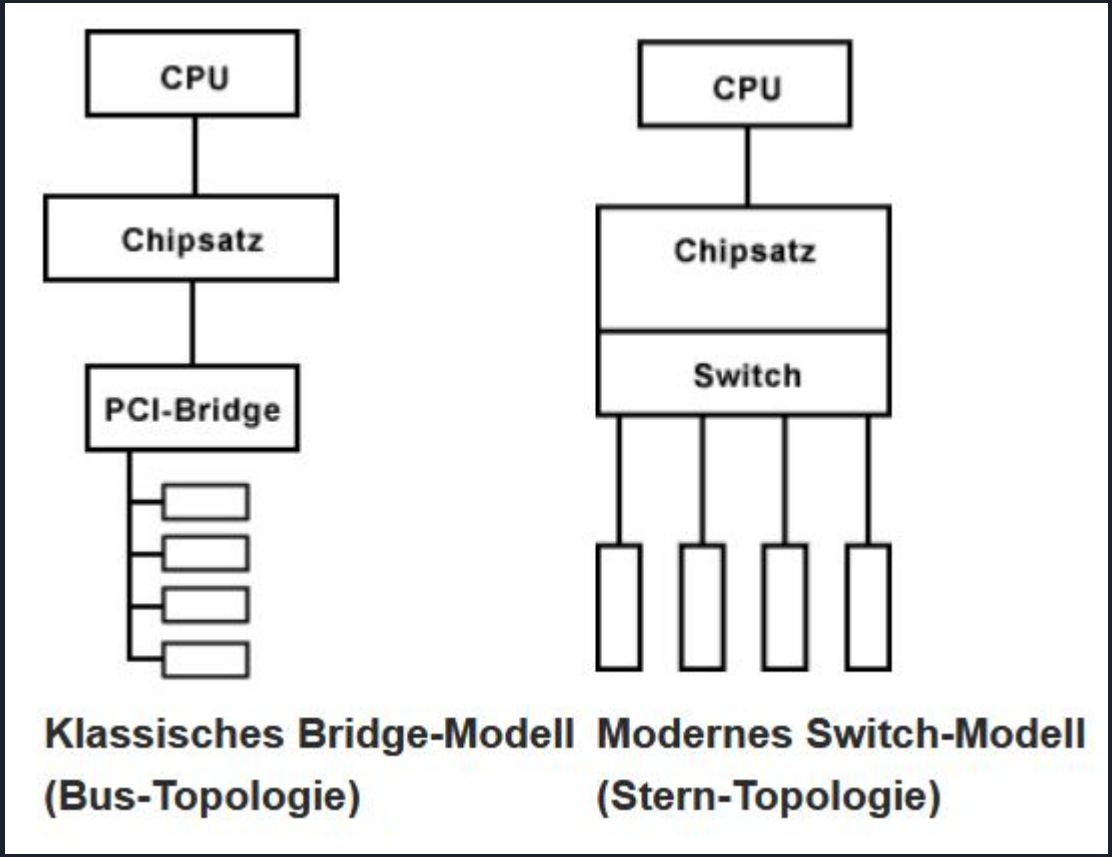
Definition



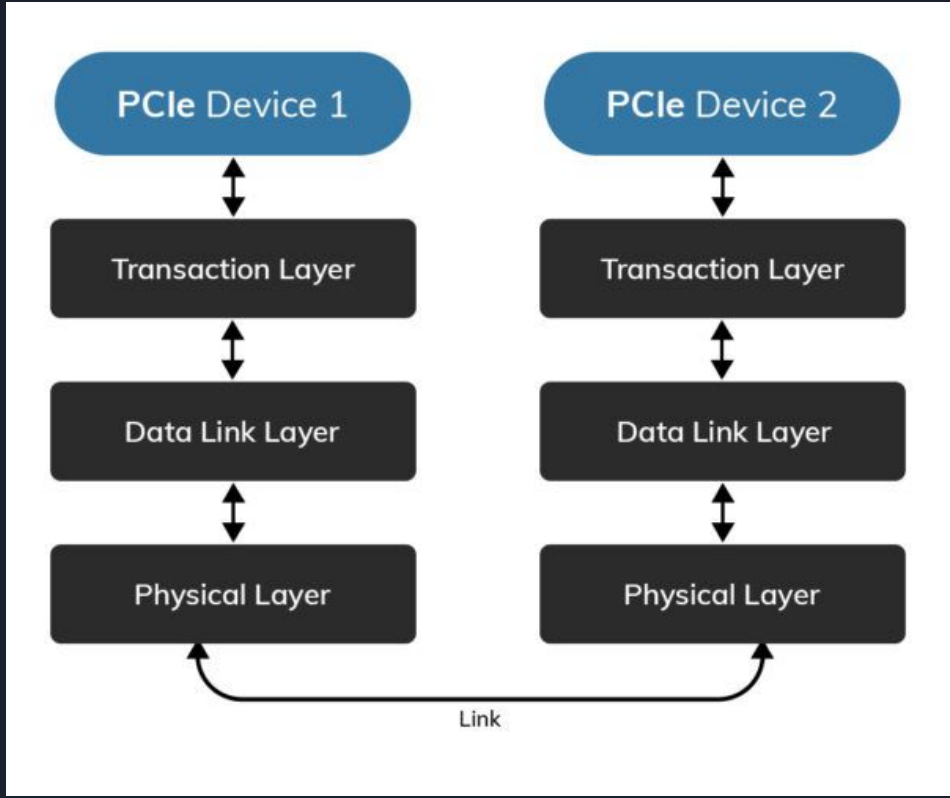
- Eine schnelle interne Schnittstelle für Erweiterungskarten in Computer-Systemen.
- Beschreibt Software-Protokoll, elektrische und mechanische Eigenschaften der Steckverbinder und Erweiterungskarten.



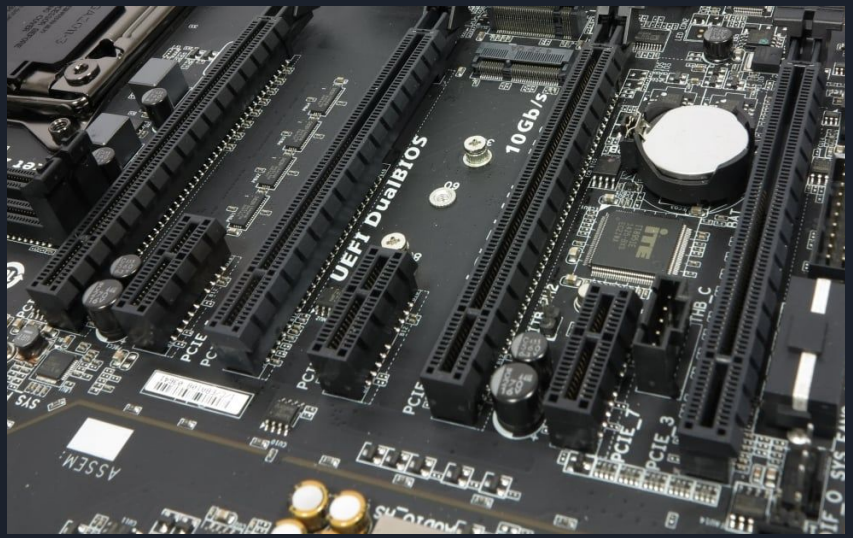
Architektur

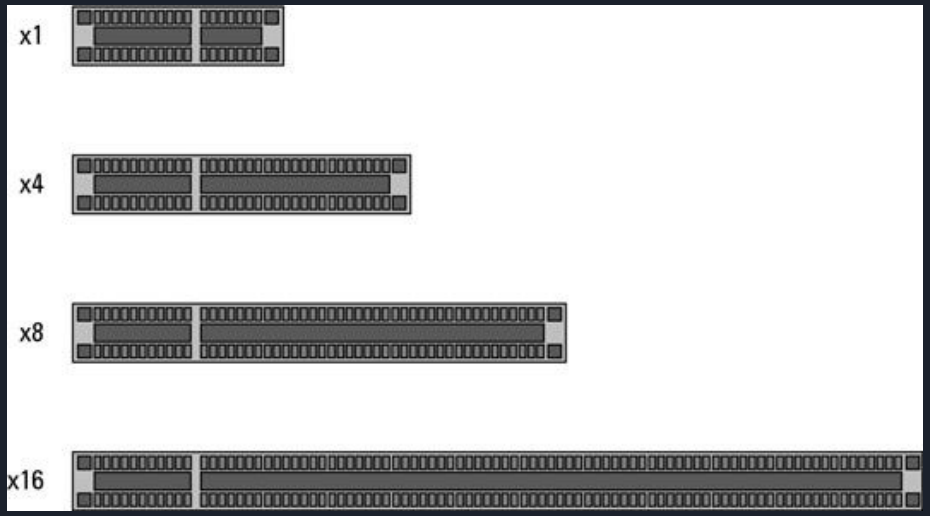


Layers


PCIe Device 1
PCIe Device 2
Transaction Layer
Transaction Layer
Data Link Layer
Data Link Layer
Physical Layer
Physical Layer
Link

Physical layer - Anschluss



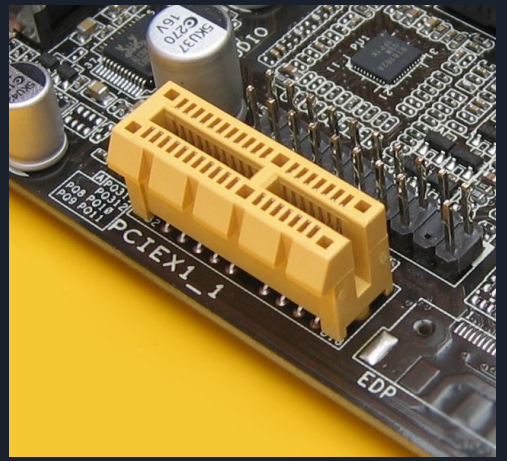


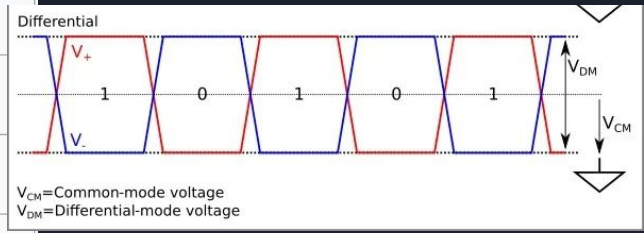
Physical layer

Pin	Side B	Side A	Description
1	+12 V	PRSNT1#	Must connect to farthest PRSNT2# pin
2	+12 V	+12 V	Main power pins
3	+12 V	+12 V	
4	Ground	Ground	
5	SMCLK	TCK	SMBus and JTAG port pins
6	SMDAT	TDI	
7	Ground	TDO	
8	+3.3 V	TMS	
9	TRST#	+3.3 V	
10	+3.3 V aux	+3.3 V	Aux power & Standby power
11	WAKE#	PERST#	Link reactivation; fundamental reset [24]
Key notch			
12	CLKREQ#[25]	Ground	Clock Request Signal
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK−	Lane 0 transmit data, + and −
15	HSOn(0)	Ground	
16	Ground	HSIp(0)	Lane 0 receive data, + and −
17	PRSNT2#	HSIn(0)	
18	Ground	Ground	
PCI Express x1 cards end at pin 18			

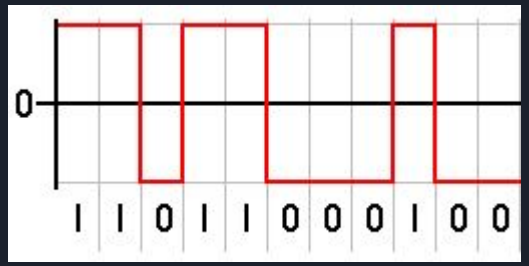
19	HSOp(1)	Reserved	Lane 1 transmit data, + and −
20	HSOn(1)	Ground	
21	Ground	HSIp(1)	Lane 1 receive data, + and −
22	Ground	HSIn(1)	
23	HSOp(2)	Ground	Lane 2 transmit data, + and −
24	HSOn(2)	Ground	
25	Ground	HSIp(2)	Lane 2 receive data, + and −
26	Ground	HSIn(2)	
27	HSOp(3)	Ground	Lane 3 transmit data, + and −
28	HSOn(3)	Ground	
29	Ground	HSIp(3)	Lane 3 receive data, + and −
30	PWRBRK#[26]	HSIn(3)	
31	PRSNT2#	Ground	
32	Ground	Reserved	
PCI Express x4 cards end at pin 32			

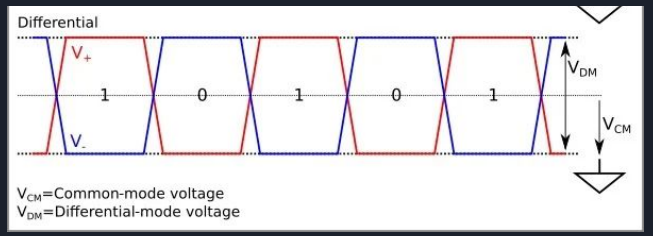
Ground pin	Zero volt reference
Power pin	Supplies power to the PCIe card
Card-to-host pin	Signal from the card to the motherboard
Host-to-card pin	Signal from the motherboard to the card





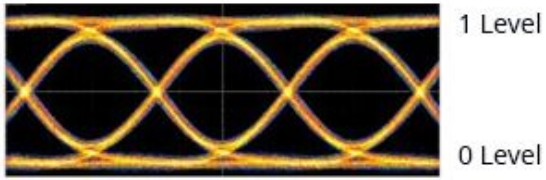
Datenübertragung



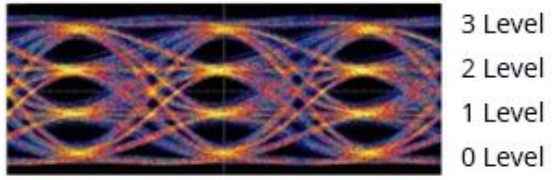


Version	Intro-duced	Line code		Transfer rate per lane[i][ii]	Throughput[i][iii]				
					x1	x2	x4	x8	x16
1.0	2003	NRZ	8b/10b	2.5 GT/s	0.250 GB/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s
2.0	2007			5.0 GT/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s	8.000 GB/s
3.0	2010		128b/130b	8.0 GT/s	0.985 GB/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s
4.0	2017			16.0 GT/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s
5.0	2019			32.0 GT/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s	63.015 GB/s
6.0	2022	PAM-4 FEC	242B/256B FLIT	64.0 GT/s 32.0 GBd	7.563 GB/s	15.125 GB/s	30.250 GB/s	60.500 GB/s	121.000 GB/s
7.0	2025 (planned)			128.0 GT/s 64.0 GBd	15.125 GB/s	30.250 GB/s	60.500 GB/s	121.000 GB/s	242.000 GB/s

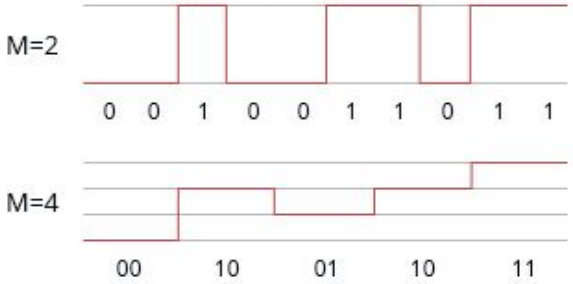
Datenübertragung



NRZ: 1 bit per clock cycle

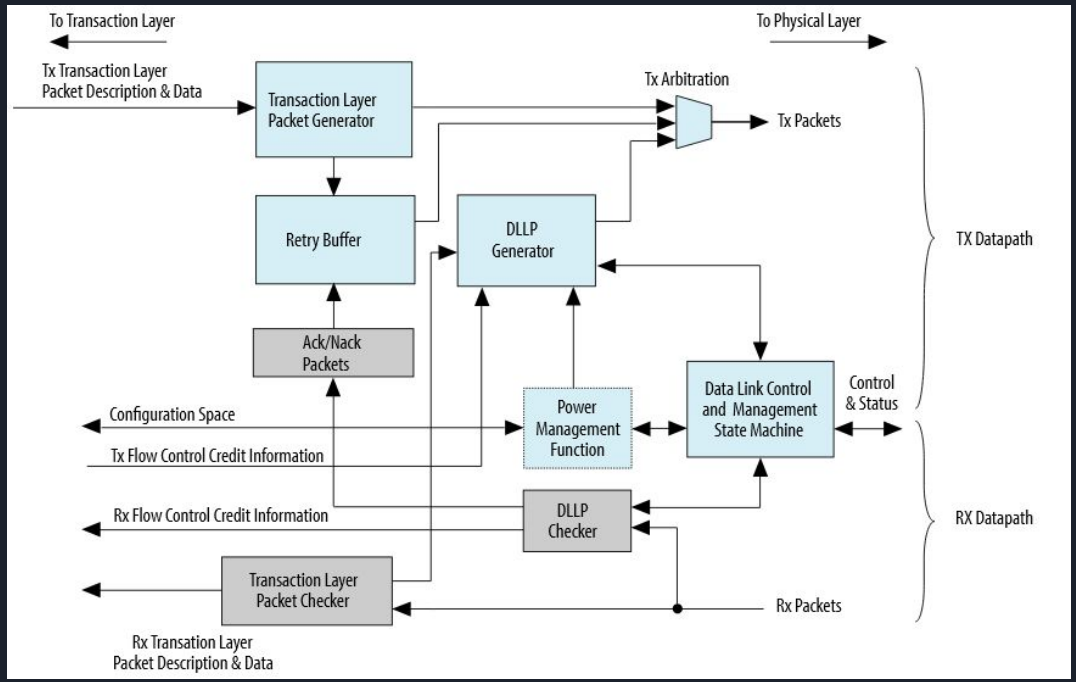


PAM4: 2 bits per clock cycle

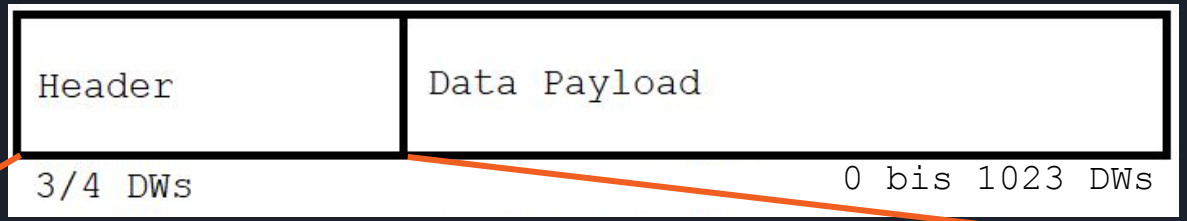


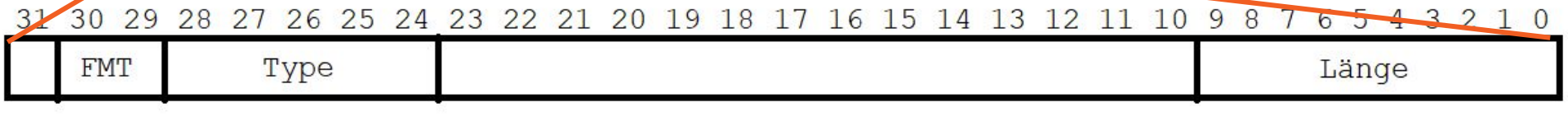
Data link layer

- Reihenfolge der TLP(Transaction Layer Packages) festlegen
- Korrekte Übertragung der Daten sicherstellen (Id Tags und Prüfsumme)
- Eigene Pakete verschicken und Interpretieren (DLLP = Data Link Layer Packages)



Transaction layer





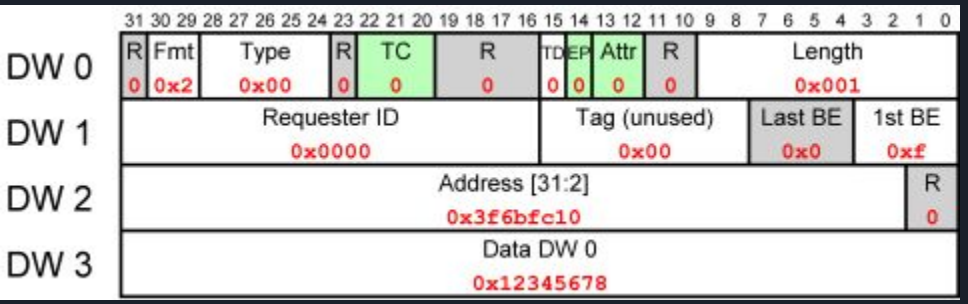
erstes DW des Headers

FMT	TLP Format
00	3 DW header, keine Daten
01	4 DW header, keine Daten
10	3 DW header, mit Daten
11	4 DW header, mit Daten

DW: Double Word -> 32 Bit

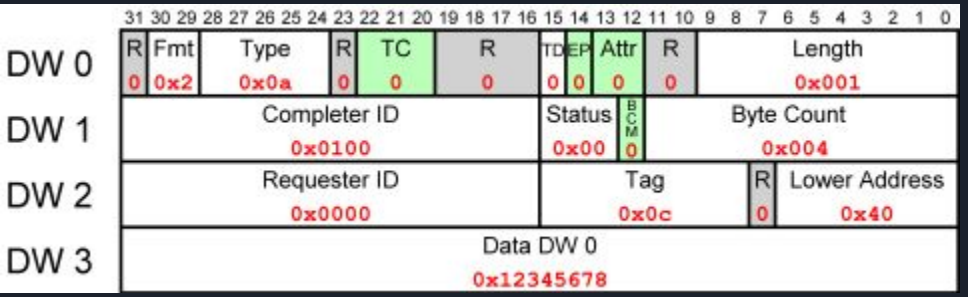
Transaction layer

FMT	TLP Format
00	3 DW header, keine Daten
01	4 DW header, keine Daten
10	3 DW header, mit Daten
11	4 DW header, mit Daten



Write Packet

0x40000001
0x0000000f
0xfdaff040
0x12345678



Completion TLP

0x4a000001
0x01000004
0x00000c00
0x12345678

Danke fürs Zuhören

Quellen

- https://www.elektronik-kompendium.de/sites/com/0904051.htm
- http://picmg.mil-embedded.com/articles/pci-express-protocol-primer/
- https://www.youtube.com/watch?v=sRx2YLzBIqk
- https://upload.wikimedia.org/wikipedia/commons/a/a3/PCIe_J1900_SoC_ITX_Mainboard_IMG_1820.JPG
- https://www.fpga4fun.com/PCI-Express4.html
- https://marvel-b1-cdn.bc0a.com/f00000000283630/samtec-cdn.azureedge.net/kineticimages/images/mackdaddy-familypages/pci-express/pci_macdaddy_mobile_header.jpg
- https://www.thomas-krenn.com/de/wikiDE/images/1/12/PCIe-Slots-Abmessungen-sind-versionsunabhaengig.jpg
- https://assets.reedpopcdn.com/digitalfoundry-best-graphics-card-every-amd-nvidia-tested-7001-1587745896837.jpg/BROK/thumbnail/1600x900/quality/100/digitalfoundry-best-graphics-card-every-amd-nvidia-tested-7001-1587745896837.jpg
- https://help.elgato.com/hc/article_attachments/360091950052/291549.image0.jpg
- https://tu-dresden.de/ing/informatik/ti/vlsi/ressourcen/dateien/dateien_studium/dateien_lehstuhlseminar/vortraege_lehrstuhlseminar/folder-2011-04-14-7861139448/pcie.pdf?lang=de
- https://prodigytechno.com/wp-content/uploads/2021/11/Fig-3-600x585-1.jpg
- https://www.pcgameshardware.de/screenshots/original/2017/02/Detail_Gigabyte_Erweiterung-pcgh.JPG
- https://de.wikipedia.org/wiki/PCI_Express