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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute)

Affiliated to Dr. A.P. J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow

Course - B.Tech

Branch- CSE/

Semester- 3rd

Second Sessional Examination

Year- (2021 - 2022)

Subject Name: DIGITAL LOGIC & CIRCUIT DESIGN

Time: 1.15Hours

[SET- A]

Max. Marks:30

General Instructions:

- This Question paper consists ofpages &questions. It comprises of three Sections, A, B, and C
- **Section A** - Question No- 1 is objective type questions carrying 1 mark each, Question No- 2 is very short answer type carrying 2 mark each. You are expected to answer them as directed.
- **Section B** - Question No-3 is Short answer type questions carrying 5 marks each. Attempt any two out of three questions given.
- **Section C** - Question No. 4 & 5 are Long answer type (within unit choice) questions carrying 6 marks each. Attempt any one part a or b.

		<u>SECTION – A</u>	[08Marks]																										
1.	All questions are compulsory		(4×1=4)																										
	a.	<div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"> AB CD </div> <table border="1"> <tr> <td></td><td>00</td><td>01</td><td>11</td><td>10</td></tr> <tr> <td>00</td><td align="center">0</td><td></td><td align="center">0</td><td align="center">0</td></tr> <tr> <td>01</td><td align="center">0</td><td></td><td align="center">0</td><td align="center">0</td></tr> <tr> <td>11</td><td align="center">0</td><td></td><td align="center">0</td><td align="center">0</td></tr> <tr> <td>10</td><td align="center">0</td><td></td><td align="center">0</td><td align="center">0</td></tr> </table> </div> <p>The minimised expression for the given K-map is (See Fig.) (a) $A'(A + B)$ (b) $A' + B A$ (c) $A'B$ (d) None of these</p>		00	01	11	10	00	0		0	0	01	0		0	0	11	0		0	0	10	0		0	0	(1)	CO1
	00	01	11	10																									
00	0		0	0																									
01	0		0	0																									
11	0		0	0																									
10	0		0	0																									
	b.	A multiplexer with 3-bit data select input is a (a) 4 : 1 multiplexer (b) 8 : 1 multiplexer (c) 16 : 1 multiplexer (d) 32 : 1 multiplexer	(1)	CO2																									
	c.	A full adder can be realised using (a) two half adder, two OR gates (b) two half adders, one OR gate (c) two half adders, two OR gates (d) none of these	(1)	CO2																									
	d.	In BCD addition, 0110 is required to be added to the sum for getting the correct result, if	(1)	CO2																									

	(a) the sum of two BCD numbers is not a valid BCD number (b) the sum of the two BCD numbers is not a valid BCD number or a carry is produced (c) a carry is produced (d) none of the above is true		
2.	All questions are compulsory	(2×2=4)	
a.	Realise a half adder using (i) NAND (ii) NOR gates only.	(2)	CO2
b.	What are the similarities and dissimilarities between decoder and Demultiplexer ?	(2)	CO2
SECTION – B		[10Marks]	
3.	Answer any <u>two</u> of the following-	(2×5=10)	
a.	Implement $F(A, B, C, D) = \sum m(0,1,2,4,6,9,12,14)$ using 4x1 multiplexer	(5)	CO2
b.	Implement and explain 1X 8 Demux using 1X 2 Demux only.	(5)	CO2
c.	Explain priority encoder by using example.	(5)	CO2
SECTION – C		[12Marks]	
4.	Answer any <u>one</u> of the following-	(1×6=6)	
a.	Minimize the function in SOP form: $F(A,B,C,D, E) = \sum m(0,1,3,4,6,15, 18, 22, 26,30) + d(5,7,11,14,24,25)$	(6)	CO1
b.	Explain Boolean expression simplification techniques with example for each.	(6)	CO1
5.	Answer any <u>one</u> of the following-	(1×6=6)	
a.	What is magnitude Comparator? Design a 1 bit magnitude comparator.	(6)	CO2
b.	Explain the designing steps of combinational circuits and design a BCD adder.	(6)	CO2