Printed page: 2 Subject Code: ACSE0305

Roll No:

**NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA**

**(An Autonomous Institute)**

**Affiliated to Dr. A.P. J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow**

**Course: B.tech** **Branch: Computer Science & Engineering**

**Semester: III** **Sessional Examination: II** **Second Year- (2021- 2022)**

**Subject Name: Computer Organization & Architecture.**

**Time: 1.15Hours** **[ SET- B]** **Max. Marks:30**

**General Instructions:**

- This Question paper consists of .....pages & .....questions.It comprises of three Sections, A, B, and C
- Section A -Question No- 1 is objective type questions carrying 1 mark each, Question No- 2 is very short answer type carrying 2 mark each. You are expected to answer them as directed.
- Section B - Question No-3 is Short answer type questions carrying 5 marks each. Attempt any two out of three questions given.
- Section C -Question No. 4 &5are Long answer type (within unit choice) questions carrying 6marks each. Attempt any one part *a* or *b*.

| | | | | |
|---|---|---|---|---|
| | | **SECTION – A** | **[08Marks]** | |
| 1. | **All questions are compulsory** | | **(4×1=4)** | |
| | a. | **The sign magnitude representation of -9 is _____** | **(1)** | **CO2** |
| | b. | **In both signed magnitude and 2's complement , positive and negative numbers are separated using ____**<br>**i LSB ii MSB iii 0 iv 1** | **(1)** | **CO2** |
| | c. | **_____algorithm using excluding sign bit for multiplication.** | **(1)** | **CO2** |
| | d. | **For j multiplier and k multiplicand bits in array multiplier needs how many AND gates required.**<br>**i. j+k ii j x k iii (j-1) x k iv. None of these** | **(1)** | **CO2** |
| 2. | **All questions are compulsory** | | **(2×2=4)** | |
| | a. | **Write the initial value of Q Qn+1 AC QR Qn+1 SC for multiplication if BR=1011 & QR=1100** | **(2)** | **CO2** |
| | b. | **Explain ashr, shr and shl with suitable examples** | **(2)** | **CO2** |
| | | **SECTION – B** | **[10Marks]** | |
| 3. | **Answer any two of the following-** | | **(2×5=10)** | |
| | a. | **Explain flow diagram of signed magnitude algorithm.** | **(5)** | **CO2** |
| | b. | **Discuss Stack organization with suitable examples.** | **(5)** | **CO2** |
| | c. | **Perform the arithmetic shift micro-operation (ashr) after shift left micro-operation (shrl) of register R1=101010111.** | **(5)** | **CO2** |
| | | **SECTION – C** | **[12Marks]** | |
| 4 | **Answer any one of the following-** | | **(1×6=6)** | |
| | a. | **Explain the Relative addressing modes with suitable diagram.** | **(6)** | **CO2** |

| | | | | |
|---|---|---|---|---|
| | b. | Perform the multiplication -2 X 5 using Signed magnitude algorithm. | (6) | CO2 |
| 5. | Answer any <u>one</u> of the following- | | (1×6=6) | |
| | a. | Discuss the Array multiplier with 4bits multiplicand(b3b2b1b0 and multiplier(a2a1a0) . | (6) | CO2 |
| | b. | Sketch the flow diagram of Signed magnitude algorithm for multiplication. | (6) | CO2 |

**ALL THE BEST**