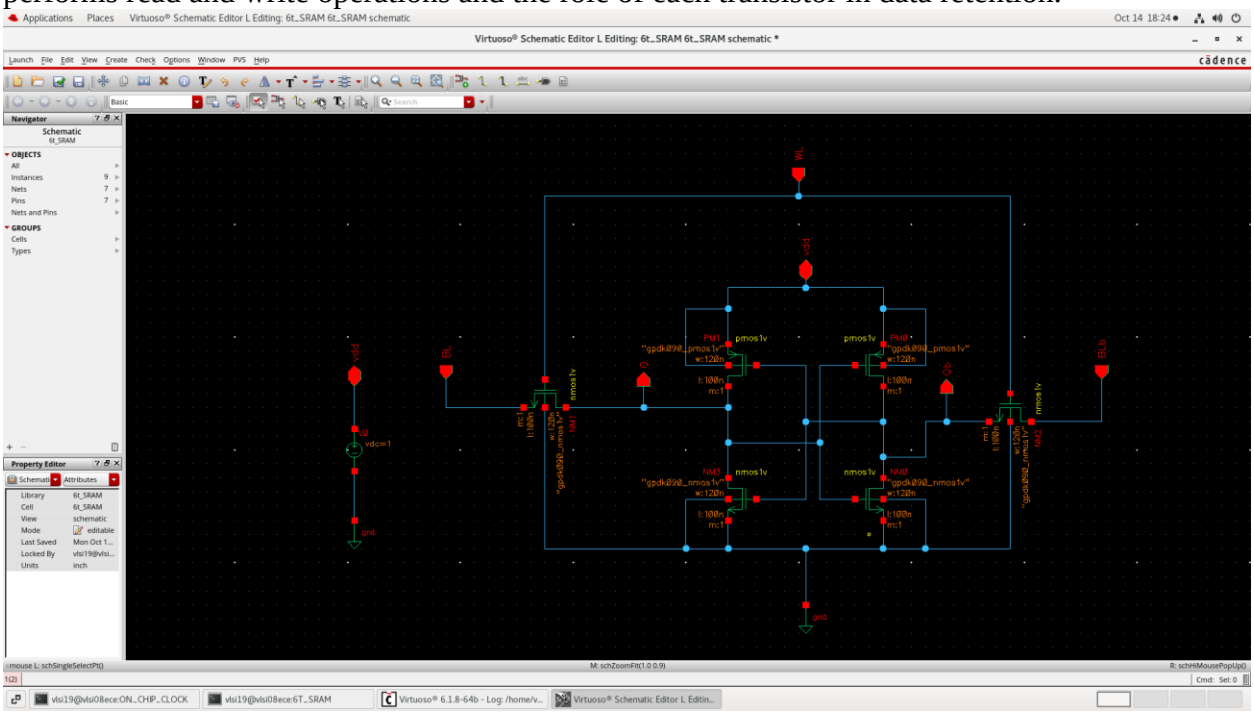
6T SRAM Cell

Objective:
To design a 6T SRAM cell and measure its characteristics, including stability, power consumption, and performance.

Circuit Description:
The 6T SRAM cell uses six transistors (two cross-coupled inverters and two access transistors) to store a single bit of data. The design focuses on read/write stability, power efficiency, and performance in memory applications.

Schematic:
The 6T SRAM cell schematic was created in 90 nm technology using Cadence Virtuoso. Describe how the cell performs read and write operations and the role of each transistor in data retention.

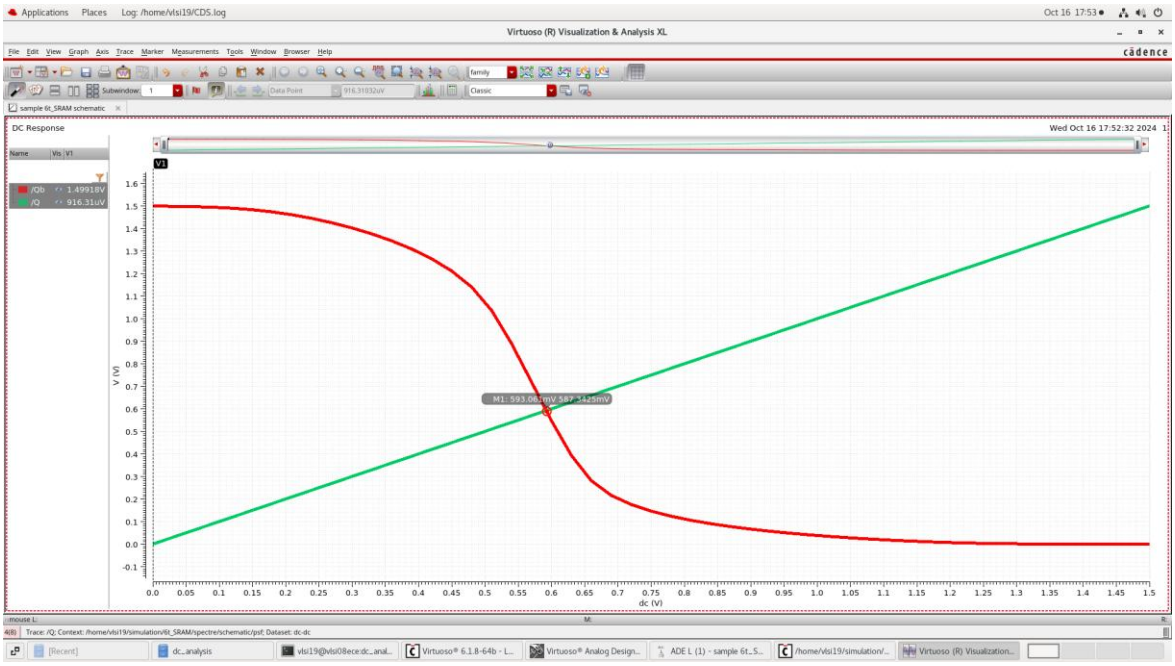


EDA Tool Setup:

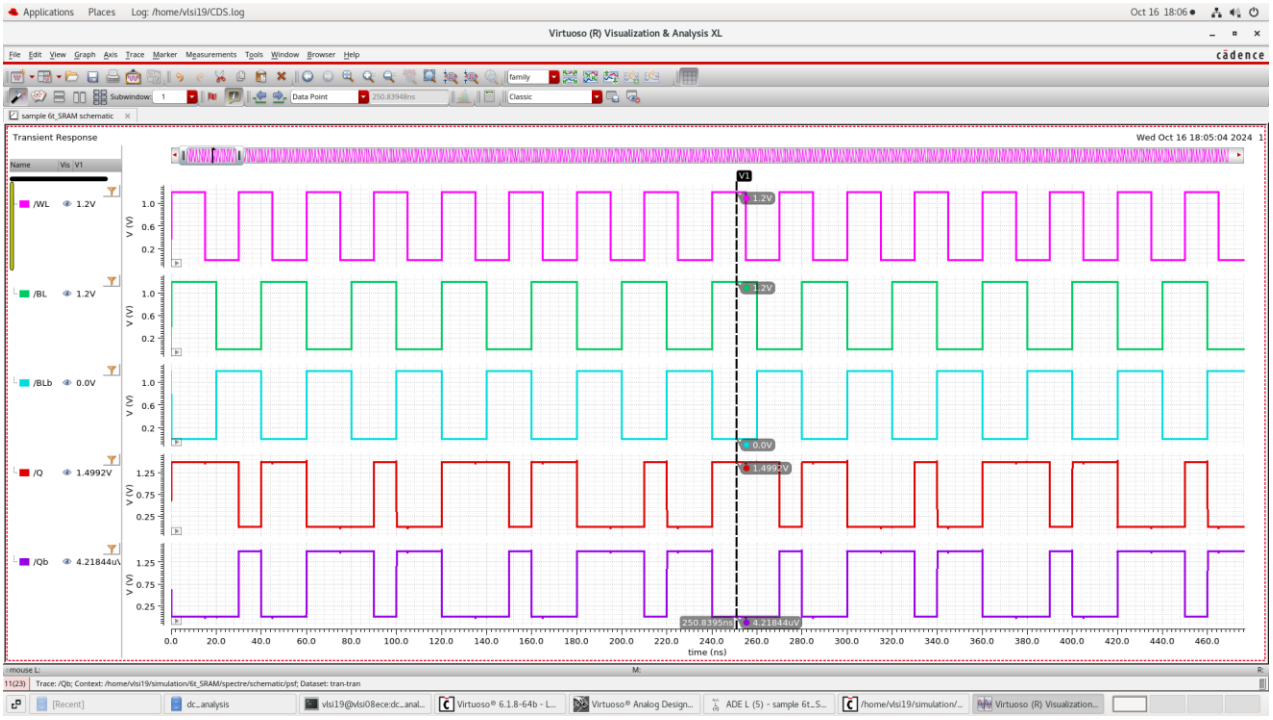
- **Schematic Creation**: Cadence Virtuoso in 90 nm technology.
- **Simulation**: ADL window for analyzing read and write operations, hold.
- **PVT Analysis**: ADL XL using 180 nm and 65 nm process parameters to test stability and performance. Making all transistor width parameter as Wn for Nmos and Wp for Pmos.

Experimental Results:

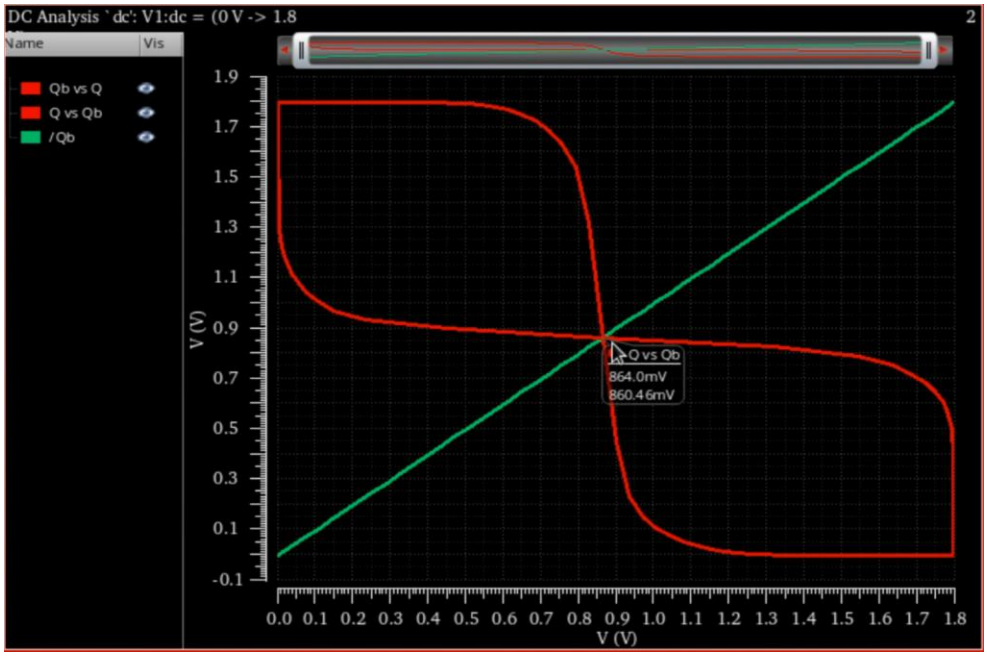
1. **DC Response**:

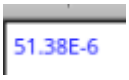


2. **Transient Response**:

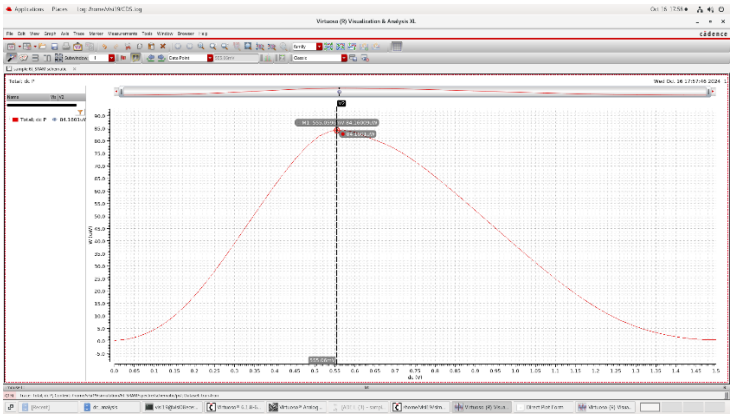


3. **Noise Margine- BUTTERFLY CURVE**

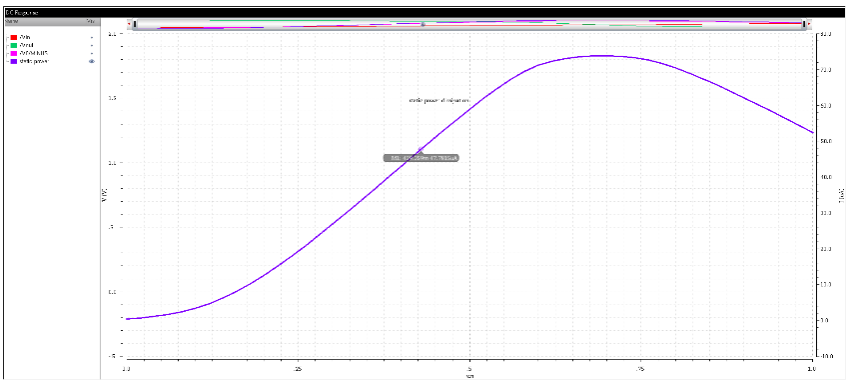


4. **Power Dissipation**: Pdyanmic = 51.3e-6, 

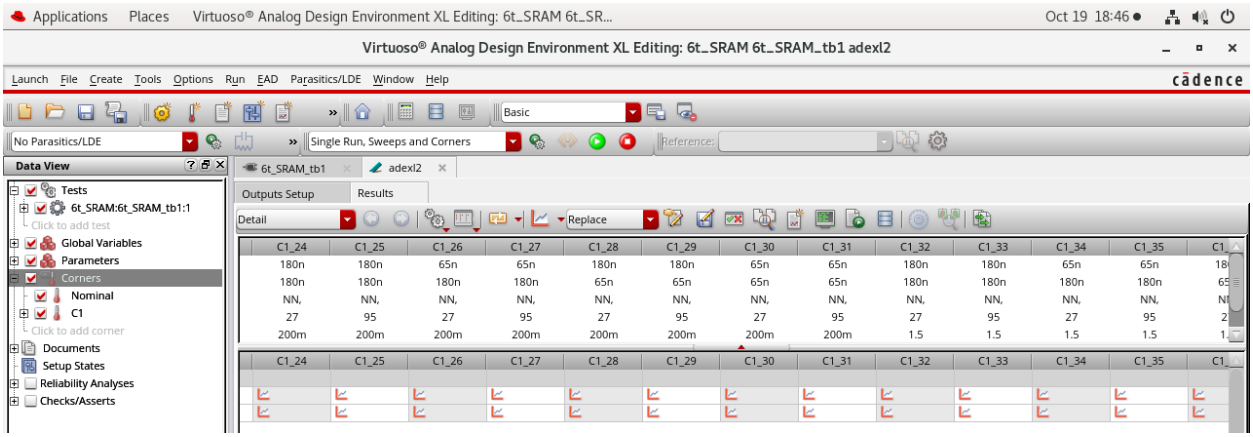
dynamic Power Dissipation of CMOS:

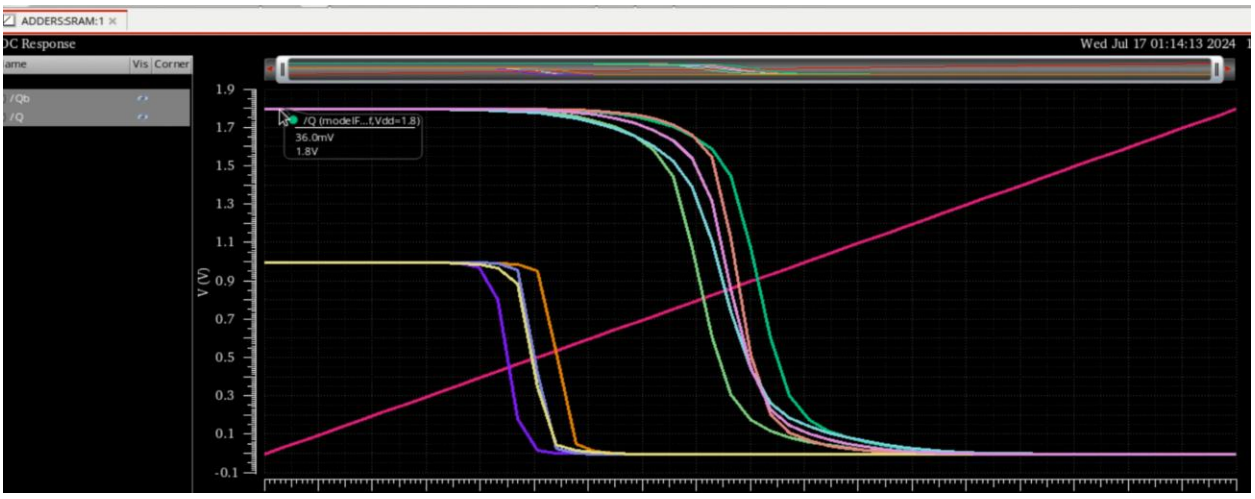


Static Power Dissipation of CMOS:



5. **delay**: 20.03E-9 20.3e-9
6. **PVT Analysis**:
   - Use 180 nm and 65 nm process parameters.
   - Evaluate the SRAM cell's stability under varying conditions.





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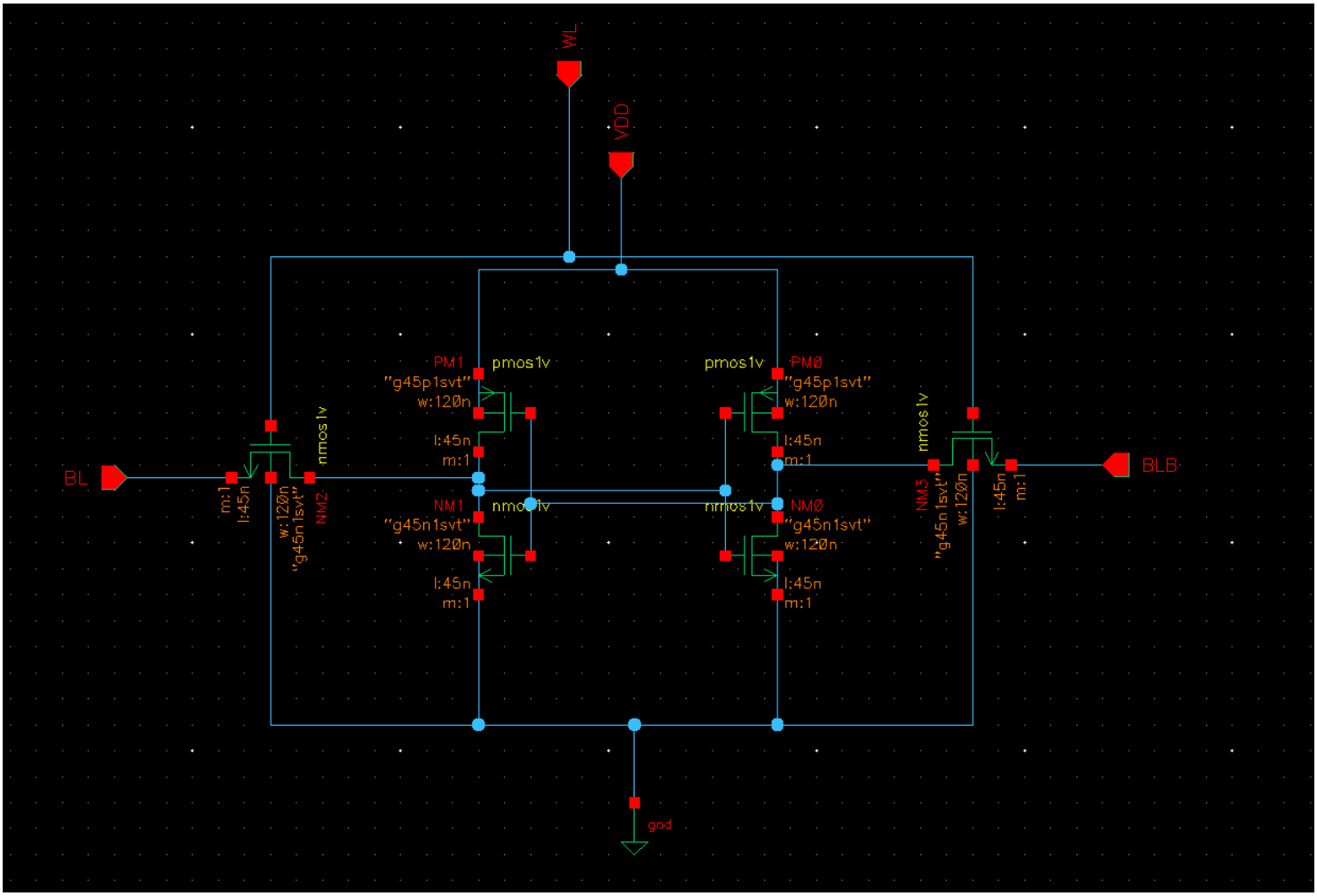
Observations:
The 6T SRAM cell was created in 90 nm technology, tested, and analyzed using Cadence software. The design successfully balances speed, power, and stability, with performance verified under PVT variations.

LAYOUT DESIGN –

Circuit design -



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Layout design -

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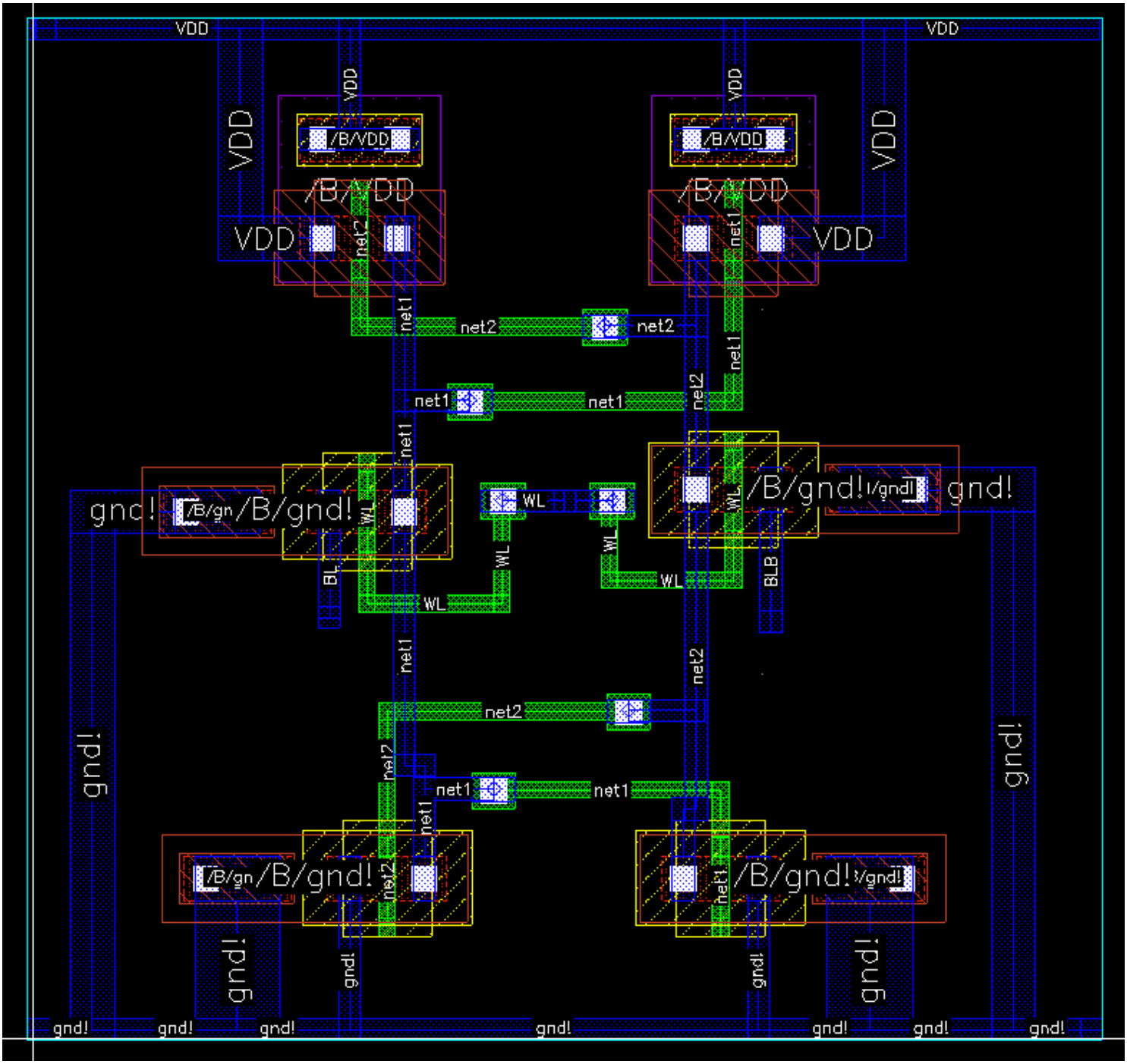

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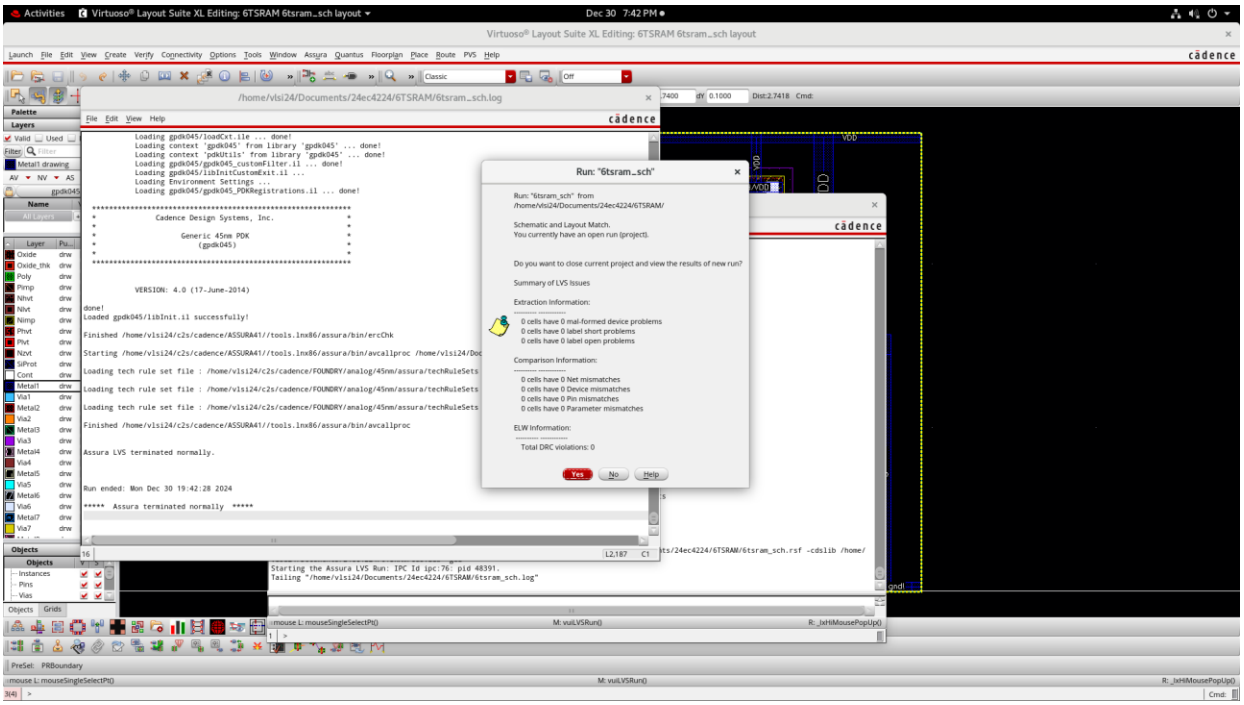
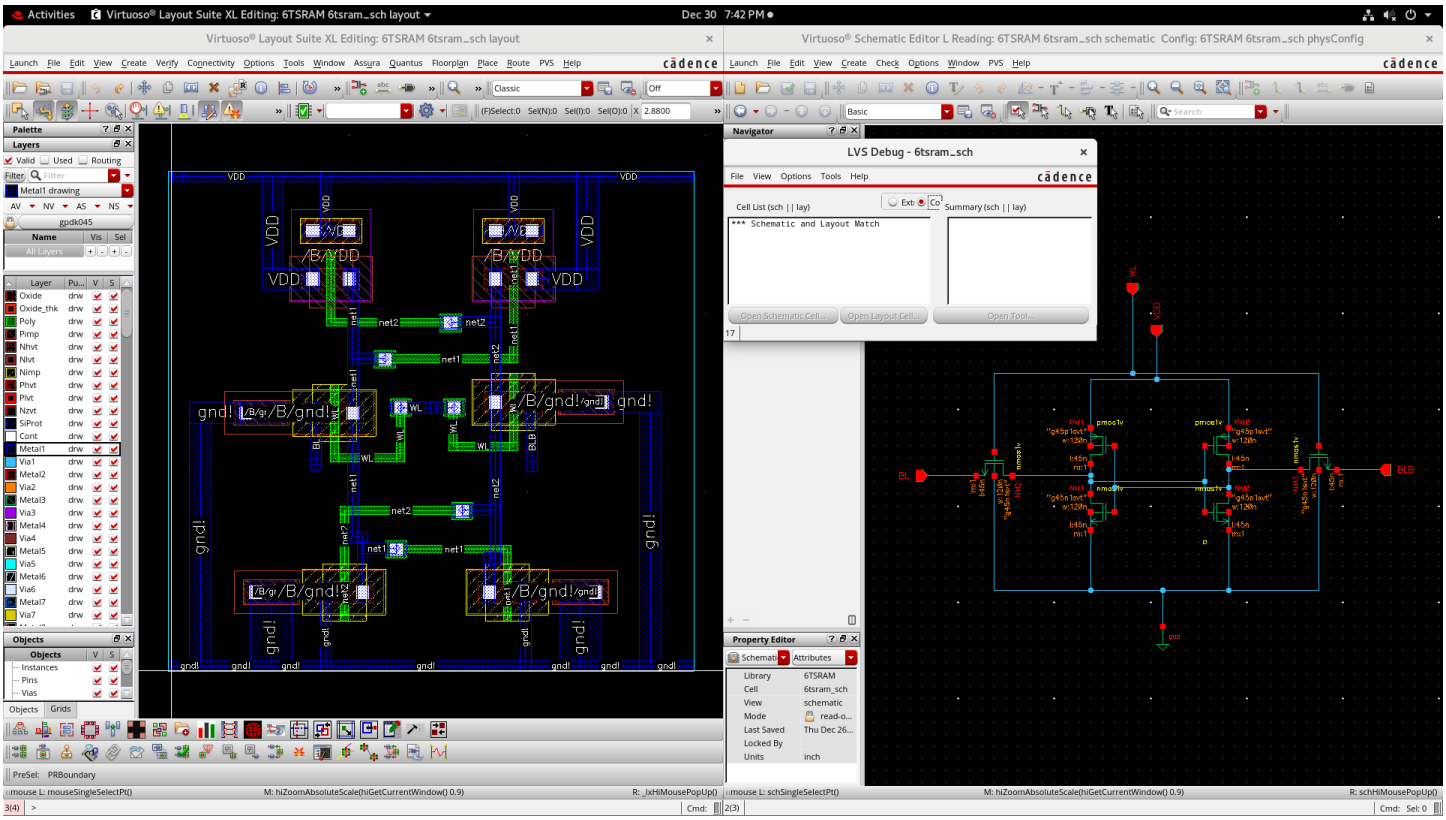
DRC AND LVS CHECK -





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