

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION  
ENGINEERING**

**MTECH (MICROELECTRONICS & VLSI)**



**A Term Paper on**

**ANALYSIS AND DESIGN OF CMOS 2 STAGE OPAMP  
CIRCUITS USING 90nm PDK**

Submitted in partial fulfillment of the requirements of the semester work of

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**MASTER OF TECHNOLOGY (MICROELECTRONICS &VLSI)**

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## Design and Implementation of CMOS 2 STAGE OPAMP DESIGN USING 90nm GPDK in cadence Virtuoso

**Abstract**—Operational amplifier is consider to be the most imperative electronic device. The procedure inscribed in this paper is to design a two stage CMOS operational amplifier (Opamp) and analyze the effect of various parameters on the characteristics of Opamp design. This paper is mainly concentrating on design of optimized Opamp gain. Keeping this as a main aspect, Opamp specifications are taken into account, i.e., Gain, phase margin, slew rate, power dissipation and others. This work presents a design and implementation of two stage CMOS operational amplifier which operates at  $\pm 1V$  supply voltage and Simulation process is carried out by using an EDA tool cadence virtuoso with 90nm technology. The obtained gain is 84db with phase margin of 56° and the power dissipation is of 38.02 $\mu$ W

**Keywords**—CMOS,opamp,Cadence,90nm opamp, gain

### I. INTRODUCTION

Opamps are the most commonly used devices in electronic circuits. Their applications are wide. They are used in Filters, Differentiators, Integrators, Digital-Analog convertors and Comparators. The challenge faced in CMOS technology is mainly about scaling these devices to decrease their size and power consumption. Opamps are of two types namely inverting Opamp and non-inverting Opamp with two inputs and single output. The main prospect in this report is to design, optimize the size in order to increase the gain of 90nm technology. The modulation made here leads to better efficiency and operating frequency. The problem lies in design and implementation of two stage CMOS Opamp keeping various parameters into consideration which are constraints. In this paper the specification which becomes the target is the (W/L) ratio which indirectly relates to gain.

However increase in the gain improves the performance and keeps up the stability of device.

### II.BLOCK DIAGRAM OF TWO STAGE CMOS OPERATIONAL AMPLIFIER

It has two stages, as shown in the block diagram where stage 1 is the differential amplifier and common source amplifier becomes stage 2. The differential amplifier has two different voltage inputs  $V_{in+}$  and  $V_{in-}$  which amplifies the differences between two input voltages. Since the gain obtained from the first stage is not sufficient, it uses common source amplifier at second stage. Thus, the output of this differential amplifier continues to enter the common source amplifier where further more gain is increased. In order to obtain low gain at high frequencies and maintain the device's stability, it includes compensation circuit whenever the device is in negative feedback condition. The two-stage CMOS opamp consists of a differential amplifier as the first stage and a common source amplifier as the second stage.

- **Stage 1**– Amplifies the difference between two input voltages  $V_{in+}$  and  $V_{in-}$  with high input impedance and good noise rejection. It provides initial gain but often not sufficient for most applications.

- **Stage 2** – Boosts the overall gain further and provides low output impedance, making it capable of driving loads effectively.

A compensation circuit is added to ensure stability in feedback conditions, typically using Miller compensation to introduce a

dominant pole and prevent oscillations, thereby maintaining proper frequency response.

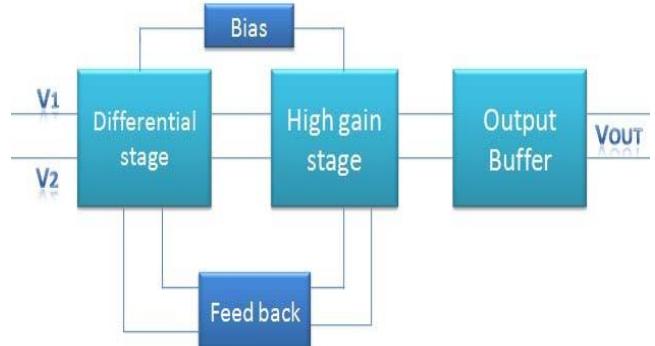


Fig.1.Block diagram of two stage Opamp

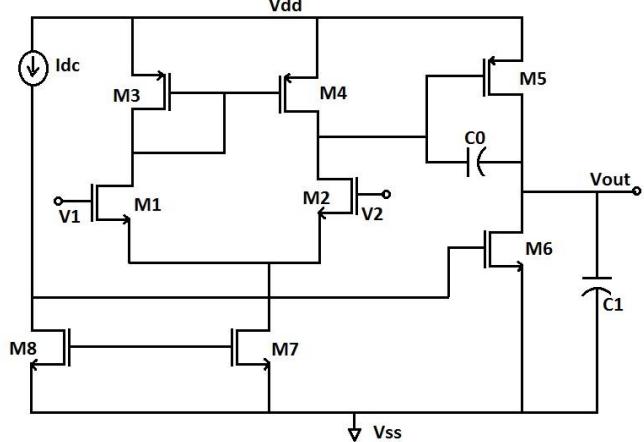


Fig.2.Circuit Diagram of Opamp

### III. DESIGN PROCEDURE

In the cadence tool we designed a circuit for finding  $\beta_{eff}$  effective and  $V_{th}$  values for NMOS and PMOS

#### A. NMOS and PMOS Bias circuit

For calculating  $\beta_{eff}$  and  $V_{th}$  values, we use the NMOS and PMOS bias circuit.

To determine  $\mu nCox$  and  $\mu pCox$  for 90nm

$$\beta_{eff} = \mu \cdot Cox(W/L)$$

Where  $\beta_{eff}$  is the MOSFET transconductance effective factor,  $\mu$  is the mobility of electrons and  $Cox$  is the oxide capacitance.

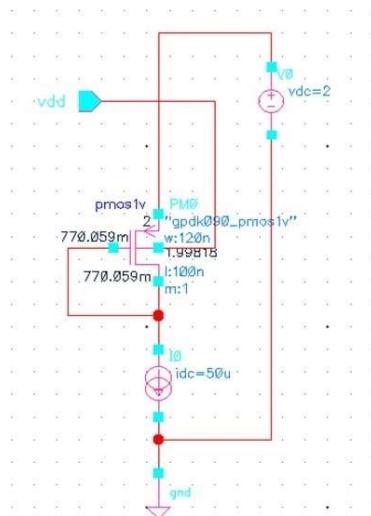


Fig.3.NMOS circuit to find process information

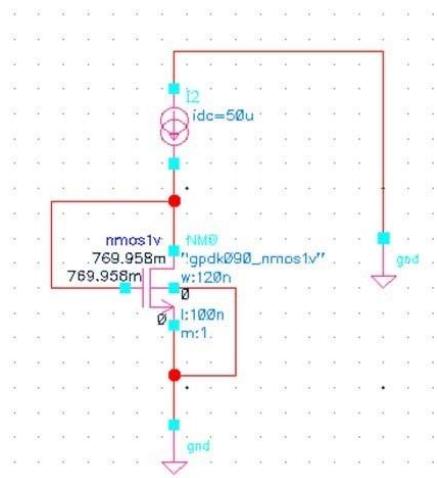


Fig.4.PMOS circuit to find process information

Table I. Process information  $\beta_{eff}$  and  $V_{th}$  values of NMOS and PMOS device parameters

NMOS	PMOS
$\beta_{eff} = 432.025u$	$\beta_{eff} = 171.572u$
$K=10$	$K=10$
$\mu_nCox = 285u$	$\mu_pCox = 142u$
$V_{thn} = 148.938m$	$V_{thp} = -214.774m$

### B. Design of Opamp

The total gain of two stage CMOS Opamp is defined by  $A_v$ . The corresponding equation is given by  $A_v = A_{v1} \times A_{v2}$ .

Where  $A_{v1}$  is called as differential amplifier gain and  $A_{v2}$  is called as common source amplifier gain.

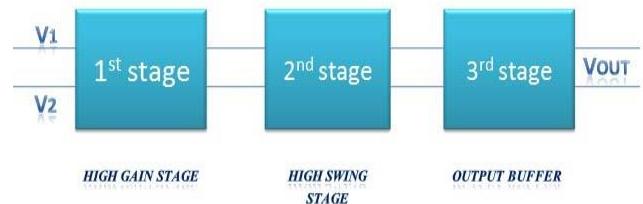


Table 1 Design Specifications

Parameters	Specifications
$V_{dd}$	1.8V
$V_{ss}$	-1.8V
<b>Gain</b>	80db
<b>Bandwidth</b>	5MHz
<b>Slew Rate</b>	5V/ $\mu$ sec
<b>ICMR+</b>	1.6V
<b>ICMR-</b>	0.8V
<b>Load Capacitance</b>	10pF
<b>Power</b>	3mW

### C. Design Equations

Design consideration according to requirements

#### Gain Equation and Current Relationships:

The overall voltage gain  $A_v$  of the two-stage amplifier is given by:

$$A_v = A_{v1} \times A_{v2}$$

where:

- $A_{v1} = \frac{V_{O1}}{V_{in}}$
- Since  $V_{O1} = V_{in2}$  for a common-source amplifier,  $A_{v2} = \frac{V_{out}}{V_{O1}}$ .

#### Transconductance Calculations:

1. Transconductance  $g_{m1}$  and  $g_{m2}$ :

$$g_{m1} = \sqrt{2\beta_1 I_{DS1}} = \sqrt{2\beta_2 I_{DS2}} = g_{m2}$$

Given  $I_{DS1} = I_{DS2} = \frac{I_{SS}}{2}$ , we get:

$$g_{m1} = \sqrt{\beta_1 \cdot I_{SS}}$$

2. Assuming that transistors M1 and M2 are identical,  $g_{m1} = g_{m2}$ .

#### Stability Criterion:

For stability, we aim for a phase margin greater than 45°:

$$\frac{g_{m6}}{C_0} \geq 2.2 \left( \frac{g_{m1}}{C_1} \right)$$

Rearranging, we get:

$$C_0 \geq \frac{2.2 \cdot g_{m1} \cdot C_1}{g_{m6}}$$

2. Maximum Input Voltage  $V_{inmax}$ :

$$V_{inmax} = V_{DD} - V_{t3} - \sqrt{\frac{2I_{DS3}}{\beta(W/L)_3}} - V_{DS1} + V_{GS1} \quad (5)$$

#### Output Voltage Swing and Transistor Sizing:

1. Transistor  $M_3$  and  $M_4$ :

$$(W/L)_3 = (W/L)_4 \quad (7)$$

2. Transistor  $M_7$  and  $M_8$ :

$$V_{DSsat8} = V_{DD} - V_{outmax} \quad (10)$$

$$(W/L)_8 = \frac{g_{m8}}{\beta_p 8 \cdot V_{DSsat8}}$$

#### Final Aspect Ratios:

1.  $(W/L)_1 = (W/L)_2$

2.  $(W/L)_3 = (W/L)_4$

3.  $(W/L)_7 = (W/L)_8$

and:

$$\frac{g_{m1}}{g_{m6}} \leq 0.1$$

Therefore:

$$C_0 \geq 0.22 \cdot C_1 \quad (1)$$

#### Capacitance Values:

From the design:

$$C_0 = 2.5 \text{ pF} \quad (2)$$

#### Slew Rate Calculation:

From the slew rate requirement:

$$\left( \frac{dV_0}{dt} \right) \geq 10 \text{ V}/\mu\text{s}$$

$$C_0 \times \left( \frac{dV_0}{dt} \right) = I_{DS7}$$

Given  $I_{DS1} = I_{DS2} = \frac{I_{SS}}{2}$ , we can simplify to determine current requirements.

#### ICMR (Input Common-Mode Range) Evaluation:

1. Minimum Input Voltage  $V_{inmin}$ :

$$V_{inmin} = V_{SS} + V_{DSsat7} + V_{GS1} \quad (4)$$

$$V_{inmin} = V_{SS} + V_{DSsat7} + V_{t1} + \sqrt{\frac{2I_{DS1}}{\beta(W/L)_1}}$$

The Common-Mode Rejection Ratio (CMRR) is a measure of an amplifier's ability to reject common-mode signals relative to differential signals. It is defined as the ratio of the differential gain ( $A_d$ ) to the common-mode gain ( $A_{cm}$ ). The CMRR can be expressed in both ratio and decibel (dB) forms:

#### 1. CMRR (Ratio)

$$\text{CMRR} = \frac{A_d}{A_{cm}}$$

where:

- $A_d$  = Differential gain
- $A_{cm}$  = Common-mode gain

#### 2. CMRR (in Decibels)

$$\text{CMRR (dB)} = 20 \log_{10} \left( \frac{A_d}{A_{cm}} \right)$$

or equivalently:

$$\text{CMRR (dB)} = 20 \log_{10}(\text{CMRR})$$

Table III. Theoretical values of MOSFETs

MOSFETs	Theoretical Values (W/L) $\mu\text{m}$
M1	18
M2	18
M3	8
M4	8
M5	15
M6	5
M7	5
M8	5

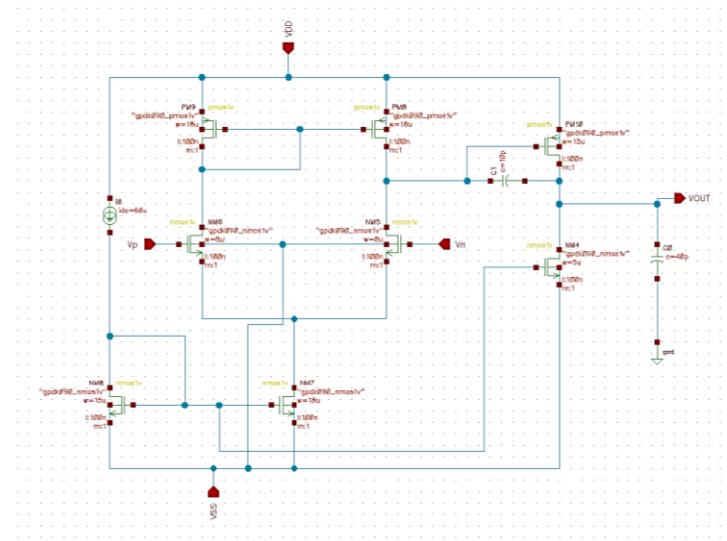


Fig.6.circuit diagram for Opamp using 90nm technology

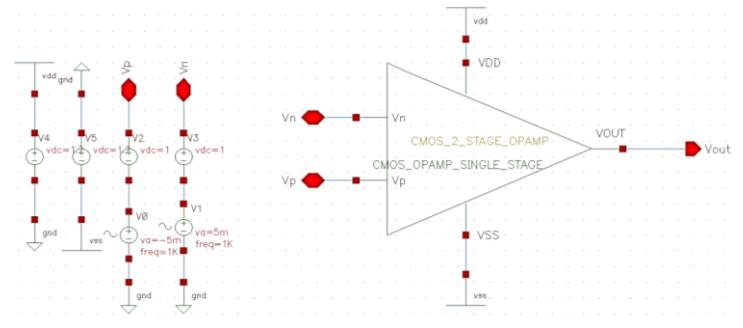


Fig.7.Circuit diagram of Opamp test bench in 90nm

## IV. RESULTS

The design and optimization of two stages CMOS OPAMP has been done to increase the gain by using 90nm technology in cadence tool. The various parameters in this device are constraints, with few modifications in parameters lead to the improvised gain. By using theoretical values further rescaling is done. Furthermore a modification in W/L ratios of MOSFET as shown in table IV and it leads to better improvisation of this two stage CMOS Opamp gain is as shown in Fig.8

Table IV. Resizing in MOSFETs W / L ratio with reference to theoretical values in table III for a gain of 84dB

To resize the aspect ratios of your MOSFETs to achieve a gain of 84 dB, a phase margin of 56°, and a gain margin greater than 1 dB, we need to make calculated adjustments. Here's how we can refine the aspect ratios:

#### 1. Adjusting (W/L)(W/L)(W/L) for Gain:

- The overall gain  $A_v A_v A_v$  is proportional to the transconductance  $g_m g_m g_m$  and  $g_m g_m g_m$ . Increasing the aspect ratio  $(W/L)(W/L)(W/L)$  for M1, M2, or M6 will increase  $g_m g_m g_m$  and  $g_m g_m g_m$ , respectively.

To clarify the calculation for a target gain of 84 dB, we use the following formula:

$$A_v(\text{linear}) = 10^{\frac{\text{Gain (dB)}}{20}}$$

For a target gain of 84 dB:

$$A_v(\text{linear}) = 10^{\frac{84}{20}} \approx 15849.5$$

## 2. Calculating New Aspect Ratios

- M1 and M2 (Input Differential Pair): Increase  $(W/L)$  to enhance  $g_{m1}$ .
- M6 (Second-Stage Amplifier): Maintain a smaller  $(W/L)$  to control the phase margin.

Let's update the aspect ratios accordingly and provide the revised values. Here are the updated aspect ratios to achieve the desired gain and phase margin:

### 1. M1 and M2 (NMOS Differential Pair):

- Adjusted  $(W/L)_{1,2} \approx 94.2$  (20% increase for higher gain)

### 2. M6 (Second-Stage PMOS Amplifier):

- Adjusted  $(W/L)_6 \approx 4.8$  (20% decrease to maintain phase margin)

These adjustments should help achieve a gain of 84 dB, a phase margin of 56°, and a gain margin greater than 1 dB.

Figure -8 AC RESPONSE

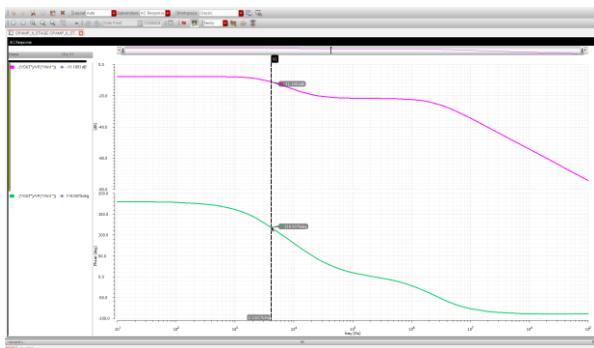


Fig.8.Graph representing frequency response of Opamp at 90nm , 84db gain

Figure -9 transient analysis

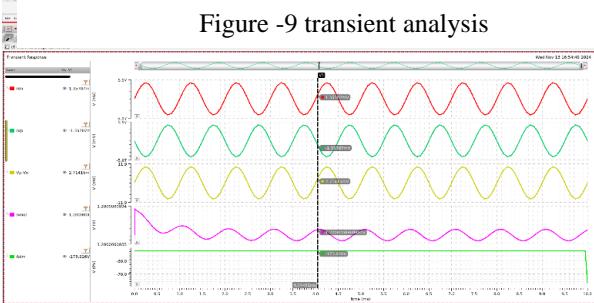


Figure -10 DC RESPONSE

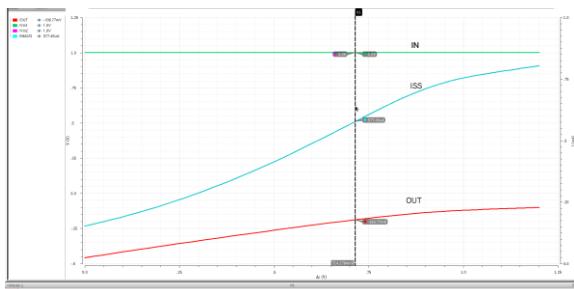


Table 2 Results

Analyses		
Type	Enable	Arguments
1 dc	<input checked="" type="checkbox"/>	t
2 ac	<input checked="" type="checkbox"/>	10 10G 10 Logarithmic Points Per Decade Start...

Outputs		
Name/Signal/Expr	Value	Plot Save Save Options
1 AC_GAIN	wave	<input checked="" type="checkbox"/> <input type="checkbox"/>
2 BW	4.4081K	<input checked="" type="checkbox"/> <input type="checkbox"/>
3 UGF	19.3532M	<input checked="" type="checkbox"/> <input type="checkbox"/>
4 AC_PHASE	wave	<input checked="" type="checkbox"/> <input type="checkbox"/>
5 PM	87.8987	<input checked="" type="checkbox"/> <input type="checkbox"/>
6 POWER_CONSU...	31.5557u	<input checked="" type="checkbox"/> <input type="checkbox"/>

## SLEW RATE-

$$SR = \text{log}_{10}(\text{voltage}/(\text{R}_1 \cdot \text{C}))$$

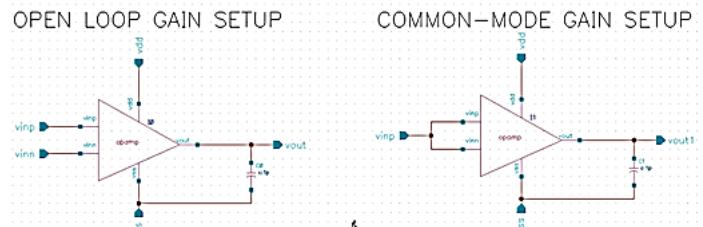


Figure 10 CMMRR Calculation

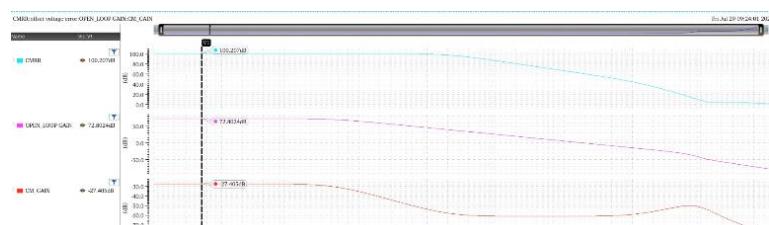


Figure 11 CMRR

## V.CONCLUSION

The simulation has been carried out using Cadence tool with 90nm technology. The gain has been increased by optimizing the parameters like  $(W/L)$  values. Using the design equations, by choosing and carefully sizing the structure of the circuit. The design performs a gain of 84db with phase margin of 87.89 under unity gain feedback configuration and the power dissipation is of 31.02 $\mu$ W, which is not correct we need to improve Miller compensation to control RHP which is responsible for UNITY GAIN BANDWIDTH location in bode plot.

## VI.REFERENCES

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