Low-Power Bidirectional Voltage Level Shifter for Wide Voltage Range Applications

***Abstract*— Voltage level shifters play a vital role in enabling intercommunication between circuit modules operating at different voltage domains, especially in modern VLSI systems. As advances in VLSI technology reduce silicon area and enhance performance, minimizing power consumption remains crucial for extending battery life in handheld devices. This paper presents an efficient single-supply, wide voltage range level shifter optimized for low-voltage operation. The proposed circuit can shift input signal levels from low to high or vice versa, effectively covering the full core supply voltage range (0.6 V to 1.8 V). Post-simulation results demonstrate that the proposed design achieves a 5× reduction in delay compared to existing level shifters, with a trade-off in power dissipation, measured in the micro-watt range. The basic layout has been designed and verified, confirming the feasibility of the proposed approach.**

Keyword- single supply voltage, dual supply typical voltage range level shifter, single supply wide voltage range level shifter, bidirectional level shifter, high-low threshold voltage device.

I. INTRODUCTION

To address the continuously increasing need for reduced power usage, and better performance. To make this possible, today's SoC designs usually include several sections, called voltage islands that run at different voltage levels. This approach optimizes the speed-to-power ratio and has become an established technique for efficient power management. A key component in this context is the level shifter circuit, which facilitates signal interfacing between circuits operating at different supply voltage domains.

A very effective way to cut down power use in digital LSI circuits is by reducing the supply voltage. As power dissipation is quadratically dependent on supply voltage. Level shifters are important circuits that connect low core voltage parts to areas with higher input-output voltage, particularly in very large-scale integration (VLSI) systems where both dynamic and static power dissipation need to be addressed. Dynamic power loss mainly happens when load capacitors charge and discharge, while static power loss is caused by leakage currents. Lowering the supply voltage and reducing capacitance can help decrease both types of power loss.

Voltage level shifters are important for allowing circuits with different voltage levels to work together and exchange signals. These components convert signal levels from one voltage domain to another, enabling seamless interaction between circuits with varying supply voltages. This project aims to develop an improved level shifter design that effectively reduces silicon area and optimizes power consumption. The focus is on creating multi-output high-voltage level shifters, specifically designed using Virtuoso for 90nm technology.

II. LITERATURE REVIEW

One big challenge in designing multi-supply circuits is keeping the cost of converting between different voltage levels low, while still making sure the system stays reliable. To solve this, LS circuits are very important.

In low-voltage large-scale integration (LSI) systems, subthreshold digital LSIs are often combined with regular circuits that run at higher supply voltages. Level shifter circuits facilitate seamless communication between these circuits. Additionally Level shifters are essential components that enable communication between different voltage domains within integrated circuits. They are particularly important in low-power and subthreshold digital circuits, where operating voltages are significantly reduced to minimize power consumption. In such scenarios, level shifters ensure signal integrity and compatibility across various parts of the system.

Voltage differences between domains can result in unreliable operation of the destination domain. To address this issue, level shifter cells are strategically placed at voltage domain interfaces. An example block diagram illustrating a conventional LS with multiple voltage domains (VDD cores) is shown in Fig. 1.

In the conventional LS setup with multiple VDD cores, two distinct supply voltages (VDDL and VDDH) are utilized, corresponding to core 1 and core 2, respectively. Routing wires for dual VDDs can be challenging, especially when cores are situated far apart, leading to issues such as routing congestion and increased parasitic capacitance. This, in turn, can cause signal degradation and routing inefficiency, which becomes more pronounced as voltage domains and cores proliferate in SoC architectures.

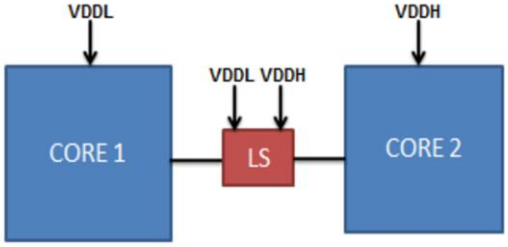

Fig. 1. block diagram of multi supply LS

Figure 2 shows the block diagram of a level shifter that uses a single supply voltage that utilizes a single supply voltage (VDDH) to perform an upward level shift. This design approach effectively reduces routing congestion, parasitic capacitance, and area penalties, making it suitable for multi-VDD systems and SoCs. One of the primary challenges in such systems is identifying efficient level shifters.

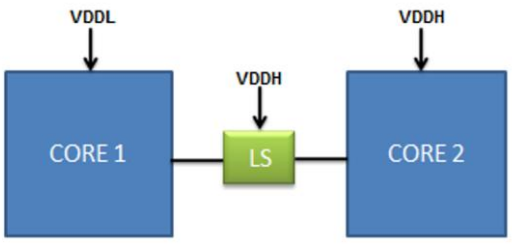

Fig. 2.block diagram of single supply LS

However, ensuring reliable communication and functional testing becomes challenging when conventional level shifter circuits are employed. This difficulty arises because subthreshold digital circuits often operate at very low supply voltages (below 0.5 V), while peripheral circuits (such as I/O circuits) typically function at significantly higher voltages, like 3.3 V. The main issue is that the drive current of low-voltage signals decreases considerably when the supply voltage is reduced, making it difficult for conventional level shifters to effectively convert IN_LOW signals to high and IN_HIGH signals to low signals.

To overcome this problem, several architectures and techniques for level shifters have been proposed, but some challenges remain unresolved. This paper presents a new single-supply level shifter named the Transmission Gate-Based Bi-Directional Level Shifter (BDLS).This innovative architecture utilizes a transmission gate configuration to achieve level shifting with multiple input voltage levels while efficiently managing full voltage swing, power consumption, and delay requirements.

The paper is organized as follows: Section III presents an in-depth analysis of various level shifter designs from existing literature. Section IV describes the proposed bidirectional level shifter architecture in detail. Section V discusses the experimental results and provides a comparative analysis with other approaches. The final Section summarizes the findings and concludes the study. Furthermore, we introduce a novel multi-input bidirectional level shifter, designed to be compatible with variable voltage transformation level SoC circuits.

III. Analysis of Current Level Shifter Technologies

A. Conventional level shifter

When the input voltage (VIN) goes above the threshold voltage (VT) of the NMOS transistors M36 and M35, the circuit shown in Figure 3. utilizing a cross-coupled PMOS structure operates as a standard level shifter. This configuration facilitates signal transfer between distinct voltage domains by converting a lower input voltage into a higher output voltage. However, a major issue arises due to strong conflict between the pull-up (PMOS) and pull-down (NMOS) transistors which can compromise the effectiveness of the voltage translation.

This problem intensifies when the lower supply voltage (VDDL) drops below the threshold voltage of the NMOS transistors. Under such circumstances, the pull-down network becomes significantly weaker and cannot effectively counteract the pull-up network, potentially causing the level shifter to fail in delivering the correct output voltage. As the drive strength of the pull-down path decreases, its ability to sink current is also reduced. To enhance the reliability and efficiency of the voltage level shifting, it is crucial to strengthen the pull-down network's current-driving capability. network the pull-down network needs to be strengthened.

In practical applications, traditional level shifters exhibit two key limitations. First, thick gate oxide transistors (such as M36 and M35) struggle to operate correctly when the core supply voltage (VDDL) falls below 1V, primarily due to their inherently high threshold voltages. Second, the current driving strength of transistors M34 and M33 is governed by the I/O supply voltage (VDDH), while that of M36 and M35 is influenced by the core voltage (VDDL). Consequently, variations in VDDH lead to inconsistent drive strength, resulting in fluctuating delay performance in the level shifter. This makes conventional designs unsuitable for applications involving a wide range of voltage levels under a fixed core voltage.

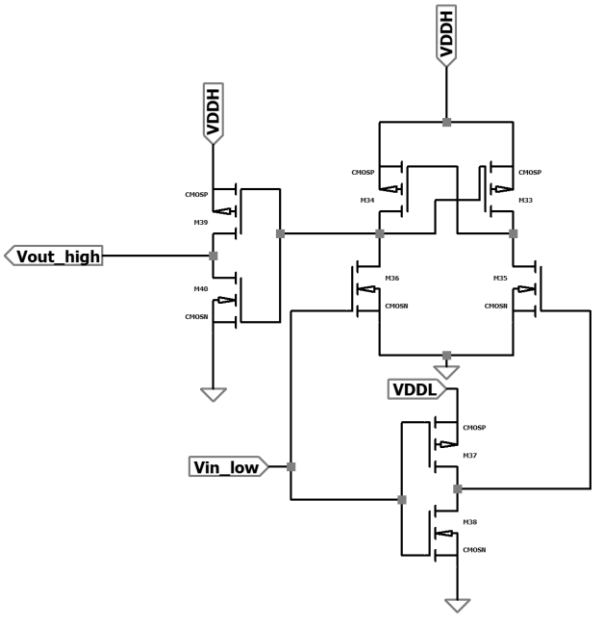

Fig. 3. PMOS cross coupled conventional LS

Furthermore, there is significant because of the conflict between the pull-down transistors (M36, M35) and the pull-up transistors (M34, M33). This contention not only increases signal propagation delay but also contributes to higher power consumption. The issue becomes more severe when VDDL varies, as optimal transistor sizing cannot effectively balance contention across both high and low VDDL conditions. Additionally, the presence of A direct current (DC) leakage path from the power supply to ground causes even more static power loss. In summary, conventional level shifters are challenged by poor performance at low core voltages, elevated static power usage, and timing instability caused by variations in transistor drive strength

B. Bi-directional level shifters

In practical applications, traditional level shifters exhibit two key limitations. First, thick gate oxide transistors (such as M36 and M35) struggle to operate correctly when the core supply voltage (VDDL) falls below 1V, primarily due to their inherently high threshold voltages. Second, the current driving strength of transistors M34 and M33 is governed by the I/O supply voltage (VDDH), while that of M36 and M35 is influenced by the core voltage (VDDL). Consequently, variations in VDDH lead to inconsistent drive strength, resulting in fluctuating delay performance in the level shifter. This makes conventional designs unsuitable for applications involving a wide range of voltage levels under a fixed core voltage.

Furthermore, there is significant delay caused by the competition between the pull-down transistors (M36, M35) and pull-up transistors (M34, M33). This contention not only increases signal propagation delay but also contributes to

higher power consumption. The issue becomes more severe when VDDL varies, as optimal transistor sizing cannot effectively balance contention across both high and low VDDL conditions. Additionally, a direct current leakage path from the power supply to ground adds to the static power loss. In summary, conventional level shifters are challenged by poor performance at low core voltages, elevated static power usage, and timing instability caused by variations in transistor drive strength

IV. IMPROVED AND PROPOSED DESIGN

A. *Improved design*

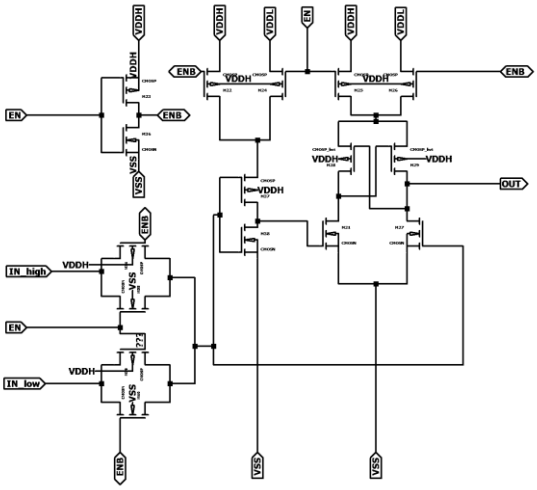

Fig. 4. Improved dual supply typical voltage range level shifter (DS-TRLS)

TABLE I. TRANSISTOR SIZES FOR DS-TRLS

Width/length	***NMOS***	***PMOS***
W/L	120n/100n	120n/100n

The level shifter circuit proposed by Madan and Iqbal encounters challenges related to voltage swing. These issues can be addressed by optimizing these problems can be solved by adjusting the sizes of MOSFETs or by using MOSFETs that have different threshold voltage (VT) levels. Or by utilizing MOSFETs with different threshold voltage levels (VT). The improved circuit, as shown in Fig.4, features a bidirectional level shifter configuration that employs high VT PMOS transistors PM1 and PM0 arranged in a cross-coupled topology. Using high VT PMOS devices helps reduce contention during the level-shifting process. This approach also increases the delay slightly, allowing adequate time for the output voltage level to achieve a complete swing from VDDL (Low Voltage Drain Drain) to VDDH (High Voltage Drain Drain) or vice versa.

To achieve a complete voltage swing, it is crucial to properly size both the PMOS transistors (in the cross-coupled pair) and The NMOS transistors in the pull-down network need to be properly sized. Correct sizing helps the circuit handle voltage swing limits and ensures reliable shifting from low to high and high to low levels. This method improves the level shifter's performance by balancing the delay from the high-threshold PMOS with enough drive strength for efficient voltage conversion.

As a result, the enhanced bidirectional level shifter efficiently manages signal transitions between different voltage domains, particularly in low-power applications where maintaining voltage swing integrity is essential.

B. *Proposed design*

While the enhanced circuit is capable of achieving full voltage levels, it comes with several drawbacks. It is not adaptable to convert a wide range of input voltages, as it can only shift the input to either VDDH or VDDL levels. Furthermore, achieving a full voltage swing results in an increase in propagation delay, primarily due to the use of high-VT devices. This design choice leads to slower performance. Additionally, incorporating high-VT devices within different CMOS process technologies complicates the integration process, making it difficult to implement across various process nodes.

Also there can static path will be formed as pull down network is directly connected to GND (VSS) level, where can be formation of leakage path , when the PMOS and NMOS both gets on by some input voltage levels this will lead to increased static power dissipation.

To overcome from this problem we've proposed the single supply bi-directional level shifter with variable voltage range output levels which can able to reduce static power dissipation (leakage currents) by providing the blocking NMOS switch between cross coupled pair and NMOS differential pair. Proposed design is shown in fig. 5 below.

TABLE II. TRANSISTOR SIZES FOR SS-WRLS

Width/length	***NMOS***	***PMOS***
W/L	120n/100n	120n/100n

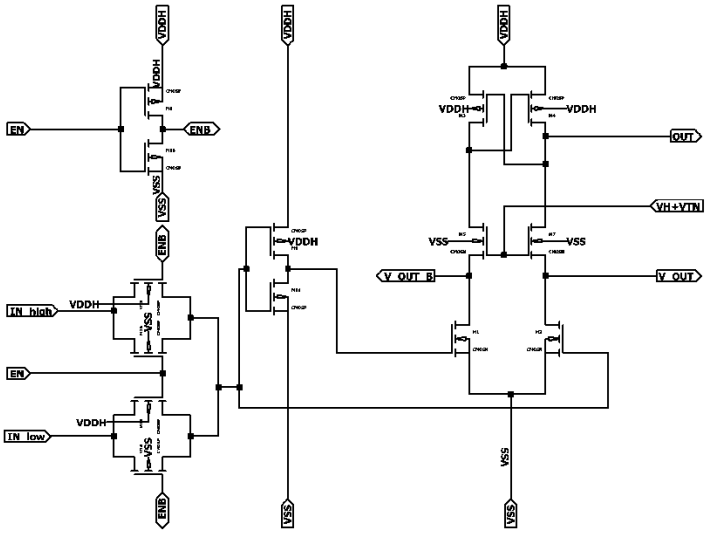

Fig. 5. A Single-Supply Level Shifter Designed for Wide Voltage Range (SS-WRLS)

This bidirectional voltage shifter utilizes a single supply voltage (VDDH) to perform both upward and downward level shifting. This design approach offers advantages in terms of placement, routing, congestion management, reduced parasitic capacitance, and minimized pin count and area requirements. The limiting NMOS pair M5 & M7 are

controlled by gate voltage VH+VTN (voltage high + threshold voltage of NMOS). VH is the highest voltage level up to which input voltage level is to be shifted.

To analyze the circuit behavior let us try low to high level shifting. To select in low input voltage EN is taken 0V which is equal to logic '1' and ENB will be 1.5V from cmos inverter output. And VDDH have taken 1.5V, in_low is 0.9V to convert a low voltage of 0.9V to a high voltage of 1.32V, the sum of VH and the NMOS threshold voltage (VTN) must equal 1.32V plus the NMOS threshold voltage for the given technology. In this case, the 90nm GPDK CMOS library is used.

The M1 & M2 will get on alternately, when 0.9 is applied to M2 gets on and M1 gets off, it will try to pull down the V_OUT_B node. The M3 & M4 from a latch that pushes one output node to a higher voltage. The regenerative action ensures that once the latch is set, it remains stable. The M7 starts conducting, allowing the charge to flow through it.
Once the output voltage reaches VH (high voltage), the VGS (gate to source voltage) of M7 reduces below the threshold, turning it OFF. This prevents further voltage rise, effectively limiting the upper voltage level.

Similarly while shifting the level from high to low voltage. EN is taken as '1.5V' which is equal to logic '0'and ENB will be '0V', in_low will be taken as '1.32V'and VH+VTN will be taken as 0.9V plus VTN of NMOS. Once the output voltage reaches 0.9V the M7 gets off, and output voltage will be limited to 0.9V voltage level.

This circuit can change an input voltage to any desired level, as long as it stays below the maximum voltage VDDH. This wide range of input voltage conversion is beneficial for large scale integration without any area, performance overhead. This circuits overcomes the drawbaacks of previous circuit of increased propagation delay, and additional transistors, and more static and dynamic power dissipation, this circuit does not required any addition process node transistors (high VT and low VT cells).

C. Another circuit improvement

The circuit can be modified to limit the low level voltage, we just need to add another PMOS pair in between NMOS differential pair and NMOS high voltage limiting pair.
The fig. 6 shows the improved circuit to limit high and low voltage level as same time, this both PMOS is controlled by their gate voltages VL-|VTP| is the voltage for which the PMOS gets on up to VL levels only going below VL the PMOS gets off and output voltage is limited by VL voltage level. Similarly as before explained the output upper voltage level will be limited by NMOS pairs with gate voltage VH+VTN.

This circuit is like the earlier ones, but adding an extra PMOS pair increases power use. However, it significantly reduces the average delay and static power loss, and it also allows easy adjustment of the VH and VL levels for any input signals.

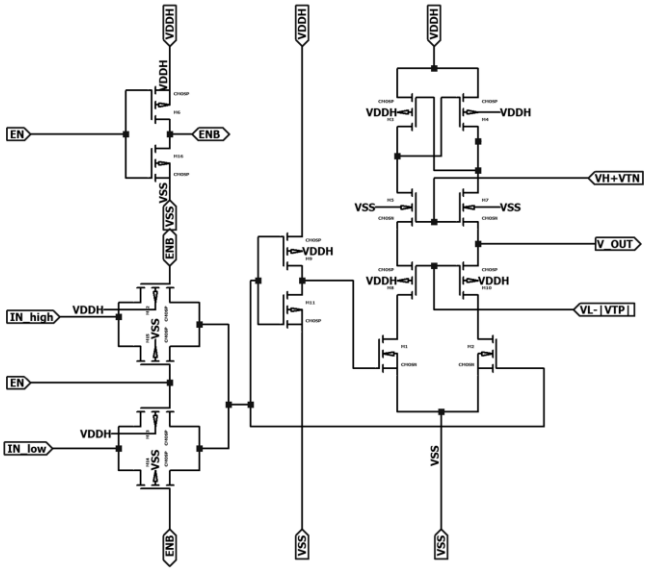

Fig. 6. Enhanced Single-Supply Level Shifter with Wide Voltage Range (SS-WRLS)

V. ANALYSIS OF SIMUALTION RESULTS

In this work, the level shifter (LS) circuit we propose shifter (LS) circuit and its associated configurations were designed and verified using the Cadence Virtuoso platform with the CMOS 90nm technology node. The robustness of the design was evaluated by varying the load capacitance from 10 fF to 90 fF and testing under different PVT conditions, including temperatures of 27°C, as well as operating frequencies of 100 MHz

A. Functional simulation

Figure 7 shows the transient analysis of the proposed single-supply dynamic bidirectional level shifter. In this design, the high supply voltage (VDDH) is 1.5 V, while the input voltages for low and high signals (IN_LOW and IN_HIGH) are 0.9 V and 1.32 V, respectively. The enable signal (EN) controls the direction of voltage level shifting.

When the EN signal is high, the circuit changes the output from 1.32 V to 0.9 V, as seen in Figure 7. When the EN signal is low, the circuit shifts the output from 0.9 V to 1.32 V, shown in Figure 8. This bidirectional feature lets the level shifter handle both high-to-low and low-to-high voltage changes effectively.

The proposed level shifter shows improved performance compared to conventional dual-supply designs. The conventional dual-supply level shifter has an average power consumption of 1.152 µW and a delay of 69.865 ps. In contrast, the single-supply wide-range voltage level shifter demonstrates a significantly lower average power consumption of 0.3728 µW and a reduced delay of 28.4 ps.

These improvements result from the efficient circuit architecture, which effectively balances power dissipation and speed. By utilizing a single supply voltage, the design minimizes routing complexity and reduces power loss, making it suitable for designed for low power use and fast performance.

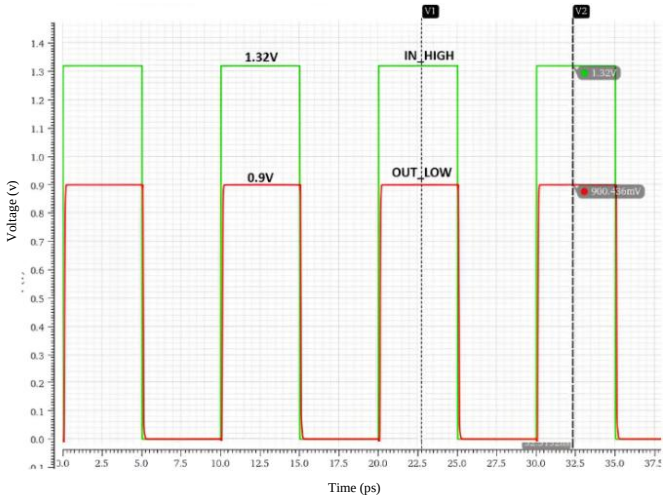

Fig. 7. Transient response of SS-WRLS in high to low shifting mode

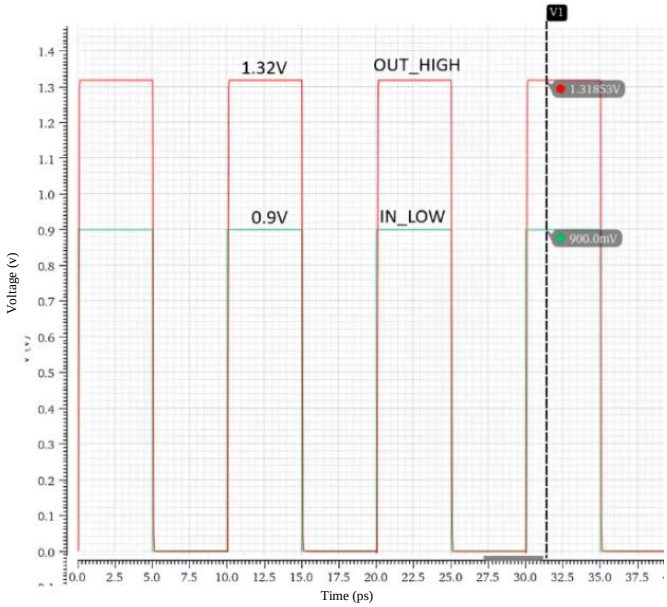

Fig. 8. Transient response of SS-WRLS in low to high shifting mode

B. *Power anlysis of the design*

The average power used by the proposed bidirectional level shifter circuit is shown in Table III and illustrated in Figure 9 below. The design behavior has been examined with other proposed designs and our proposed, improved designs. The analysis has been taken in 100 MHz operating frequency and 10fF load capacitance. The static power dissipation is also compared with other proposed designs and it is shown in table IV and fig.10.

Dynamic power dissipation takes place when a digital circuit transitions between states (from 0 to 1 or vice versa). This type of power loss primarily arises from the charging and discharging of load capacitances, as well as short-circuit currents that occur during switching events. On the other hand, static power dissipation occurs when the circuit remains idle (not switching) and is mainly attributed to leakage currents flowing through transistors in the off state. The major contributors to static power are subthreshold leakage and gate oxide leakage.

TABLE III. COMPARISON OF AVERAGE DYNAMIC POWER DISSIPPATION

Mode of shifting	*[1]*	*[2]*	*[3]*	***Improved design***	***Proposed design***
Low to high	6.23	7.22	39.28	1.026	0.62
High to low	5.97	3.39	26.74	1.278	0.1256

a. Unit of power dissipation taken here is in Microwatts (uW)

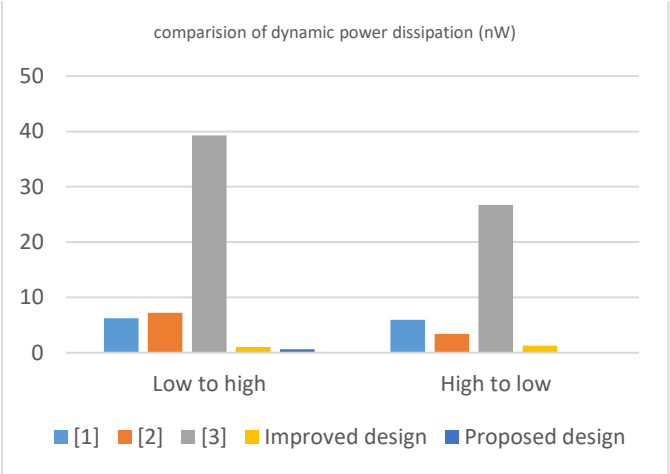

Fig. 9. Comparison of proposed and existing level shifter in terms of dynamic power dissipation

TABLE IV. COMPARISON OF AVERAGE STATIC POWER DISSIPPATION

Mode of shifting	*[1]*	*[2]*	*[3]*	***Improved design***	***Proposed design***
Leakage power	2.50	3.10	4.20	2.80	1.20

b. Unit of power dissipation taken here is in Nano watts (nW)

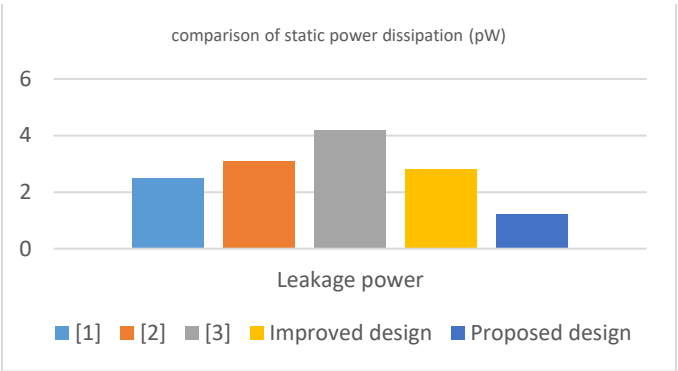

Fig. 10. Comparison of proposed and existing level shifter in terms of static power dissipation

C. *Delay analysis*

The delay characteristics of various BDLS circuit designs are presented in Table V and illustrated in Figure 11. The analysis examines the delay behavior during different shifting modes, including covering both high-to-low and low-to-high transitions. In the simulation, a load capacitance of 10 fF was used to measure the delay performance.

TABLE V. COMPARISON OF AVERAGE PROPAGRATION DELAY

Mode of shifting	*[1]*	*[6]*	*[4]*	***Improved design***	***Proposed design***
Low to high	145.3	298.6	218.2	70.6	33.3
High to low	127.7	146.4	240.1	89.13	23.5

c. Unit of propagation delay is taken here is in picoseconds(ps)

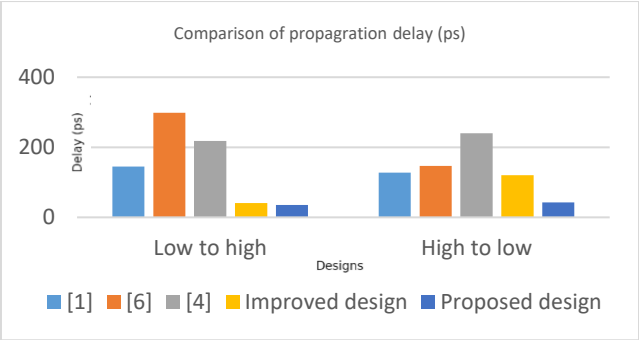

Fig. 11. Comparison of proposed and existing level shifter in terms of propagation delay

D. *Layout of CMOS level shifter*

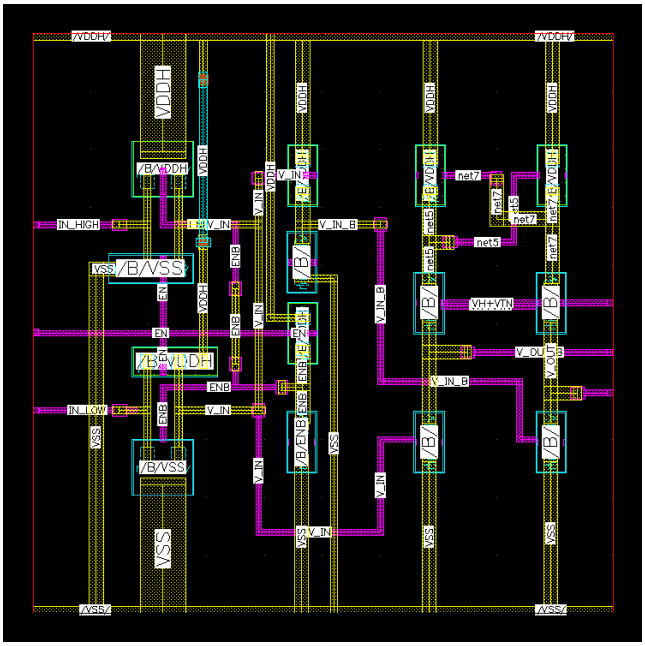

Fig. 12. Design Layout for the SS-WRLS Circuit

E. *Comaparison analysis with other existing design*

The proposed BDLS can be effectively compared with other benchmark designs. Table VI presents the characteristics of various level shifters, highlighting a comparison with existing LS designs while taking into account key VLSI constraints. The proposed design demonstrates superior performance in most critical aspects.

TABLE VI. COMPARISON OF EXISTING AND PROPOSED LEVEL SHIFTERS

Parameters	*[1]*	*[2]*	*[3]*	*[4]*	*[5]*	*Improved*	*Proposed*
Shifting type	H-L	BI	BI	BI	BI	BI	BI
Average dynamic power dissipation (uW)	6.10	5.30	33.10	640.00	9.15	1.15	0.37
Average static power dissipation(pW)	2.50	3.10	4.20	-	1.05	2.80	1.20
Average delay(ps)	136.50	40.90	-	21.00	281.00	79.80	28.40
VOUT(MAX)	1.80V	1.32	13.50	2.20	1.50	1.80	Up to VH
VOUT(MIN)	1.20V	0.60	4.50	0.20	1.00	0.90	Up to VL
Supply type	SST	SST	DST	MST	DST	DST	SST
Area overhead	High	Med	High	High	Low	High	Med
Process node	45nm	90nm	45nm	90nm	90nm	90nm	90nm
Special VT device	LVT	None	None	HVT, LVT	None	HVT, LVT	None

VI. CONCLUSION

This paper introduces and analyzes two types of bidirectional level shifters a dual-supply level shifter with a fixed voltage range and a single-supply level shifter that supports a wide voltage range these designs are evaluated based on their power efficiency and timing performance. Simulations were conducted using TSMC & CMOS technologies at 180nm, 90nm. The enhanced dual-supply level shifter achieves an average power consumption of 1.152 µW with a propagation delay of 69.865 ps.

In contrast, the proposed single-supply design demonstrates superior performance, with average power usage of only 0.3728 µW and a delay of 28.4 ps. This results in power and delay reductions of approximately 67.63% and 59.35%, respectively, highlighting its advantages in terms of efficiency, system complexity, and cost.

This paper also introduces a reliable single-supply level shifter design that can handle a wide range of input and output voltages. The single-supply wide voltage range level shifter (SS-WVRLS) works well across the full core voltage range from 0.5 V to 1.8 V, no matter how VDDIN and VDD are combined or increased.

This feature makes it particularly well-suited for low-voltage applications and removes the need for special threshold voltage transistors, which would otherwise require additional processing steps and increase manufacturing costs.

In SoCs that use dynamic voltage scaling (DVS) across multiple cores or voltage domains, the voltage levels of individual regions may vary or be unknown at design time. Therefore, a flexible level shifting solution is essential to support voltage translation across any pair of supply voltages without introducing constraints on power or performance. The proposed SS-WVRLS circuit addresses this challenge by employing a current-mode architecture that avoids limitations imposed by threshold voltages, making it highly suitable for DVS-enabled modern SoCs.

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