DIGITAL IC DESIGN LAB (EC1062)

LAB ASSIGNMENT - 3

Submitted By:

ANKIT KUMAR

24EC4224

Department: Microelectronics and VLSI

Submitted To:

Dr. Hemanta Kumar Mondal

Assistant Professor, Department of ECE, NIT Durgapur

Submitted on-

Experiment No.:3

Objective:

To design and plot the static Voltage Transfer Characteristics (VTC) of CMOS inverters and implement 2-input NAND and NOR gates using Cadence Virtuoso.

Specification:

1. **CMOS Inverter:**
   - **Technology:** 90 nm CMOS technology.
   - **Supply Voltage (VDD):** 1.2 V.
   - **Threshold Voltage (Vth):** NMOS = 0.3 V, PMOS = -0.3 V.
   - **Load Capacitance:** 5 fF.
   - **Design Constraints:**
     - The PMOS transistor size (W/L) should be larger than the NMOS to balance drive strength due to differences in mobility.
     - Symmetry in switching thresholds should be maintained for optimal noise margin.
   - **Expected VTC Behavior:**
     - The plot should exhibit distinct low-to-high and high-to-low transitions.
     - The transition region should be analyzed for the switching threshold (VM), defined as the input voltage at which the output is at half of VDD.
2. **2-input NAND Gate:**
   - **Transistor Count:** 4 (2 NMOS in series, 2 PMOS in parallel).
   - **Supply Voltage (VDD):** 1.2 V.
   - **Logical Expression:** Y = (A * B)'
3. **2-input NOR Gate:**
   - **Transistor Count:** 4 (2 PMOS in series, 2 NMOS in parallel).
   - **Supply Voltage (VDD):** 1.2 V.
   - **Logical Expression:** Y = (A + B)'

Schematic Entry:

- **CMOS Inverter Schematic:** Designed using Cadence Virtuoso with properly sized PMOS and NMOS transistors. Connections made to input, output, power supply, and ground.

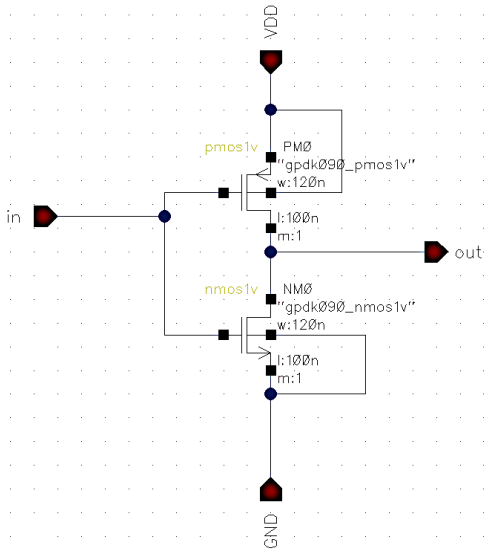


Figure 1 cmos inverter

- **2-input NAND Gate Schematic:** Transistor-level design using two NMOS transistors in series and two PMOS transistors in parallel, based on CMOS logic design.

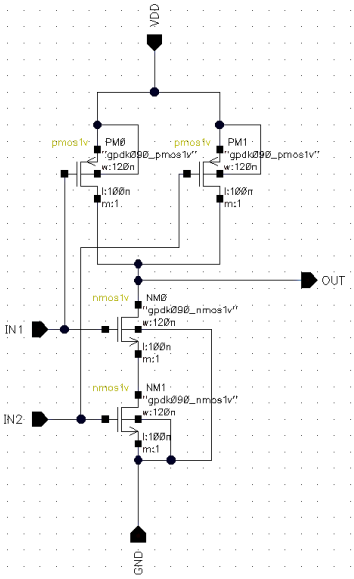


Figure 2 cmos nand

- **2-input NOR Gate Schematic:** Similar to the NAND gate but with a parallel NMOS configuration and series PMOS configuration.

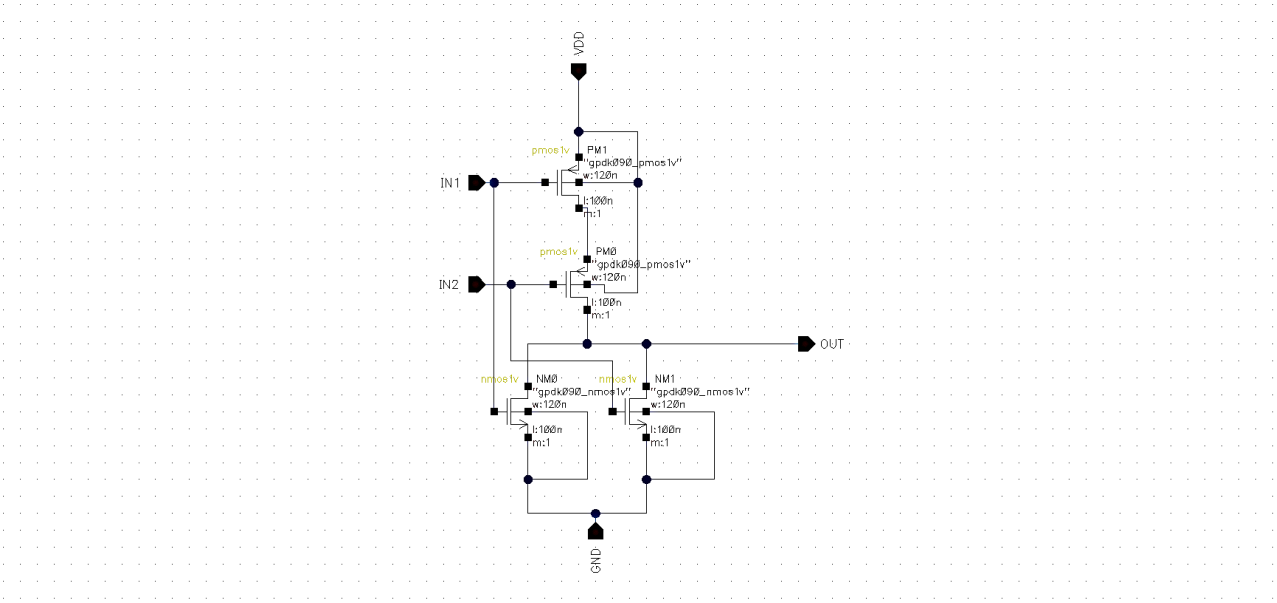
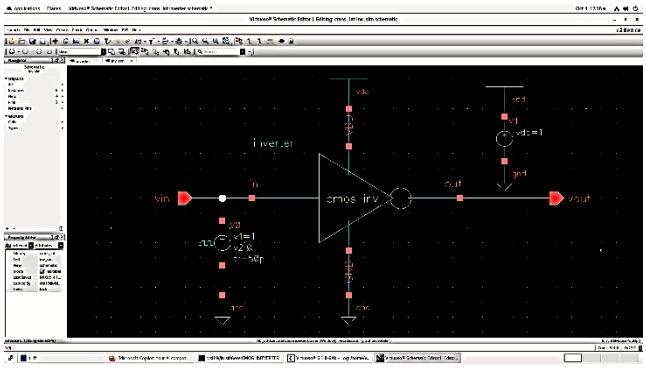


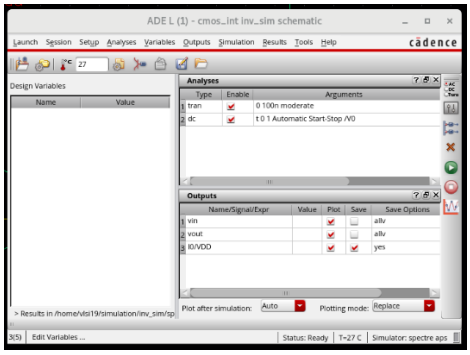
Figure 3 cmos nor

Simulation Setup:

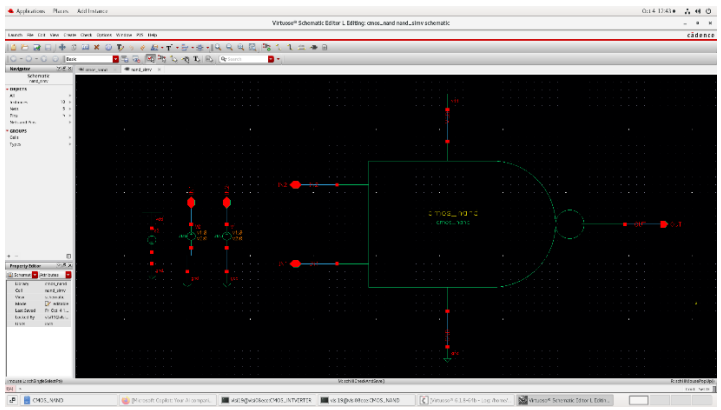
- **Cadence Virtuoso ADE L Window:** Set up transient analysis and DC sweep in ADE L window to measure the VTC of the CMOS inverter and verify logic gate functionality.
- **Voltage Sweep:** A DC sweep is used for the CMOS inverter to generate the VTC by varying the input voltage from 0 to 1.2 V.
- **Transient Analysis:** Logic gates (NAND, NOR) are tested by applying combinations of logical 0 and 1 to the inputs (A, B) and observing the outputs in the transient window.

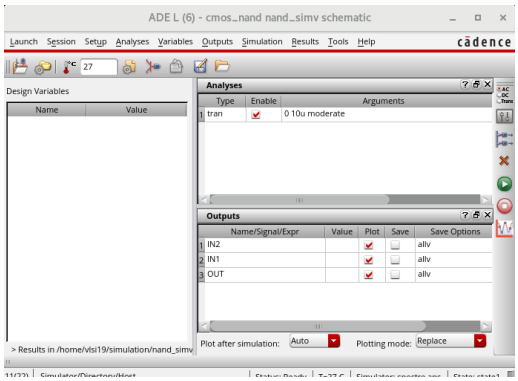
CMOS INVETER



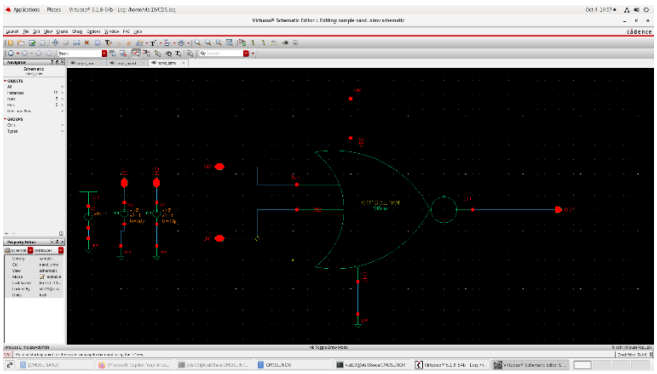


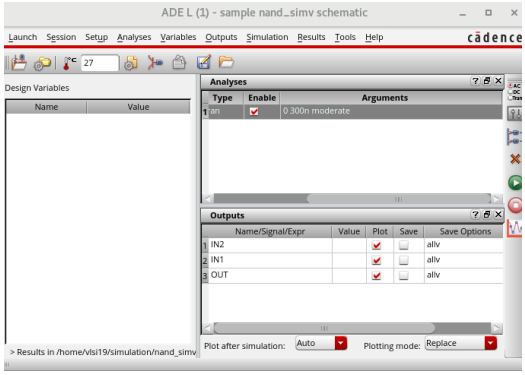
CMOS _NAND





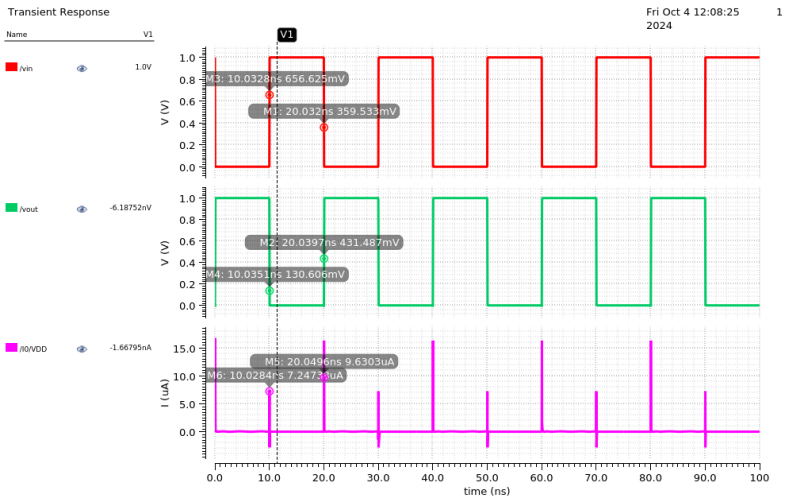
CMOS NOR



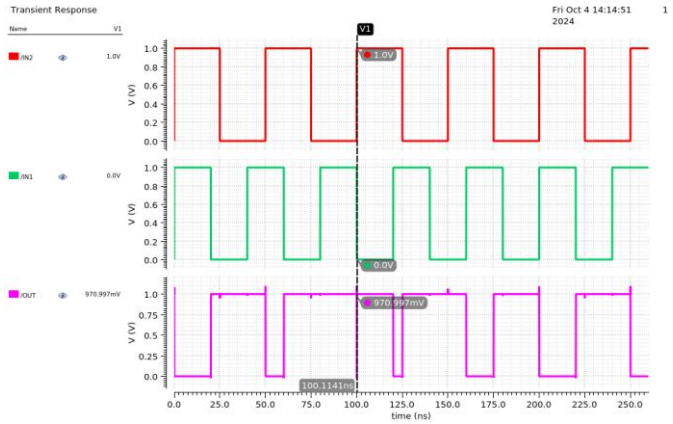


Experimental Results:

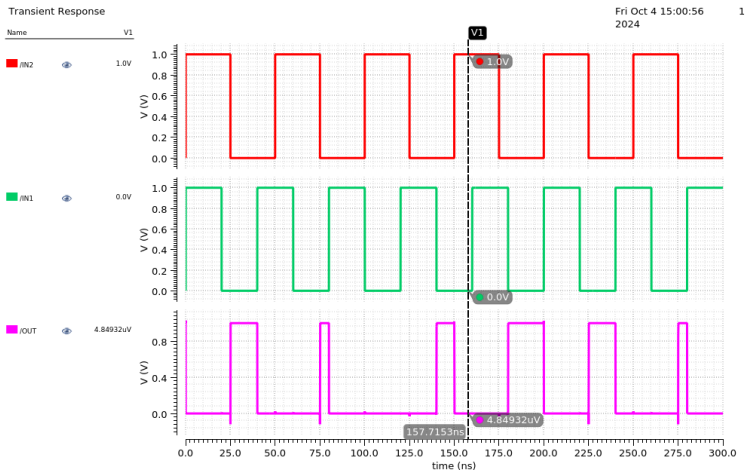
- **CMOS Inverter:** The VTC graph was plotted, showing a clear transition at the switching threshold, approximately at half of the supply voltage (~0.6 V). Noise margins were verified from the VTC plot.



- **NAND Gate Output:** The output was high for all combinations except when both inputs were high (A = 1, B = 1). The truth table was verified.



- **NOR Gate Output:** The output was high only when both inputs were low (A = 0, B = 0). The truth table was verified.



Observations:

- The static VTC for the CMOS inverter showed expected behavior, with a sharp transition in the middle of the voltage range.
- Both the 2-input NAND and NOR gates functioned correctly, with logical behavior corresponding to their truth tables. The transistor-level implementation adhered to CMOS logic design rules, and power consumption was within acceptable limits.