DIGITAL IC DESIGN LAB (EC1062)

LAB ASSIGNMENT - 6

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Submitted To:

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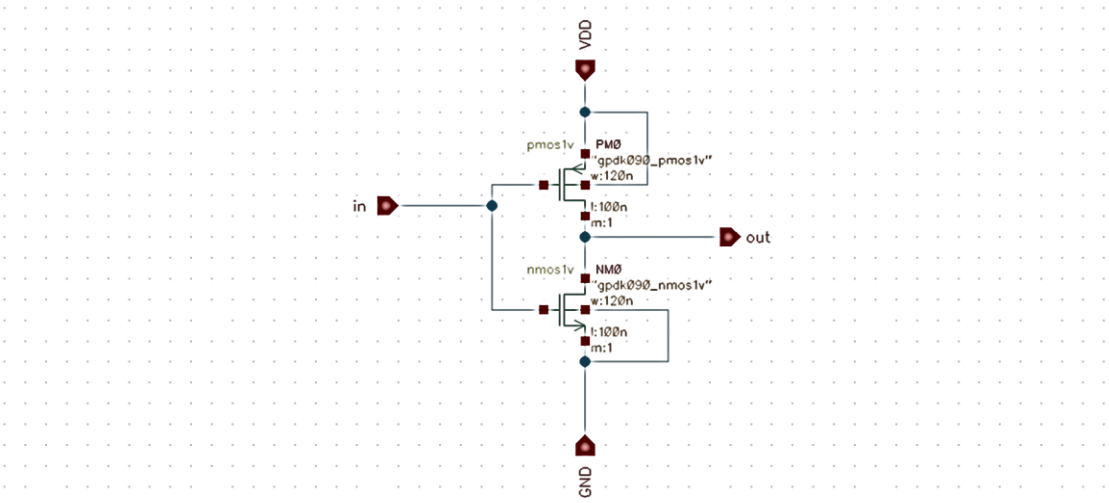
Submitted on-

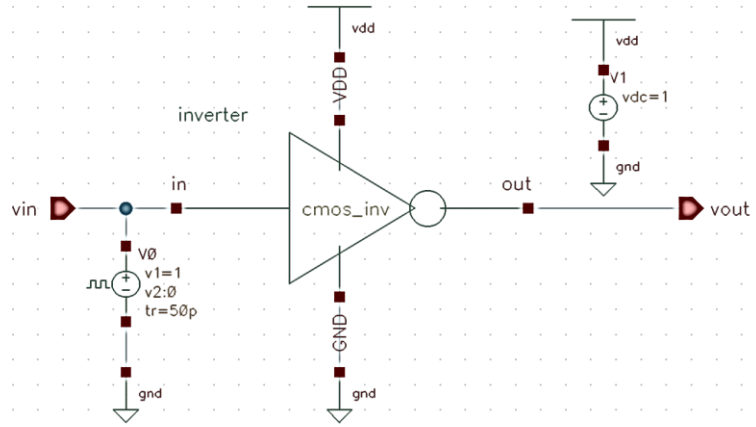
Design 1: Dynamic Characteristics of CMOS Inverters

Objective:
To design and simulate the dynamic characteristics of CMOS inverters and analyze their behavior under varying load conditions and PVT variations.

Circuit Description:
The CMOS inverter serves as the fundamental building block in digital circuits, where a high input voltage results in a low output voltage and vice versa. The design and simulation are based on CMOS 90 nm technology for schematic creation, with analysis of PVT variations using 180 nm and 65 nm processes. The performance is characterized through key parameters like noise margin, power dissipation, and delay.

Schematic:
The schematic diagram was created using Cadence Virtuoso in 90 nm technology, showing the PMOS and NMOS transistors connected in a complementary manner



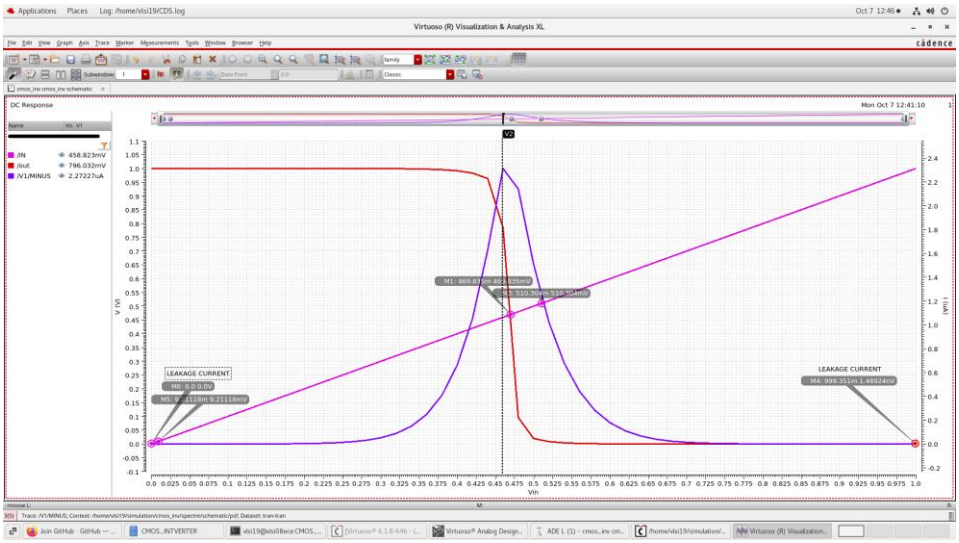


EDA Tool Setup:

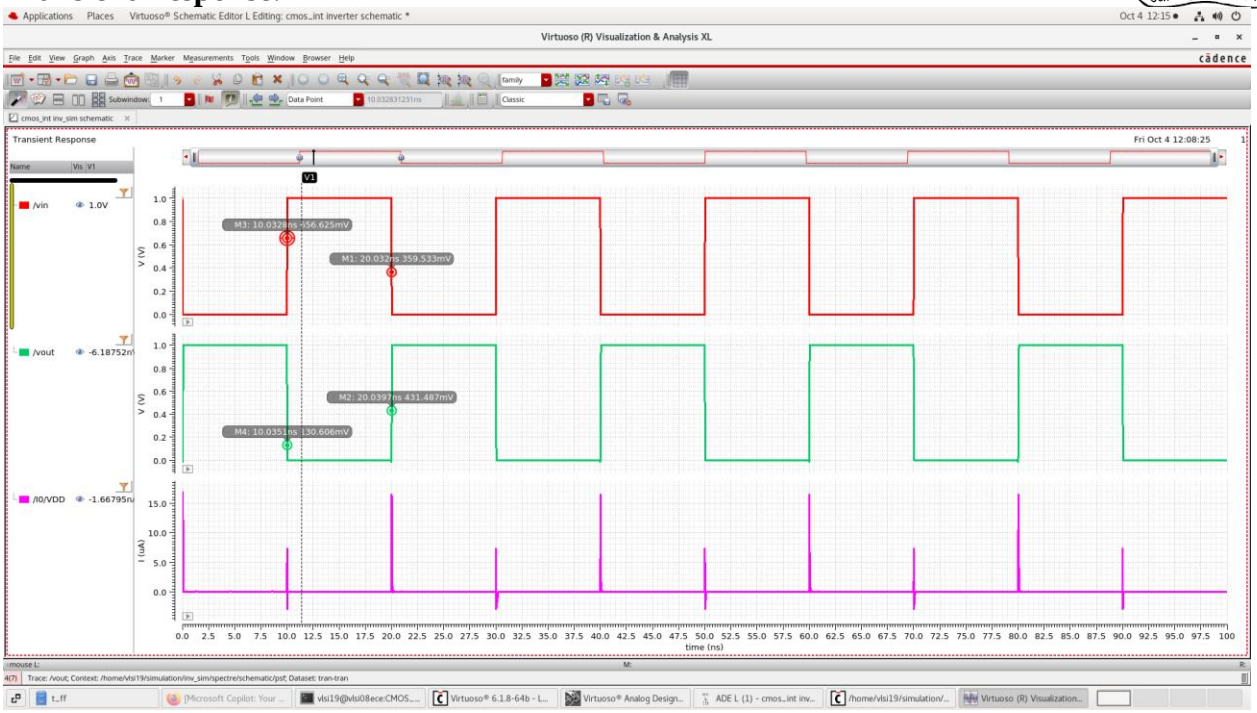
- **Schematic Creation**: Using Cadence Virtuoso in 90 nm technology.
- **Simulation**: ADL window for analyzing DC and transient responses.
- **PVT Analysis**: ADL XL to examine variations in process, voltage, and temperature for both 180 nm and 65 nm processes. Making all transistor width parameter as Wn for Nmos and Wp for Pmos.

Experimental Results:

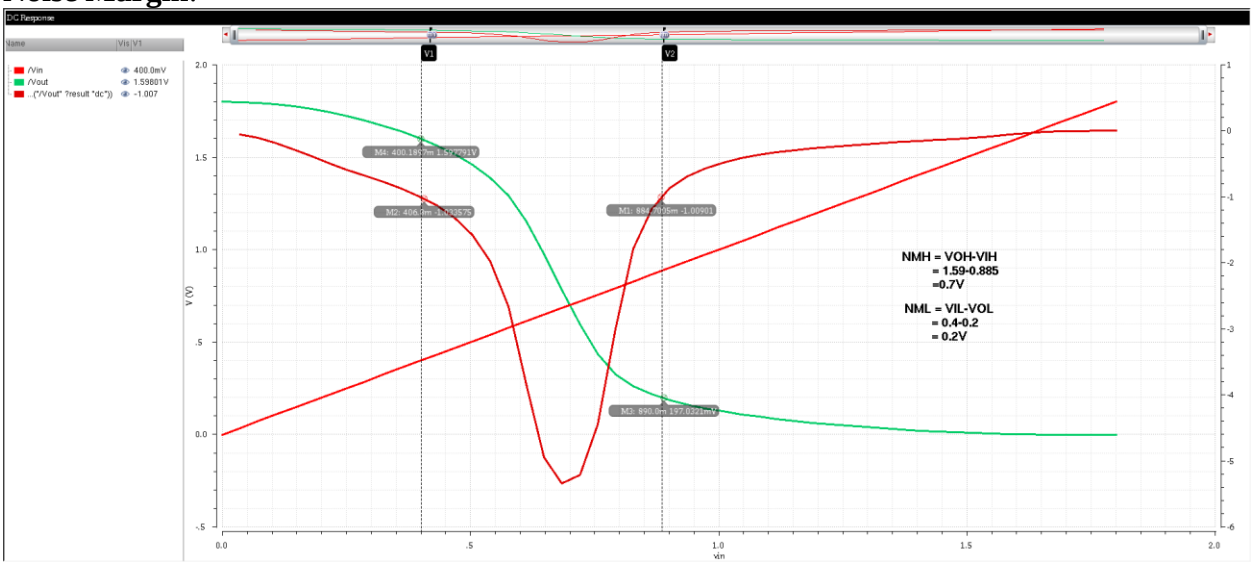
1. **DC Response**:



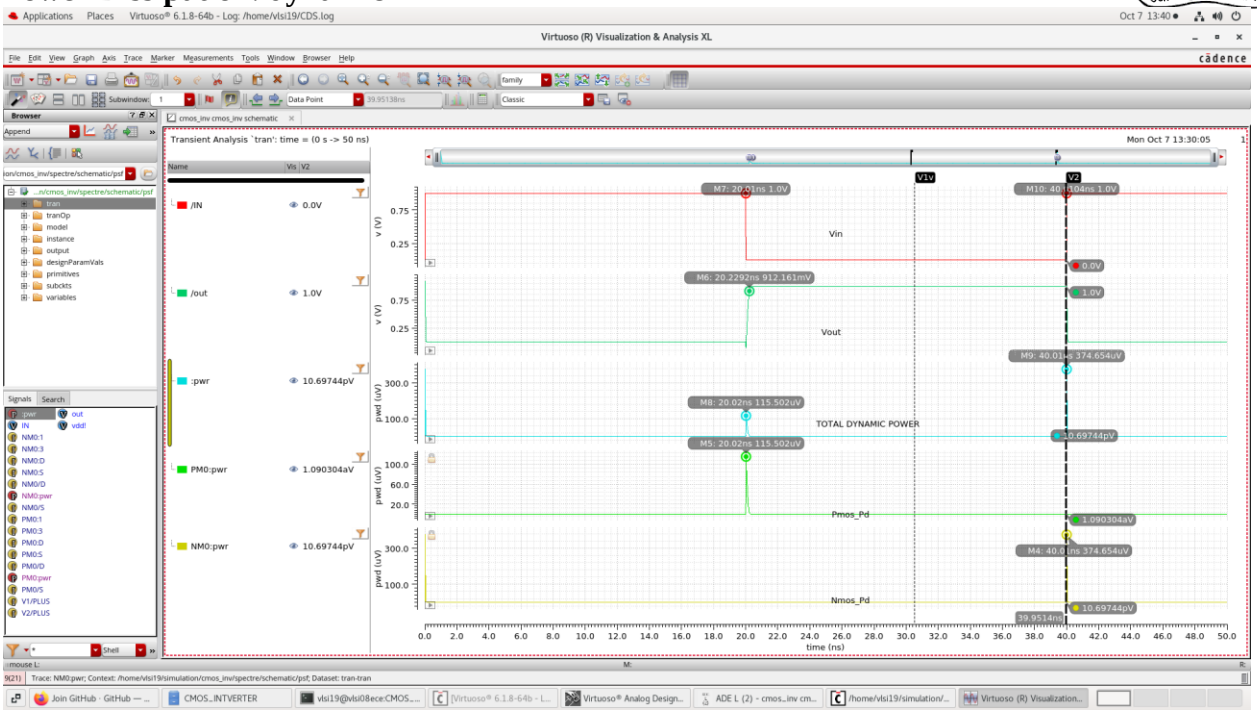
2. **Transient Response**:



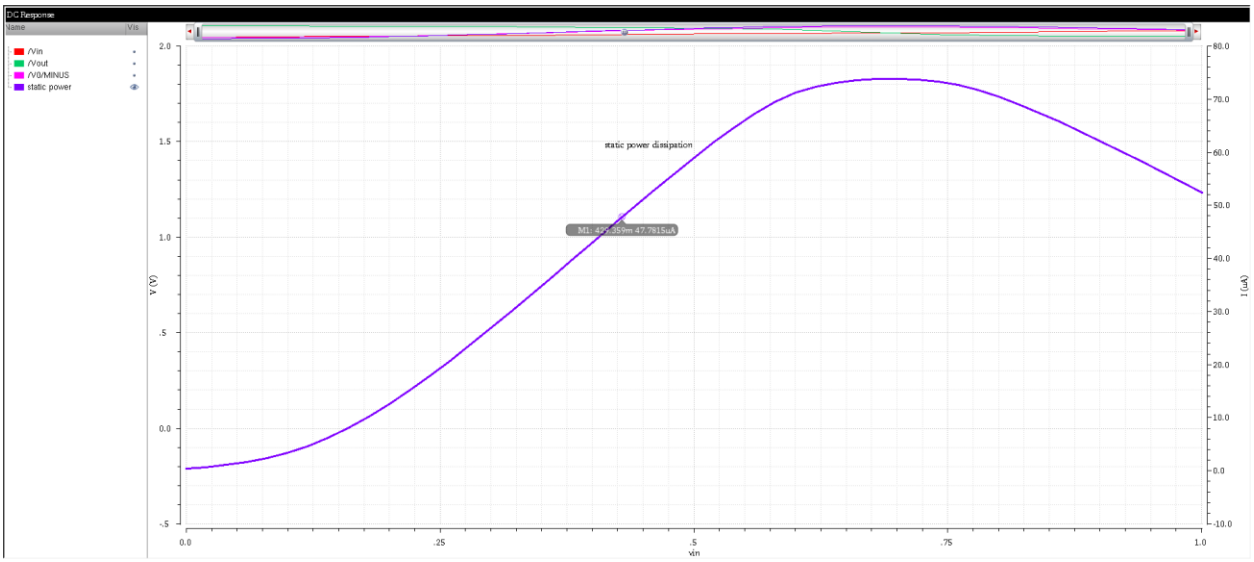
3. **Noise Margin**:



4. **Power Dissipation: dynamic**

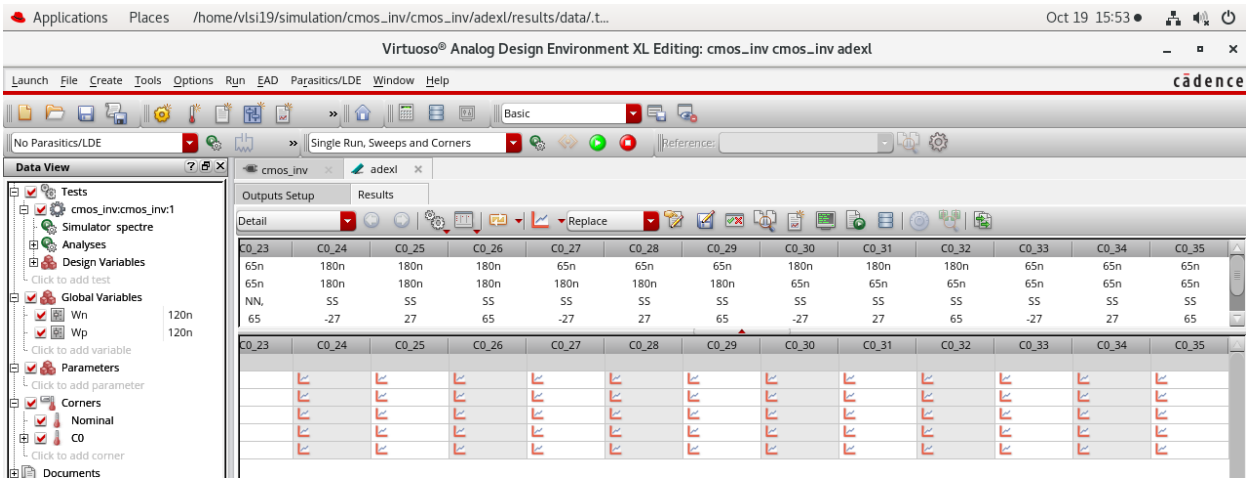


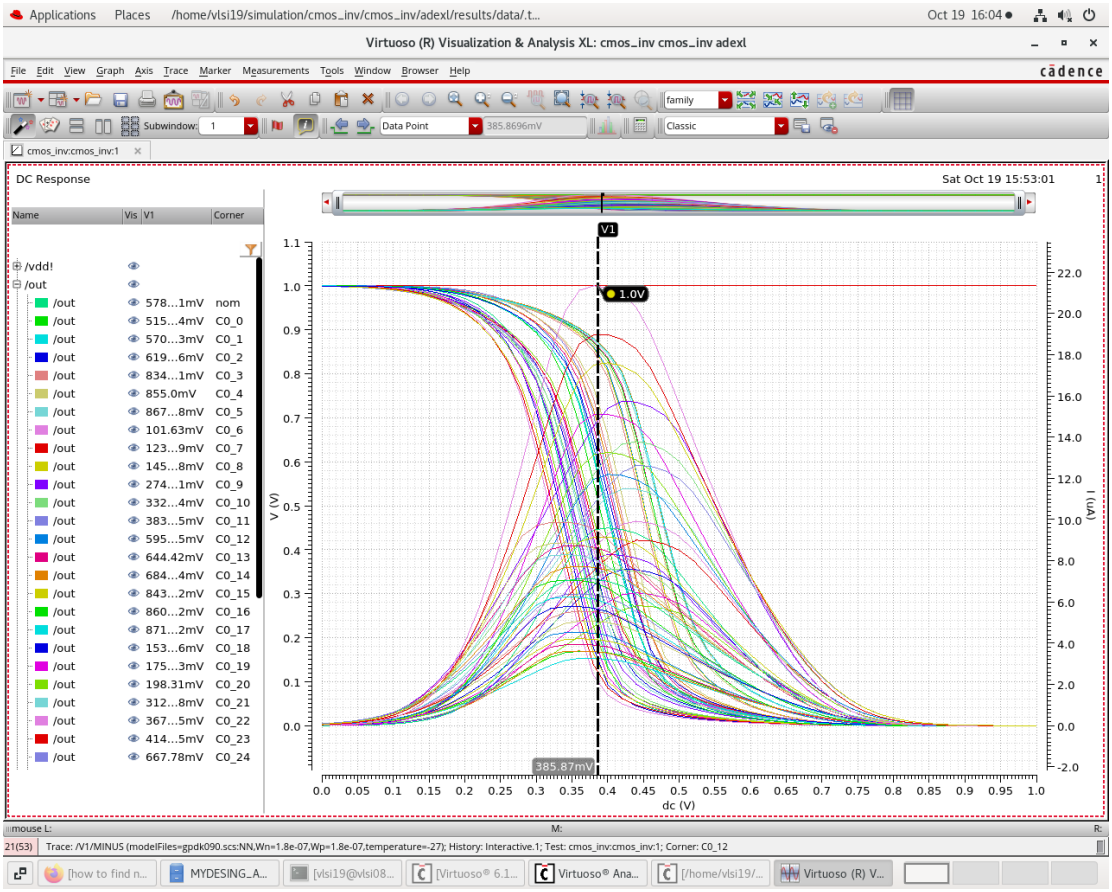
Static Power Dissipation of CMOS:



5. **Delay**: $\frac{579.7E-12}{} = \frac{(345.8E-12 + 813.6E-12)/2}{}$ falltime and risetime dealy average.

6. **PVT Analysis**:
   - Use CMOS 180 nm and 65 nm process parameters.
   - Analyze the robustness of the inverter design with respect to these variations.
   -





Observations:
The circuit was created in 90 nm technology, tested, and analyzed using Cadence software according to the design specifications. The analysis showed that the CMOS inverter meets expected performance criteria, with insights into optimizing noise margins, delay, and power efficiency.

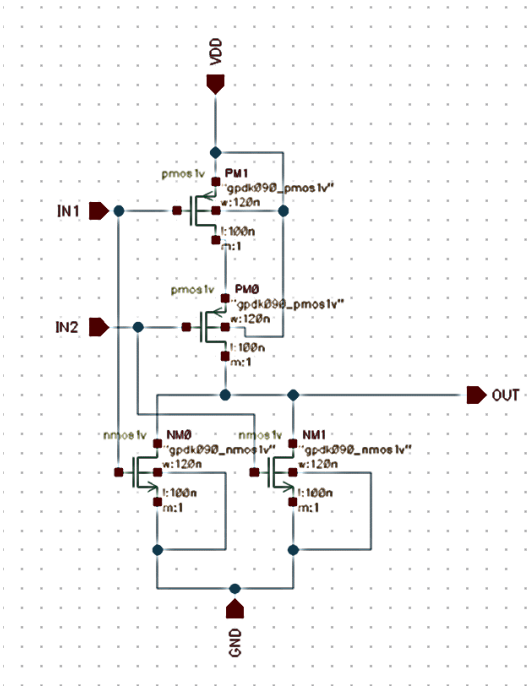
Design 2: CMOS NAND, NOR, and XOR Gates

Objective:
To design and simulate CMOS NAND, NOR, and XOR gates, and evaluate their performance in terms of speed, power dissipation, and noise margins.

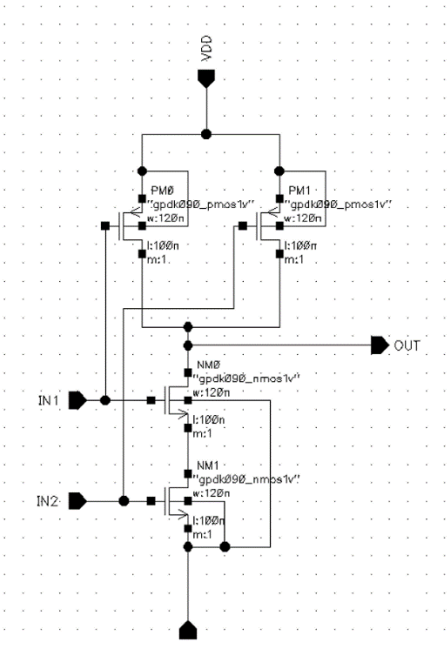
Circuit Description:
CMOS NAND and NOR gates are essential components for building complex logic circuits, while XOR gates are crucial for arithmetic and parity operations. These gates are implemented using CMOS technology, with schematics created in 90 nm technology and PVT analysis conducted using 180 nm and 65 nm processes. The design explores how different gates behave under varying conditions.

Schematic:
The schematics for each gate were created in 90 nm technology using Cadence Virtuoso. Explain the transistor arrangements and how logic functions are achieved.

CMOS NOR



CMOS NAND



CMOS XOR

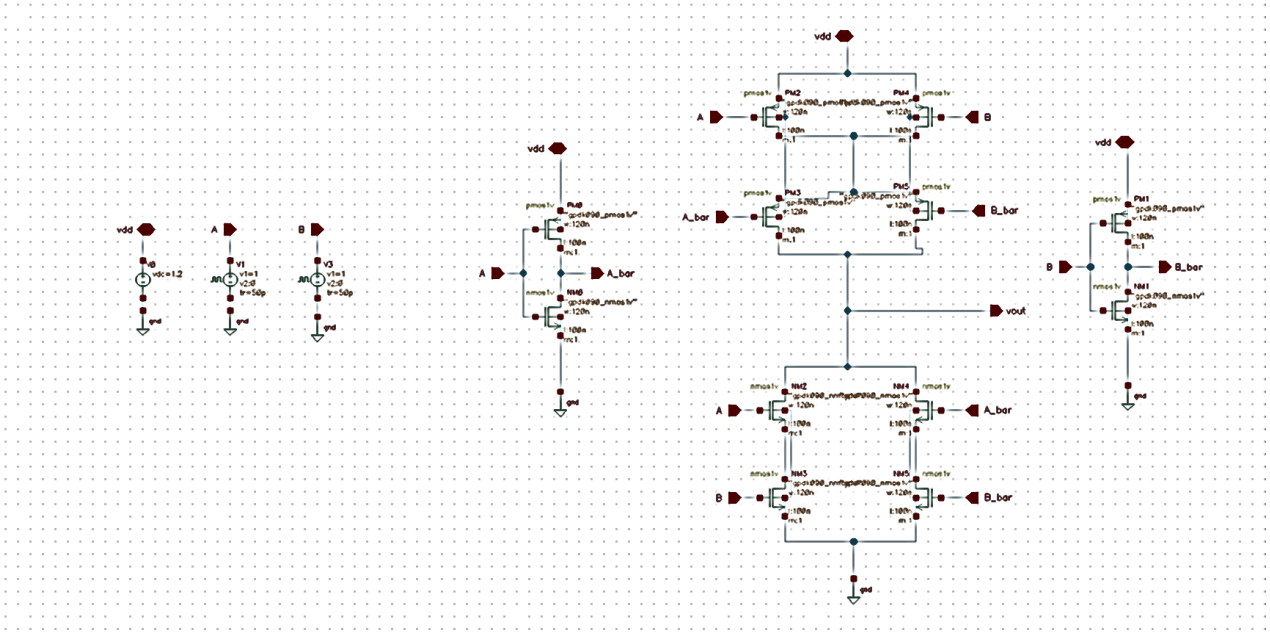
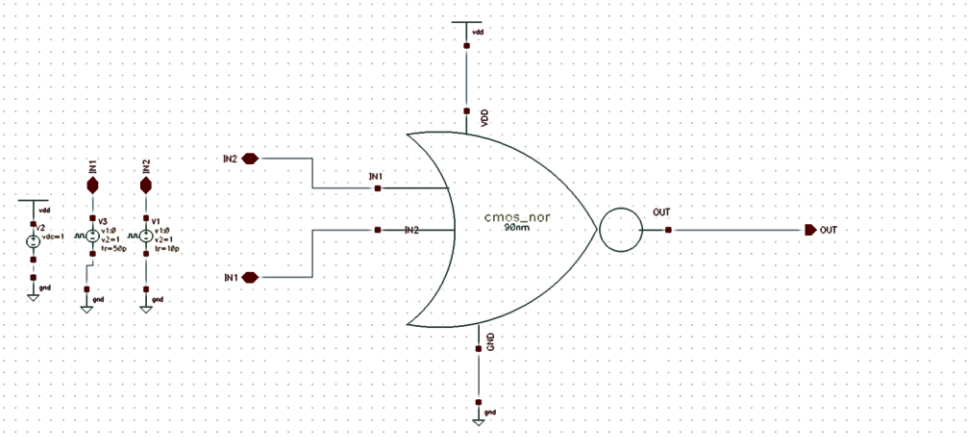


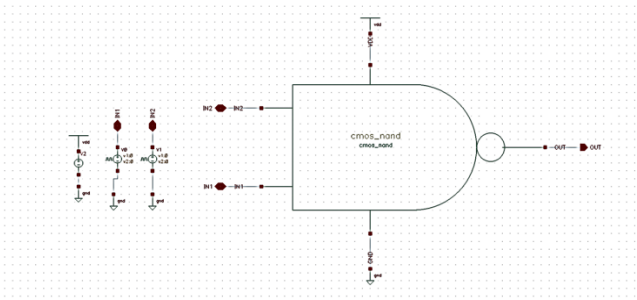
Fig: XOR gate schematic.

EDA Tool Setup:

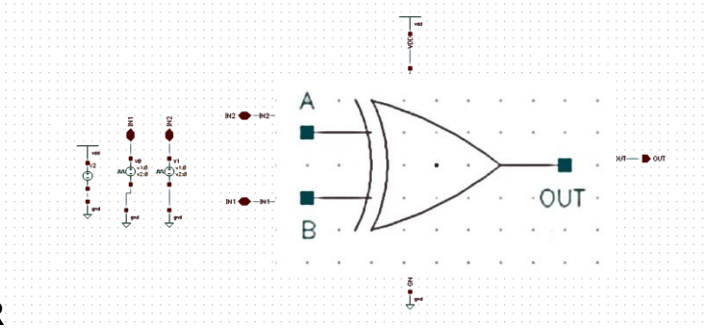
- **Schematic Creation**: Cadence Virtuoso in 90 nm technology.
- **Simulation**: ADL window for functional and performance analysis.
- **PVT Analysis**: ADL XL for comprehensive variation studies using 180 nm and 65 nm process parameters. Making all transistor width parameter as Wn for Nmos and Wp for Pmos.

CMOS NOR :





CMOS NAND

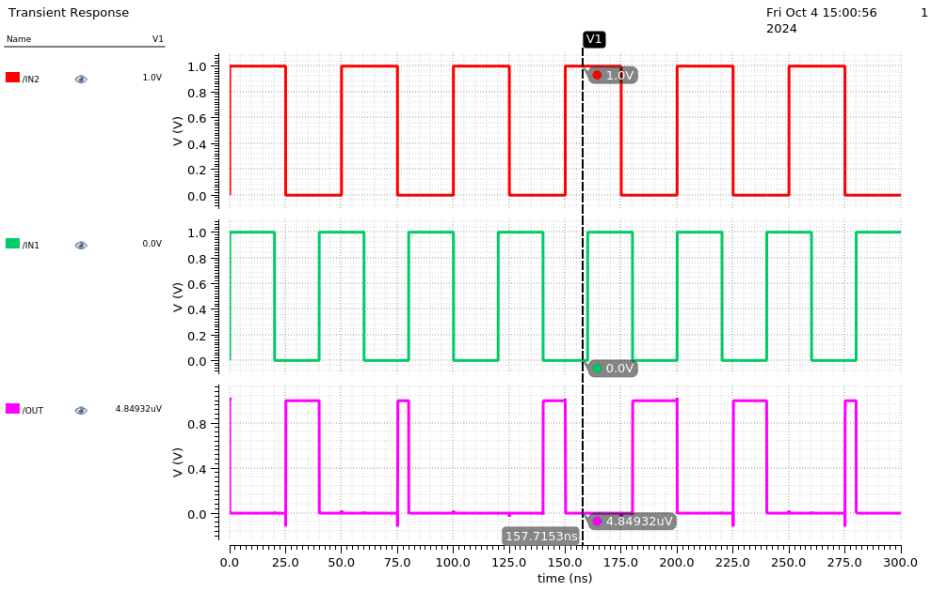


CMOS XOR

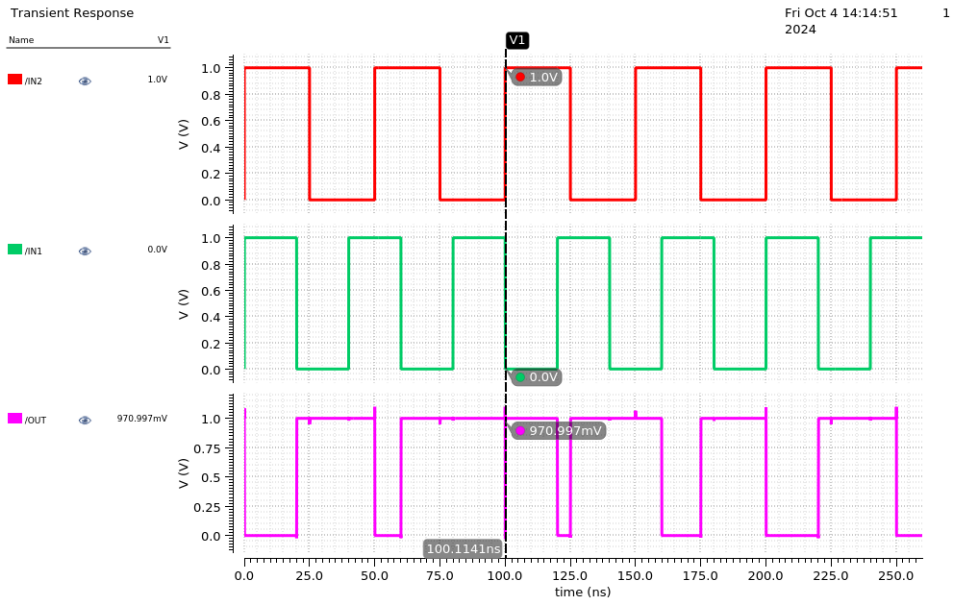
Experimental Results:

1. **Transient Response**:
   - Show input-output timing diagrams.
   - Measure and discuss the delay for different input conditions.

CMOS NOR



CMOS NAND



CMOS XOR

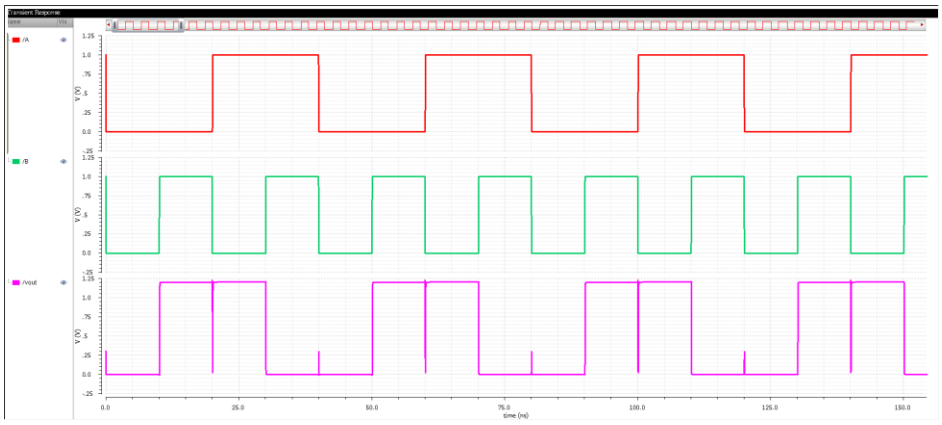


Fig: XOR transient response.

Observations:

The circuits were created in 90 nm technology, tested, and analyzed using Cadence software. The results provide valuable insights into the trade-offs between power, speed, and reliability for each gate.

Design 3: CMOS Transmission Gates and PTL Logic Circuits

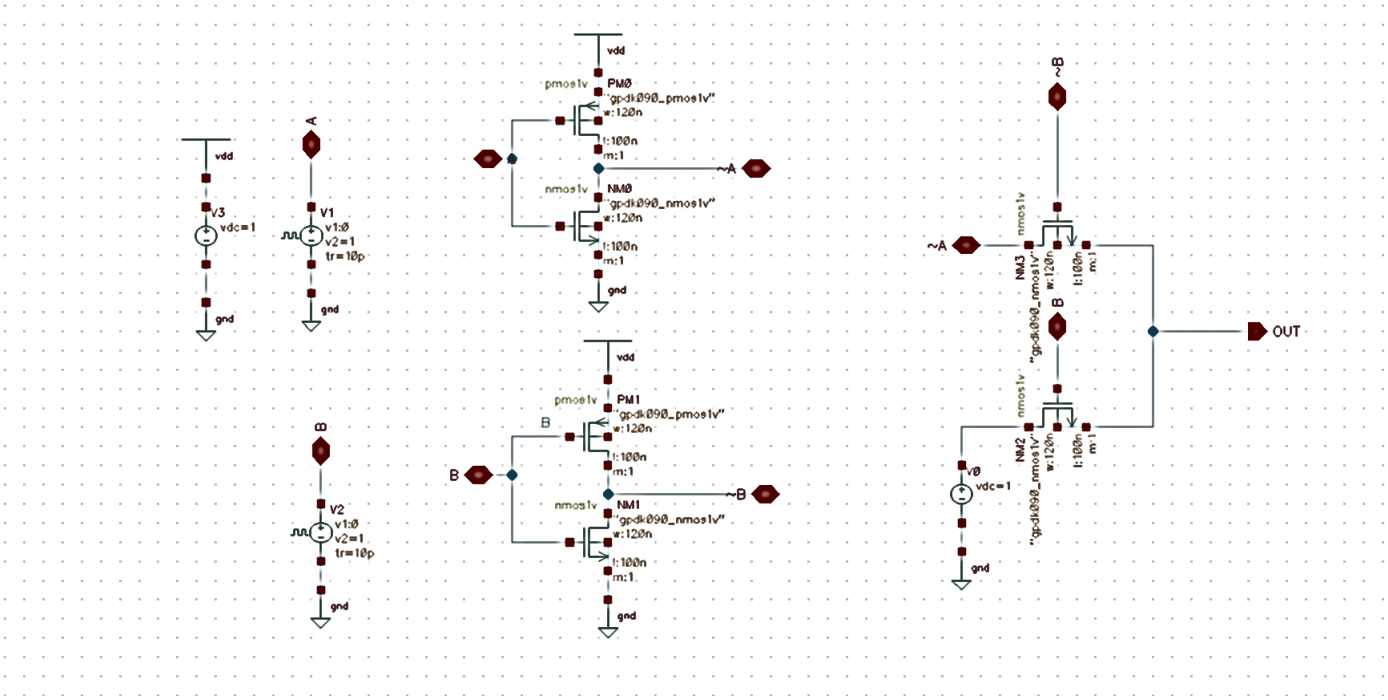
Objective:
To design and implement CMOS transmission gates and logic circuits using pass transistor logic (PTL), and analyze their performance.

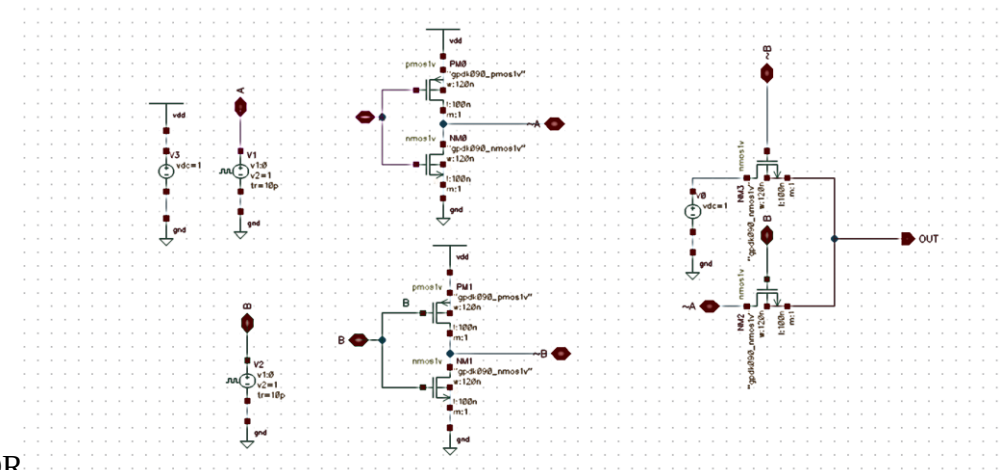
Circuit Description:
CMOS transmission gates are versatile components used to implement efficient multiplexers and switches. PTL circuits reduce transistor count and potentially increase speed. The schematics were created in 90 nm technology, with PVT analysis performed using 180 nm and 65 nm processes. This design examines the advantages and limitations of PTL circuits in digital logic implementation.

Schematic:
Transmission gate and PTL logic circuit schematics were created in 90 nm technology using Cadence Virtuoso. Explain how these circuits achieve efficient signal transmission and logic operations.

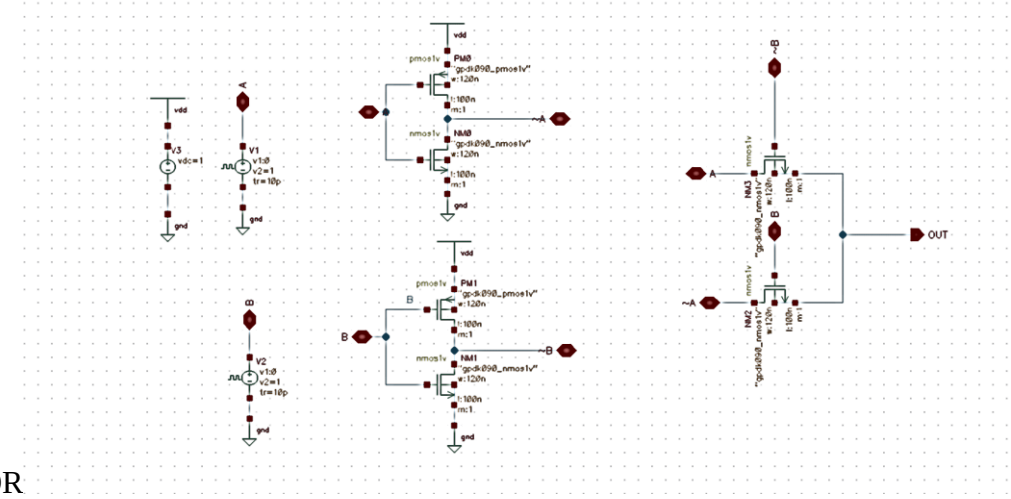
LOGIC_CIRCUITS USING PT LOGIC

NAND





NOR



XOR

TG_LOGIC-

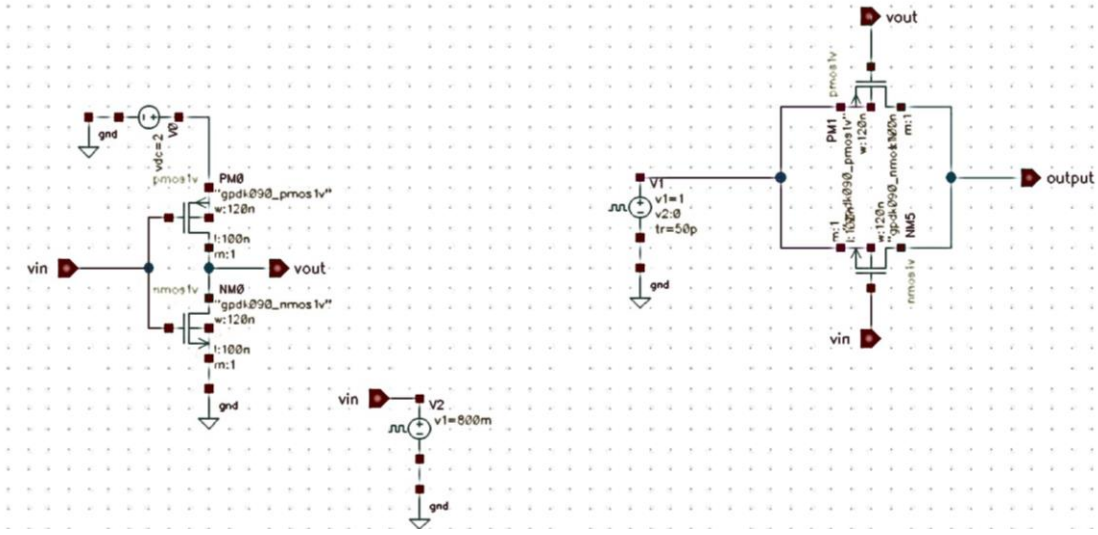


Fig: Transmission Gate schematic using pass transistor.

EDA Tool Setup:

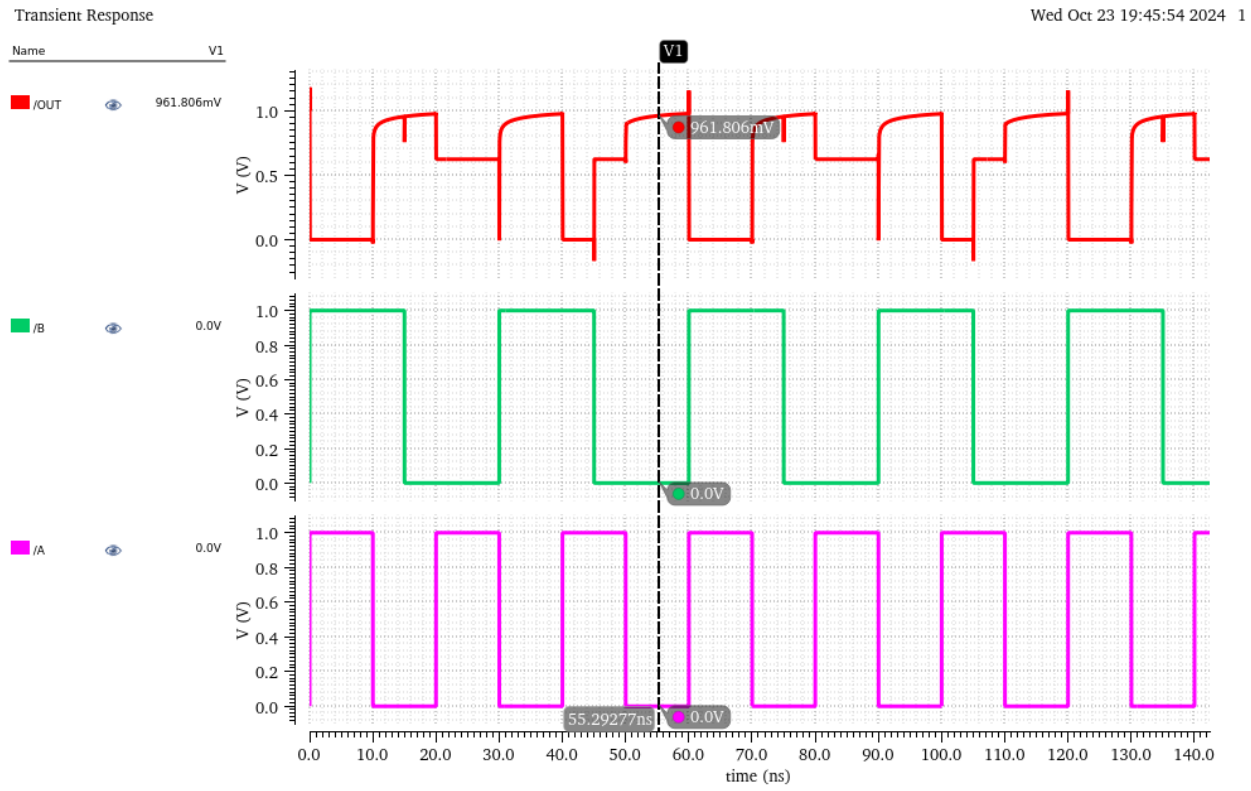
- **Schematic Creation**: Cadence Virtuoso in 90 nm technology.
- **Simulation**: ADL window for timing and functional tests.
- **PVT Analysis**: ADL XL for performance variation assessment using 180 nm and 65 nm process parameters. Making all transistor width parameter as Wn for Nmos and Wp for Pmos.

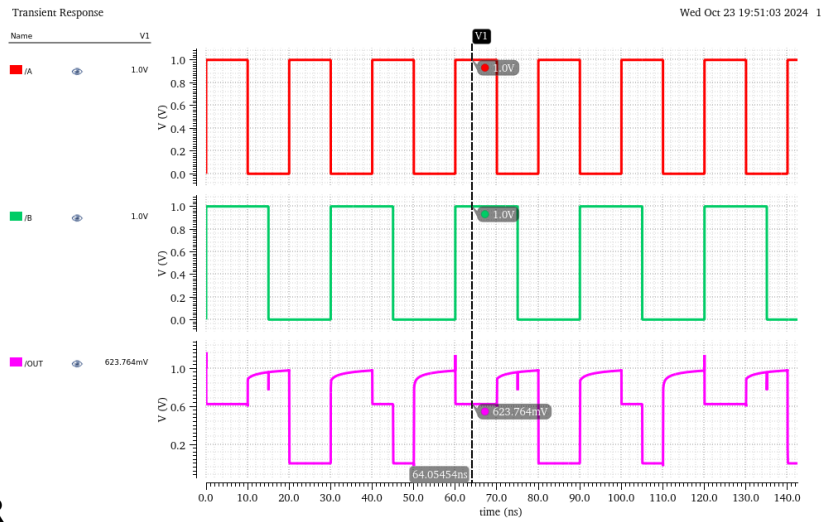
Experimental Results:

1. **DC Response**:
   - Measure and plot the voltage characteristics of PTL circuits.
   - Explain the behavior in terms of signal degradation and threshold levels.
2. **Transient Response**:
   - Display timing waveforms.
   - Discuss speed and efficiency compared to traditional CMOS logic.

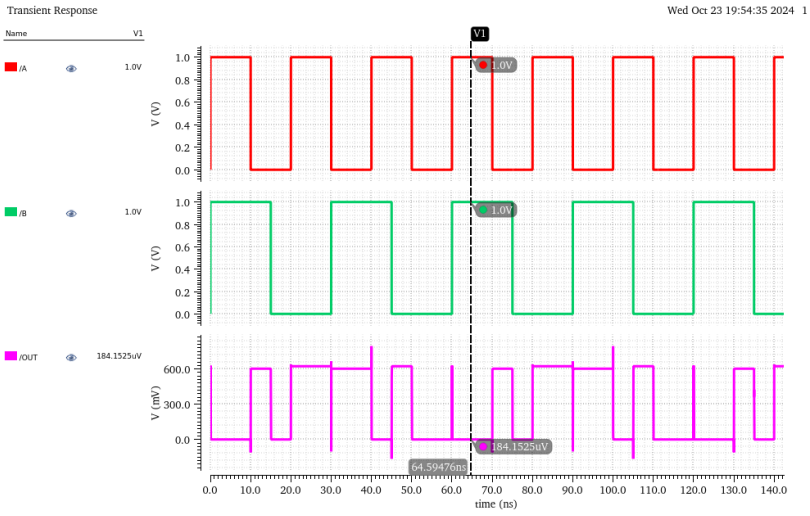
LOGIC_CIRCUIT USING PT LOGIC

NAND

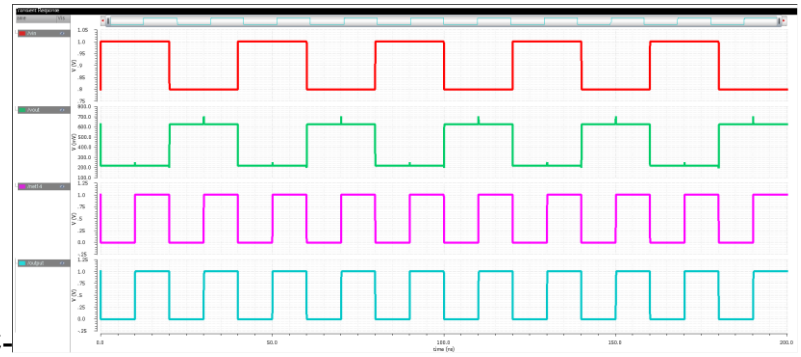




NOR



XOR



TG LOGIC-

Observations:

The circuits were created in 90 nm technology, tested, and analyzed using Cadence software. Performance assessments reveal when PTL or transmission gates are more effective, and the trade-offs associated with their use.

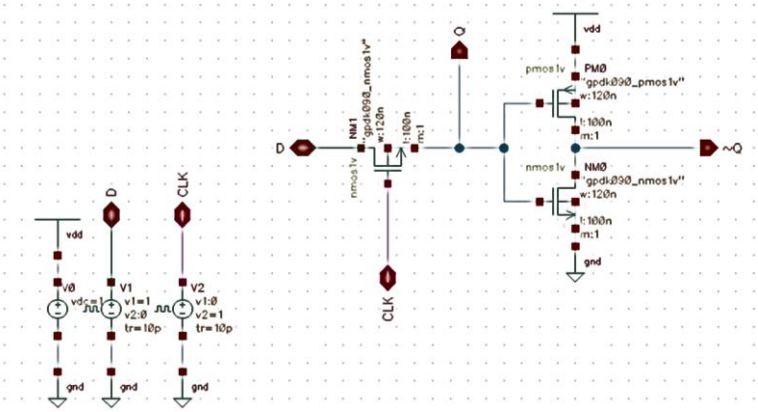
Design 4: Flip-Flops Using Pass Transistors

Objective:
To design and simulate various flip-flops (D, T, and Master-Slave configurations) using pass transistor logic, and evaluate their behavior.

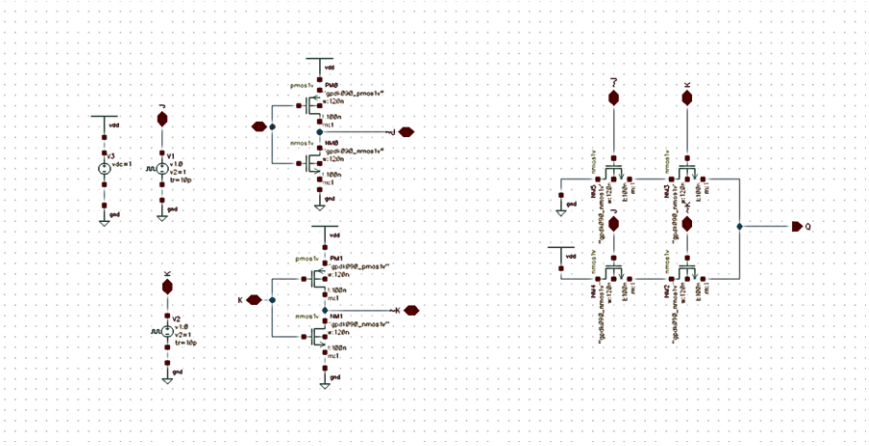
Circuit Description:
Flip-flops are fundamental memory elements used in sequential logic circuits. Using pass transistors, we explore efficient flip-flop designs with minimized transistor counts. The schematics were created in 90 nm technology, with PVT analysis performed using 180 nm and 65 nm processes. The focus is on understanding setup time, hold time, and overall performance.

Schematic:
Detailed schematics for D, T, and Master-Slave flip-flops were created in 90 nm technology using Cadence Virtuoso. Explain how pass transistors implement the required functionality.

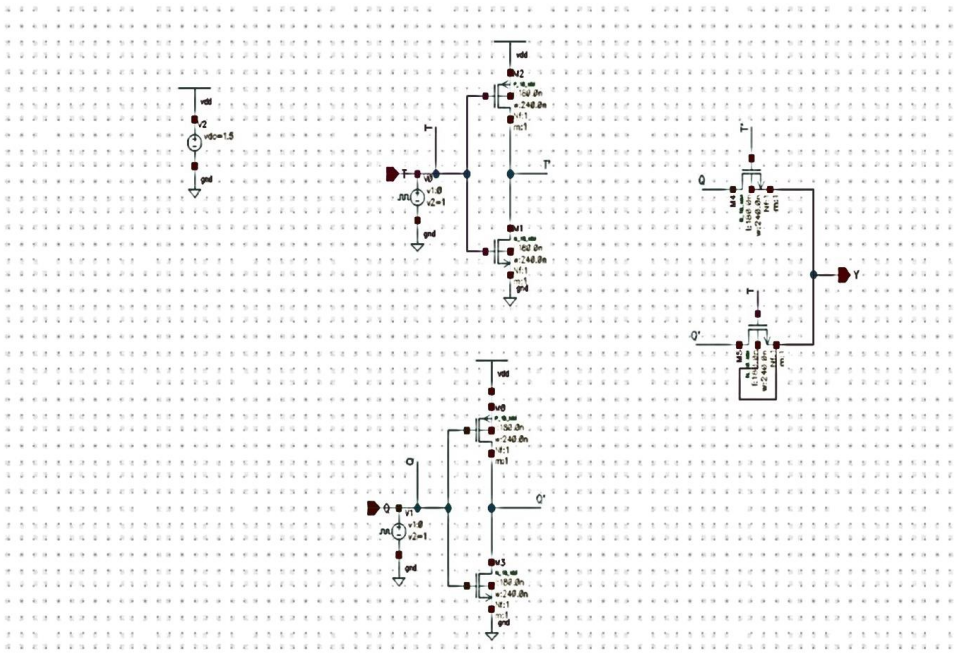
DFF USING PT LOGIC



MASTER_SLAVE JKTFF



T Flip Flop using Pass Transistor:



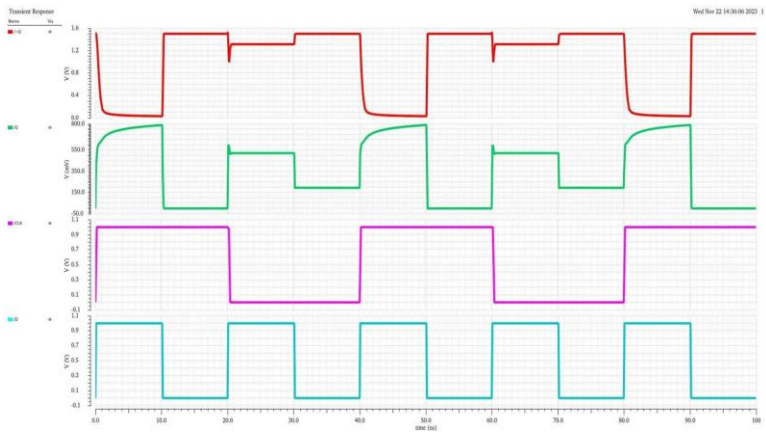
EDA Tool Setup:

- **Schematic Creation**: Cadence Virtuoso in 90 nm technology.
- **Simulation**: ADL window for capturing timing and functional behavior.
- **PVT Analysis**: ADL XL for examining variations using 180 nm and 65 nm process parameters. Making all transistor width parameter as Wn for Nmos and Wp for Pmos.

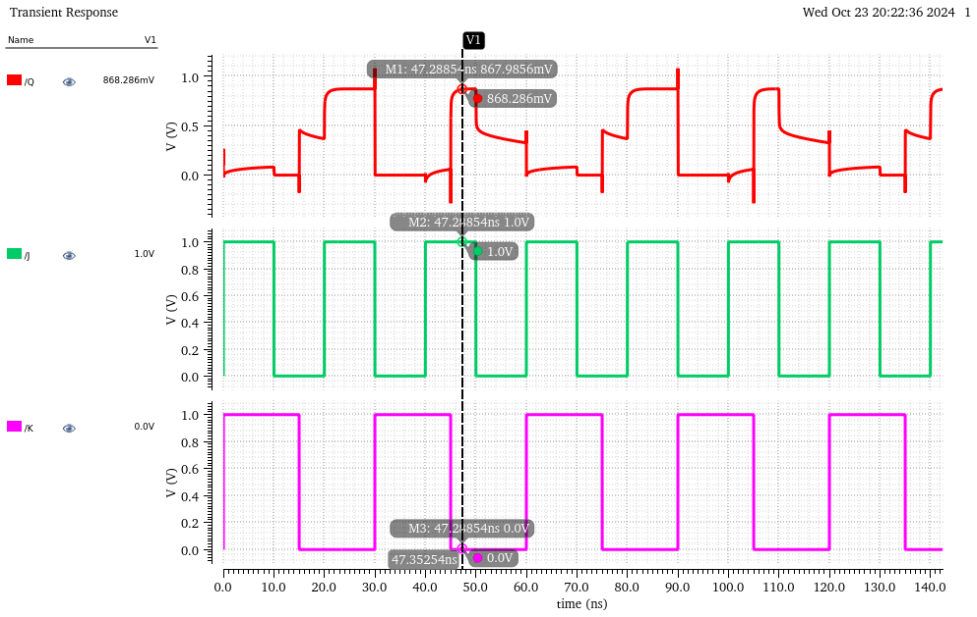
Experimental Results:

1. **Transient Response**:

DFF

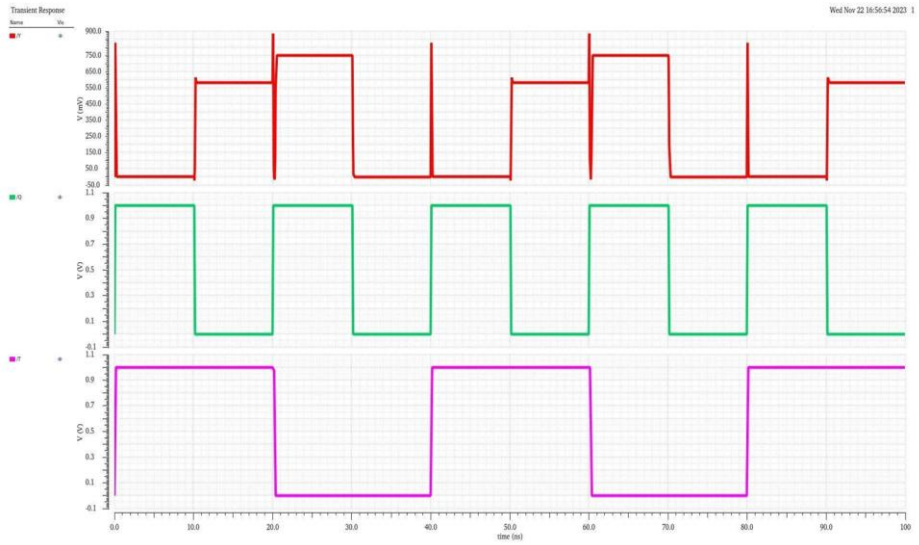


JKMS



T FF

Transient Response:



Observations:
The flip-flop circuits were created in 90 nm technology, tested, and analyzed using Cadence software according to design requirements.

All Flip Flops can be designed using pass transistor logic which reduces the number of transistor. Conclusion: The AIM of designing D, T, Master Slave JK Flip Flop and studying various characteristics is successful.