DIGITAL IC DESIGN LAB (EC1062)

LAB ASSIGNMENT - 4

Submitted By:

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Department: Microelectronics and VLSI

Submitted To:

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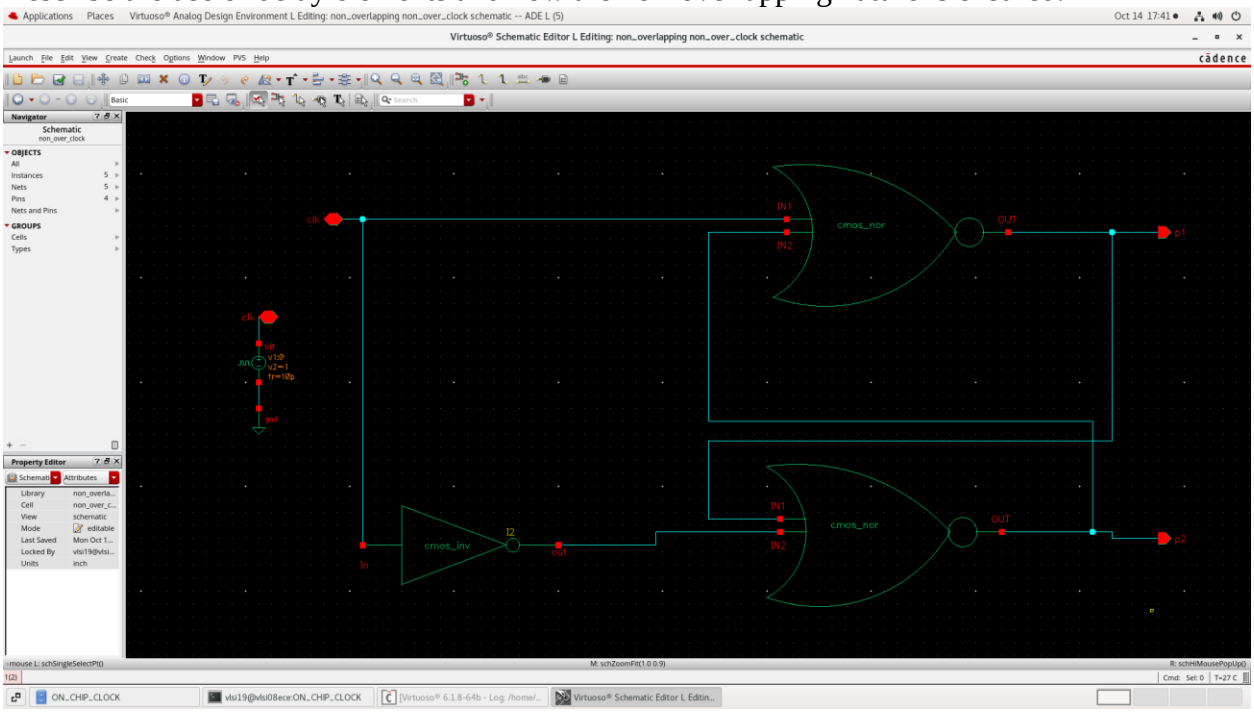
Submitted on-

Design 1: Two-Phase Non-Overlapping Clock Generator

Objective:
To design a two-phase non-overlapping clock generator and analyze its performance characteristics.

Circuit Description:
The two-phase non-overlapping clock generator produces two clock signals that do not overlap, ensuring safe operation in dynamic logic circuits. The design uses CMOS technology, with a focus on achieving minimum overlap while maintaining a consistent phase relationship.

Schematic:
The schematic for the clock generator was created in 90 nm technology using Cadence Virtuoso. Describe the use of delay elements and how the non-overlapping nature is ensured.

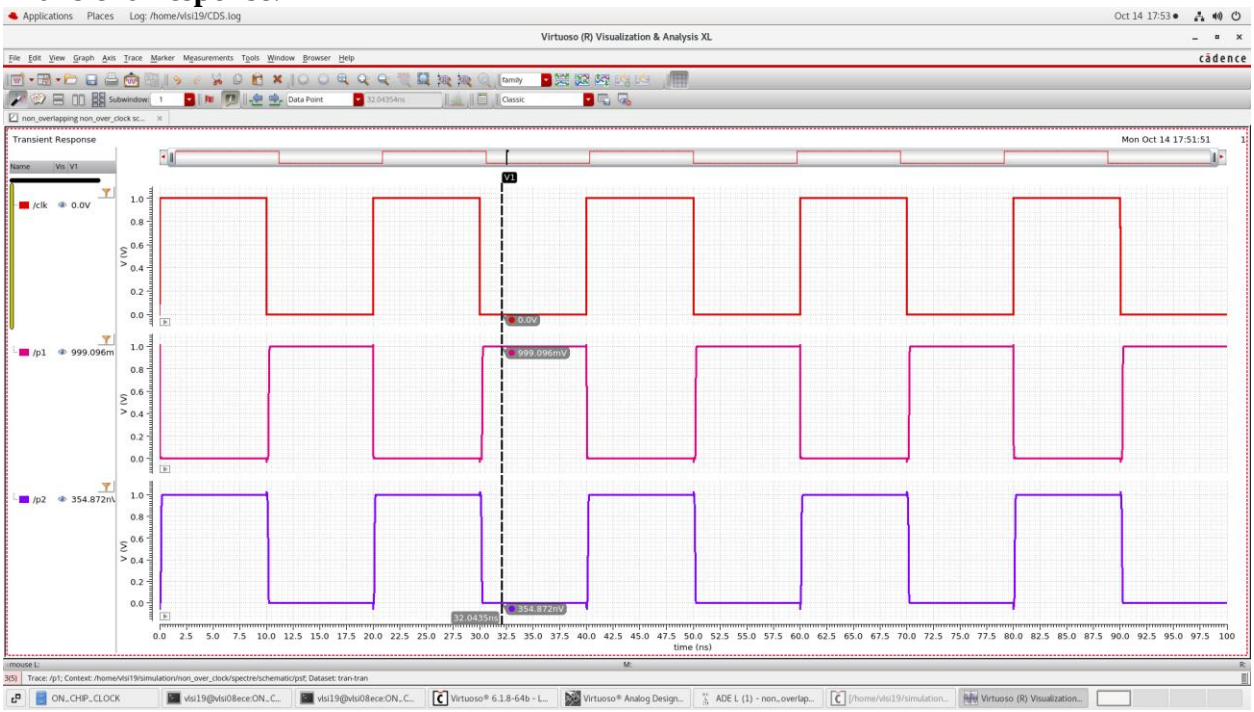


EDA Tool Setup:

- **Schematic Creation**: Cadence Virtuoso in 90 nm technology.
- **Simulation**: ADL window to verify non-overlapping properties.
- **PVT Analysis**: ADL XL using 180 nm and 65 nm process parameters to analyze performance under variations. Making all transistor width parameter as Wn for Nmos and Wp for Pmos.

Experimental Results:

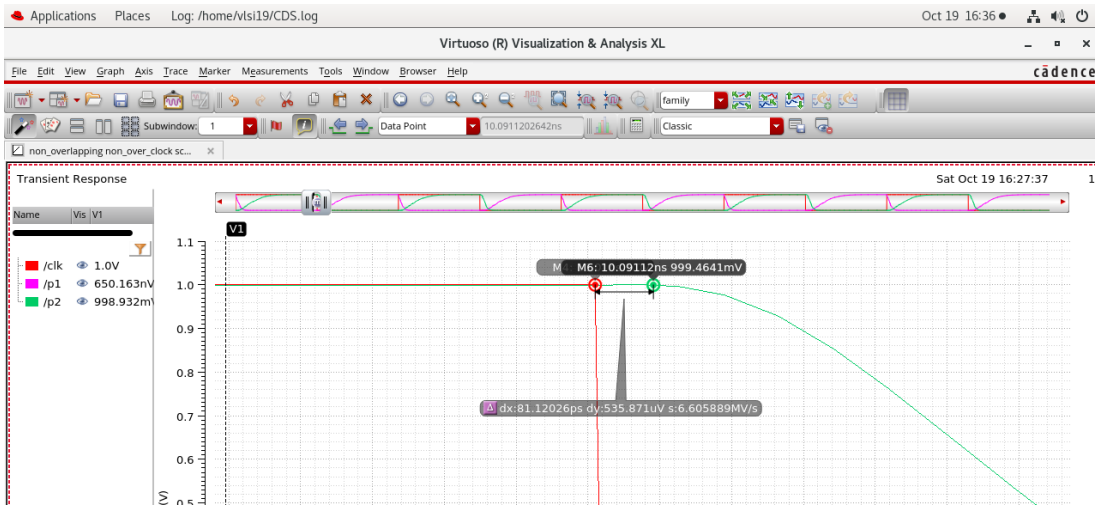
1. **Transient Response**:

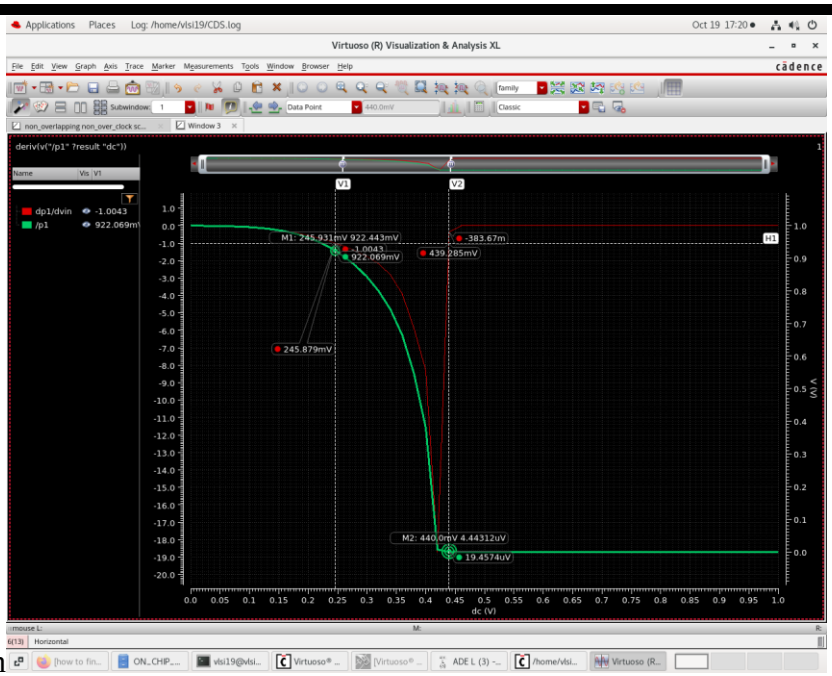


2. **Power Dissipation**:

   Pstatic= 665.4e-9, Pdynamic= 750.3e-6

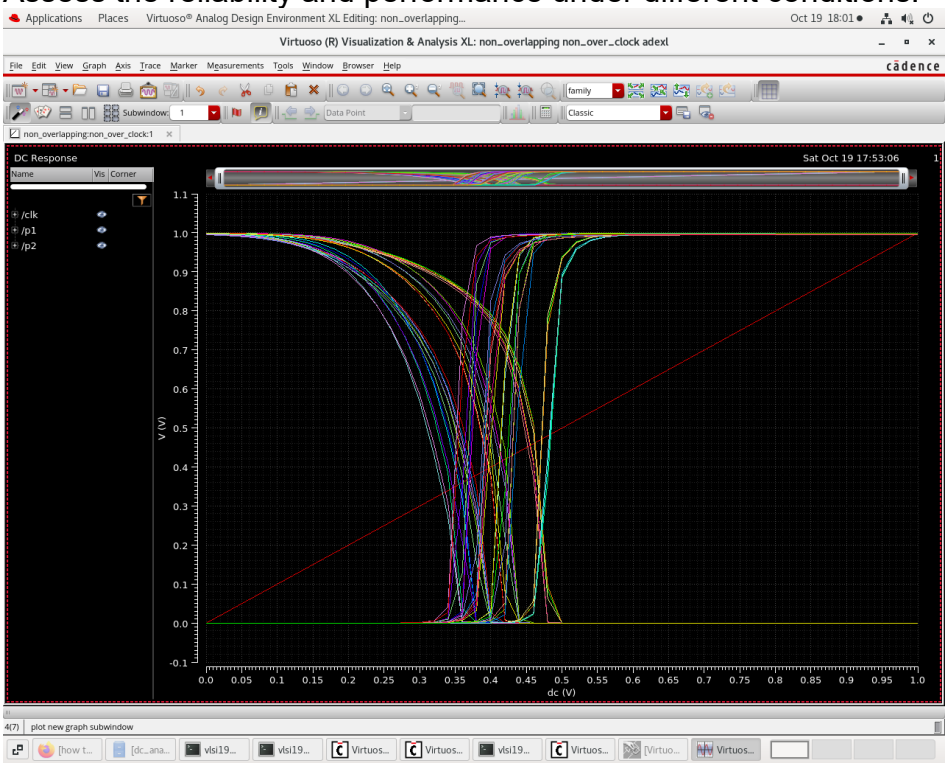
3. **Delay**: 81.12ps

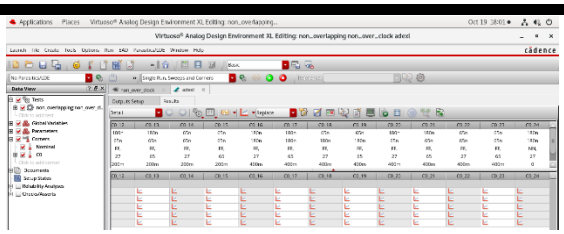




Noise margin

4. **PVT Analysis**:
   - Use 180 nm and 65 nm process parameters.
   - Assess the reliability and performance under different conditions.





Observations:
The clock generator circuit was created in 90 nm technology, tested, and analyzed using Cadence software. The design ensures robust clock generation with minimal overlap and stable operation under PVT variations.

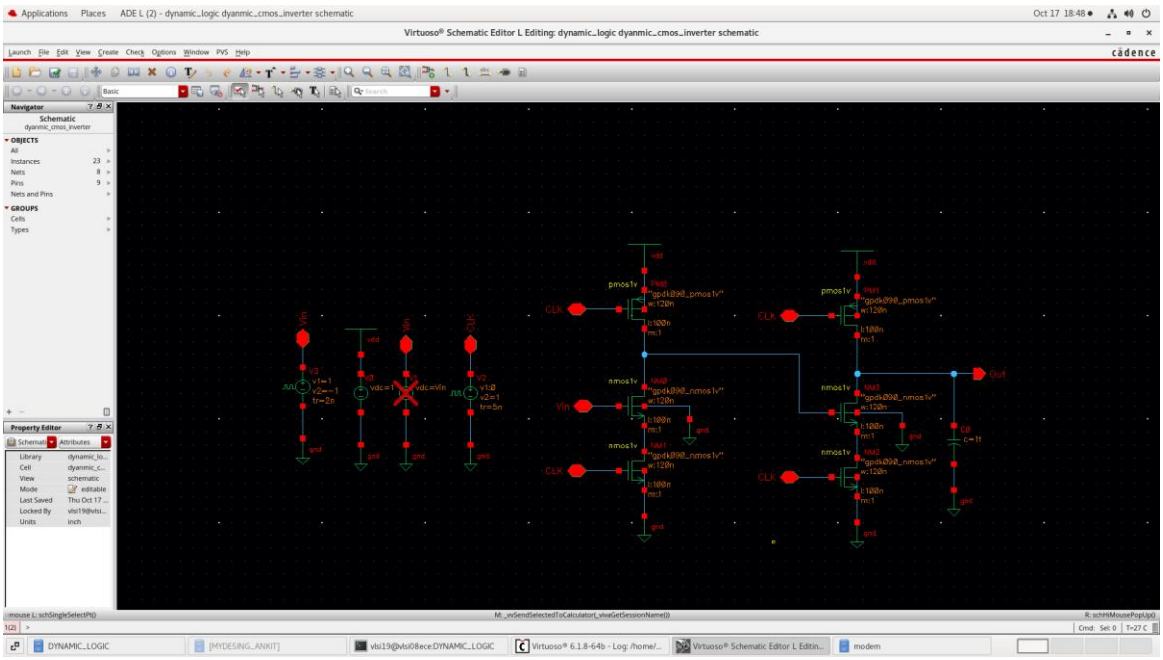
Design 2: Dynamic and Domino Logic Circuits

Objective:
To design and implement dynamic and domino logic circuits, and evaluate their performance.

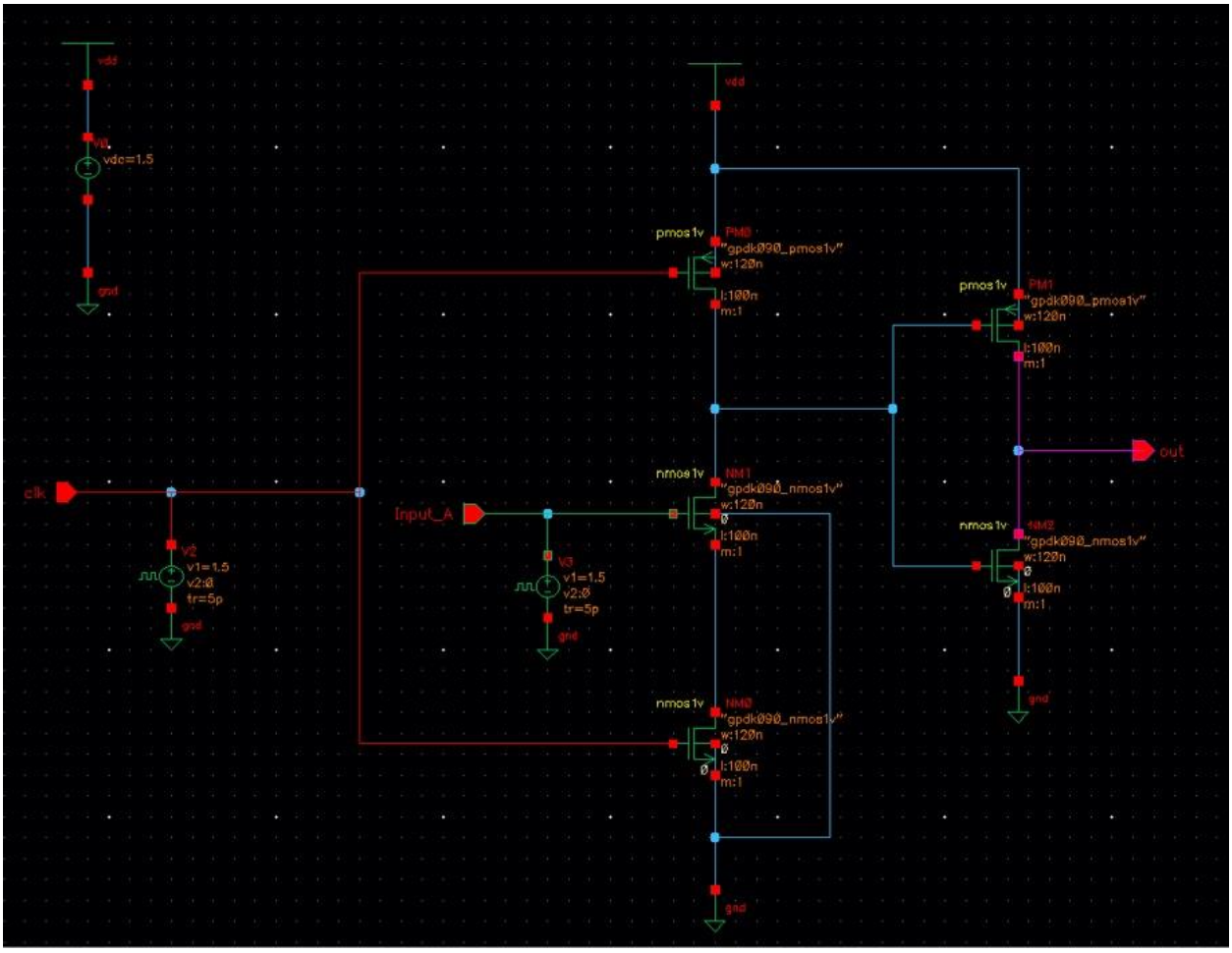
Circuit Description:
Dynamic and domino logic circuits use clocked precharge and evaluate phases to achieve high-speed operations. The design reduces transistor count and power consumption compared to static CMOS logic but requires careful clock management to avoid charge leakage and noise issues. Dynamic logic uses a single-phase clock and a simple pull-down network, alternating between precharge and evaluate phases, making it efficient in terms of speed and area but prone to noise and charge-sharing issues. Domino logic enhances dynamic logic by adding an inverter at the output, which improves stability and noise immunity, allowing multiple logic stages to be reliably cascaded like falling dominos.

Schematic:
The schematics for dynamic and domino logic circuits were created in 90 nm technology using Cadence Virtuoso.

DYNAMIC-



DOMINO-

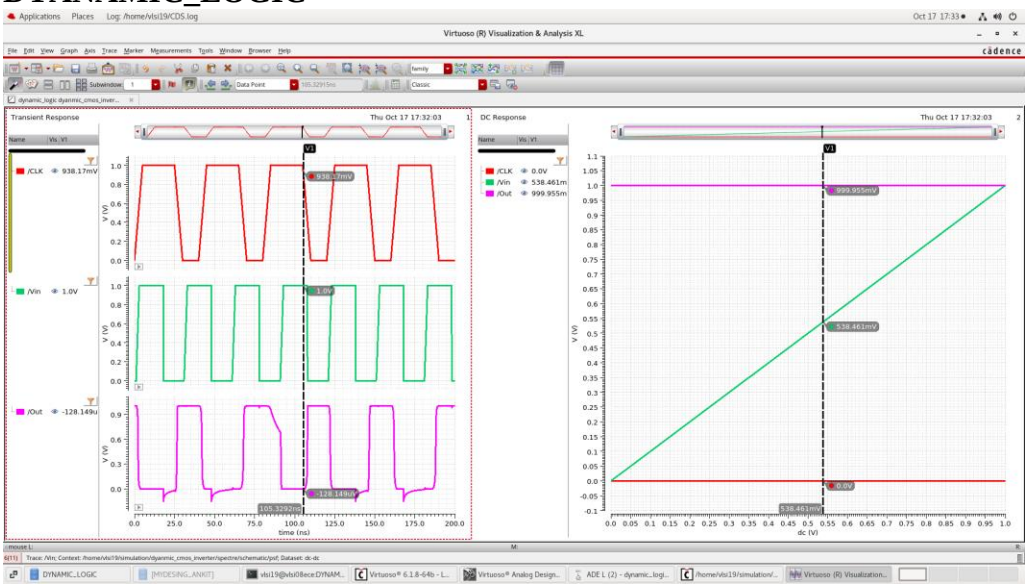


EDA Tool Setup:

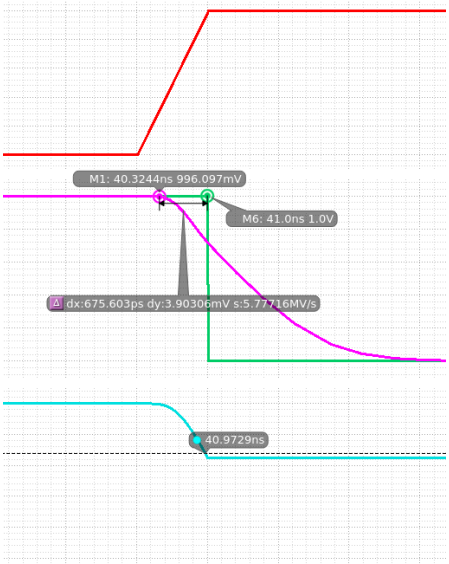
- **Schematic Creation**: Cadence Virtuoso in 90 nm technology.
- **Simulation**: ADL window to check the functionality during precharge and evaluate phases.
- **PVT Analysis**: ADL XL using 180 nm and 65 nm process parameters to evaluate variations. Making all transistor width parameter as Wn for Nmos and Wp for Pmos.

Experimental Results:

DYANAMIC_LOGIC-

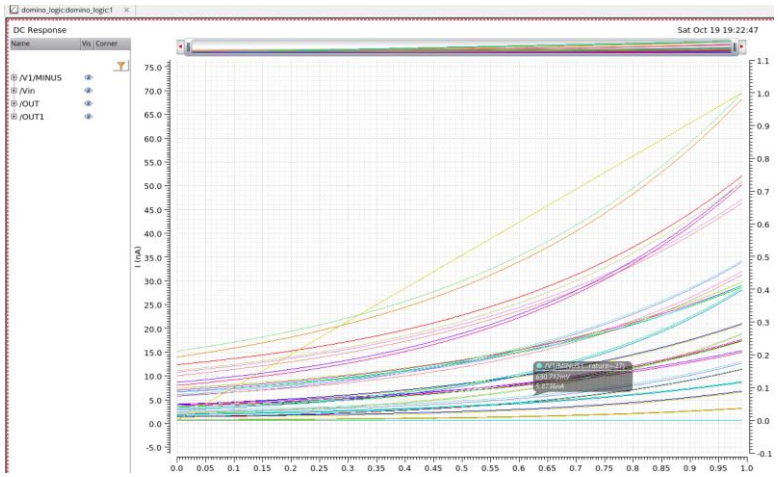


Delay-675.60ps

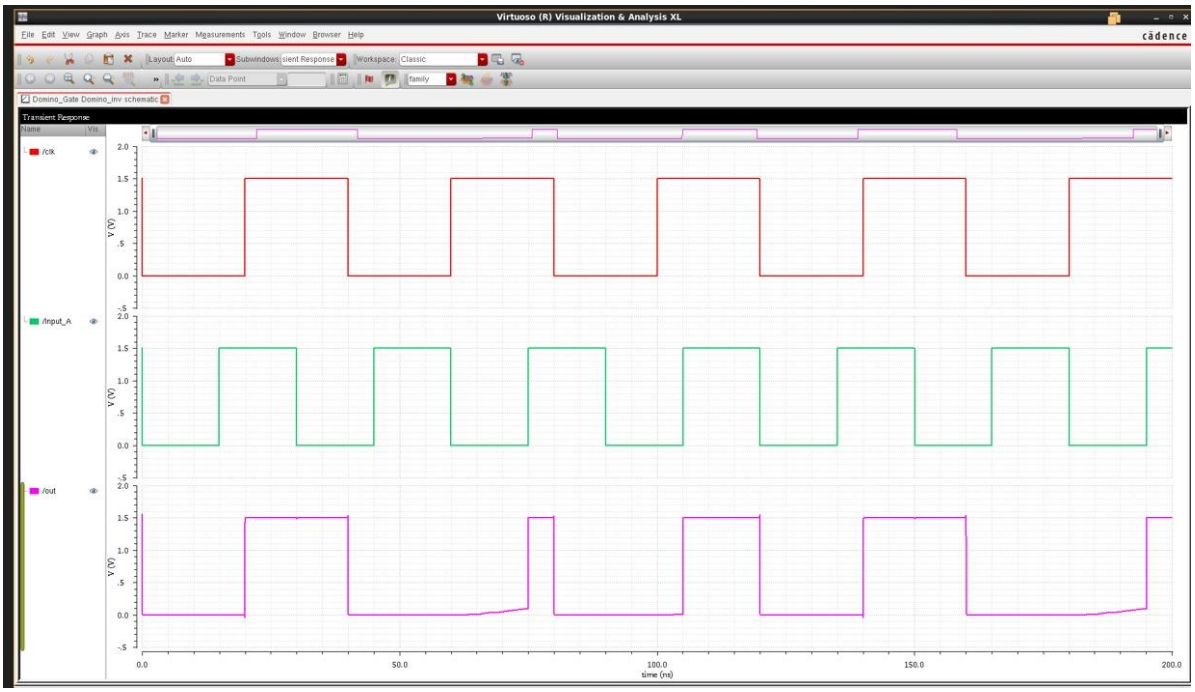


Power dissipation-770.4E-9

PVT –



DOMINO_LOGIC-



DELAY – 2.461E-9s
POWER DISIPATION-Pdynamic = 2.909E-6w, Pstatic = 5.818e-6

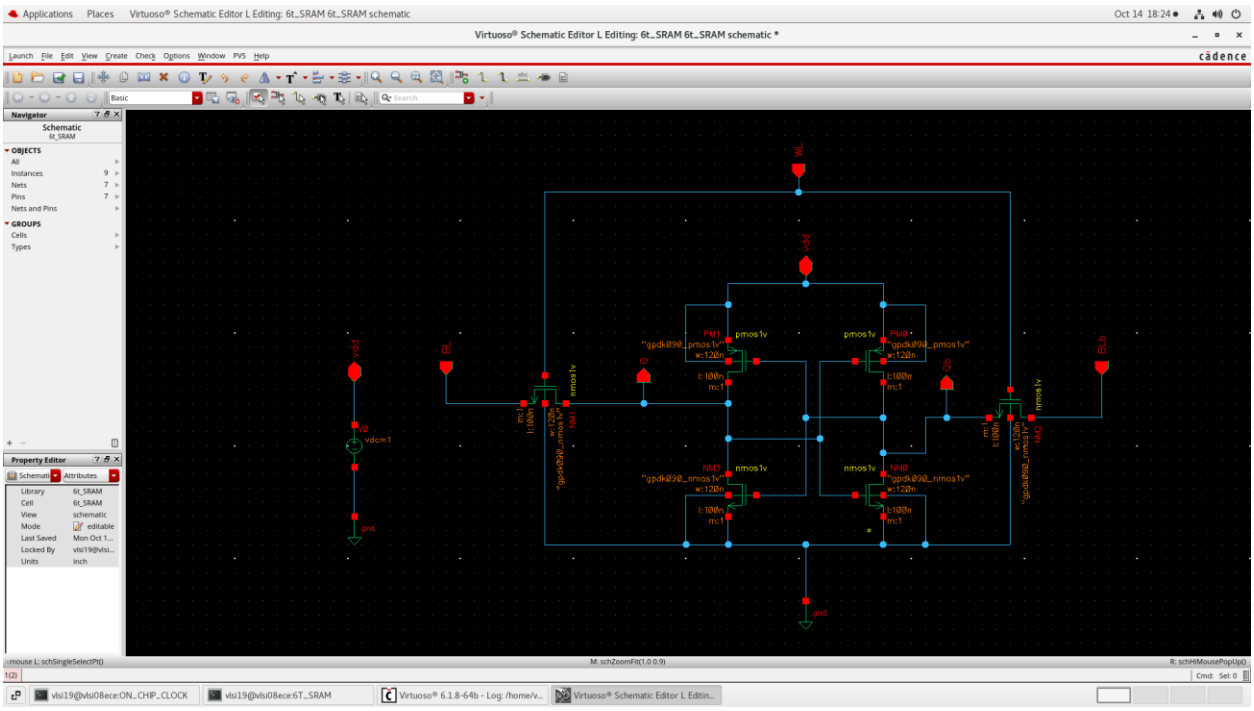
Observations:
The dynamic and domino logic circuits were created in 90 nm technology, tested, and analyzed using Cadence software. The design demonstrates high-speed operation with trade-offs in power and noise susceptibility.

Design 3: 6T SRAM Cell

Objective:
To design a 6T SRAM cell and measure its characteristics, including stability, power consumption, and performance.

Circuit Description:
The 6T SRAM cell uses six transistors (two cross-coupled inverters and two access transistors) to store a single bit of data. The design focuses on read/write stability, power efficiency, and performance in memory applications.

Schematic:
The 6T SRAM cell schematic was created in 90 nm technology using Cadence Virtuoso. Describe how the cell performs read and write operations and the role of each transistor in data retention.

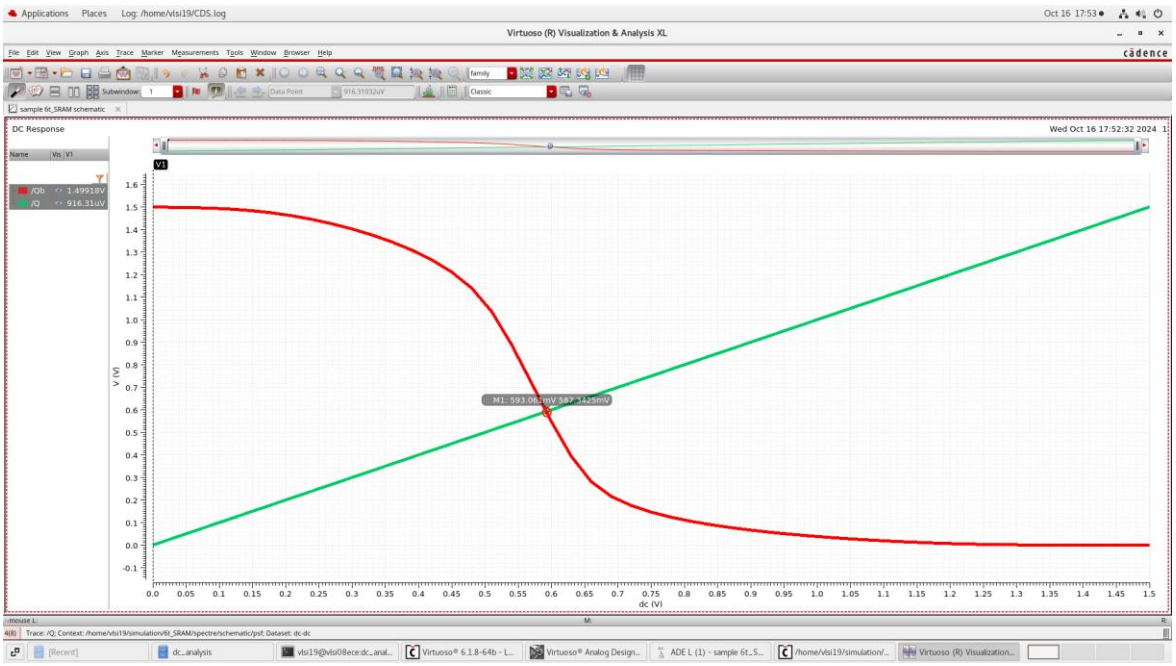


EDA Tool Setup:

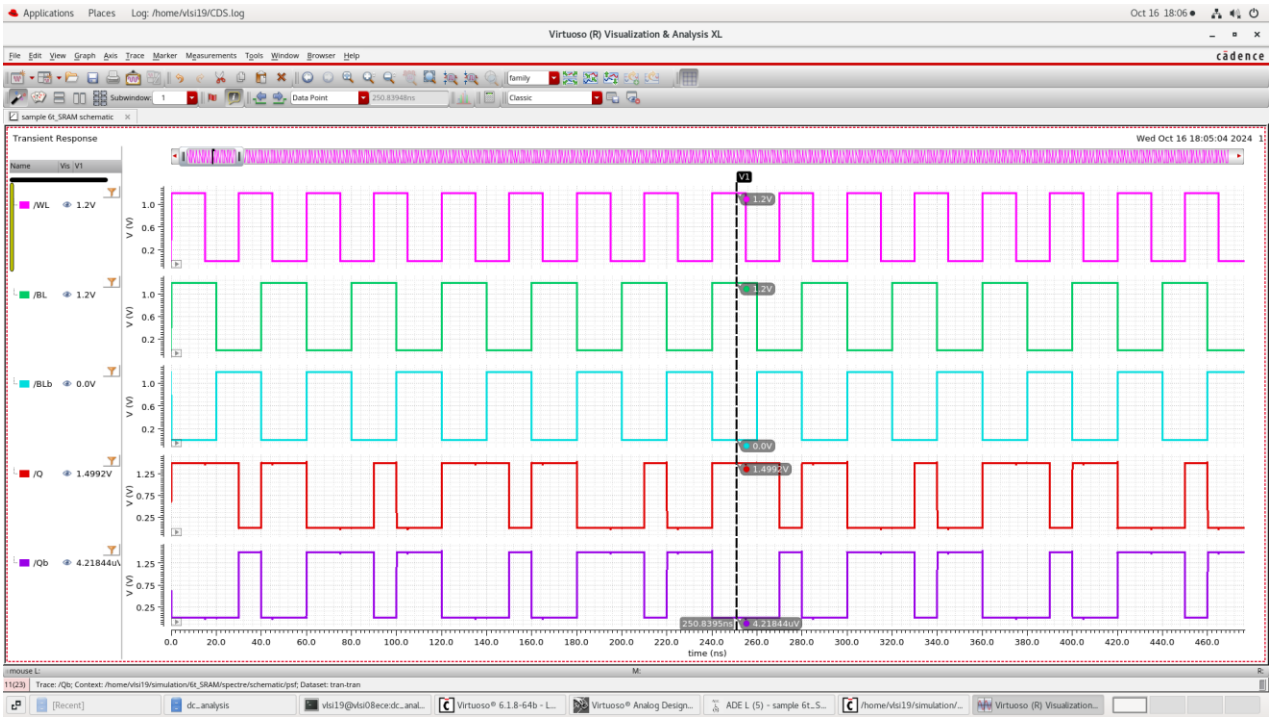
- **Schematic Creation**: Cadence Virtuoso in 90 nm technology.
- **Simulation**: ADL window for analyzing read and write operations, hold.
- **PVT Analysis**: ADL XL using 180 nm and 65 nm process parameters to test stability and performance. Making all transistor width parameter as Wn for Nmos and Wp for Pmos.

Experimental Results:

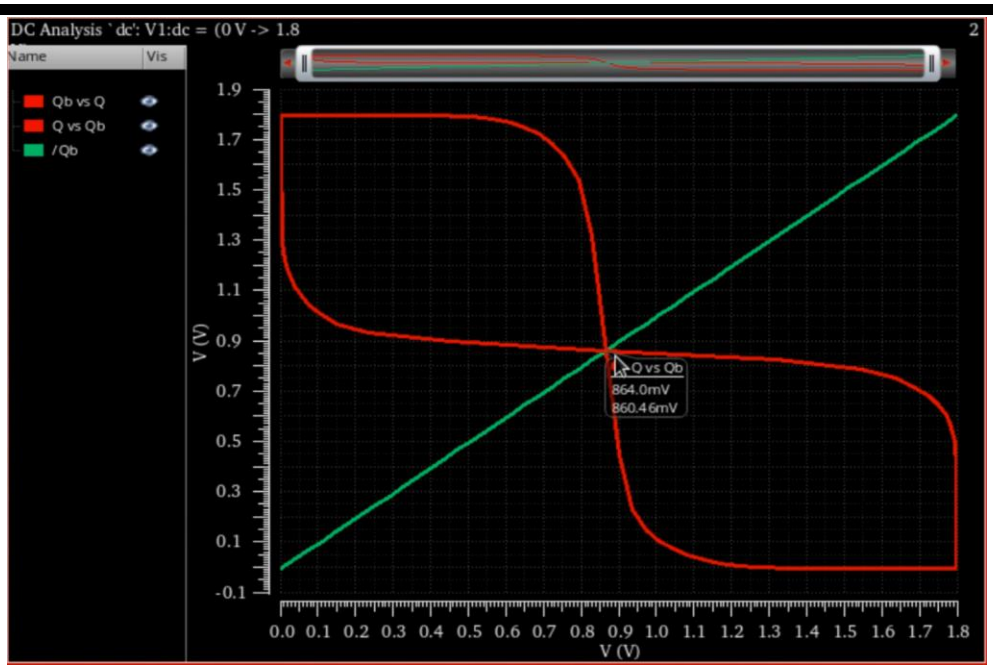
1. **DC Response**:

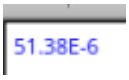


2. **Transient Response**:

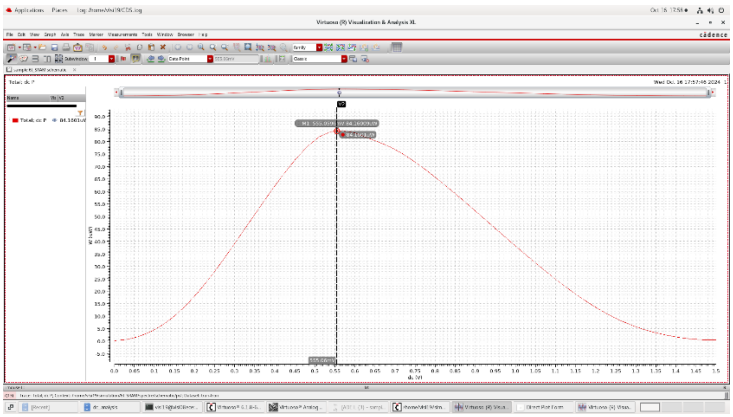


3. **Noise Margine- BUTTERFLY CURVE**

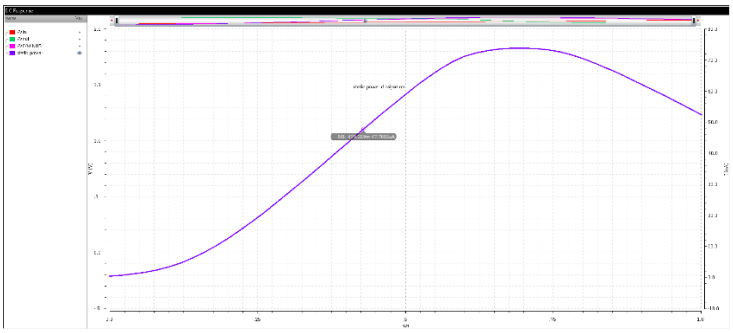


4. **Power Dissipation**: Pdyanmic = 51.3e-6, 

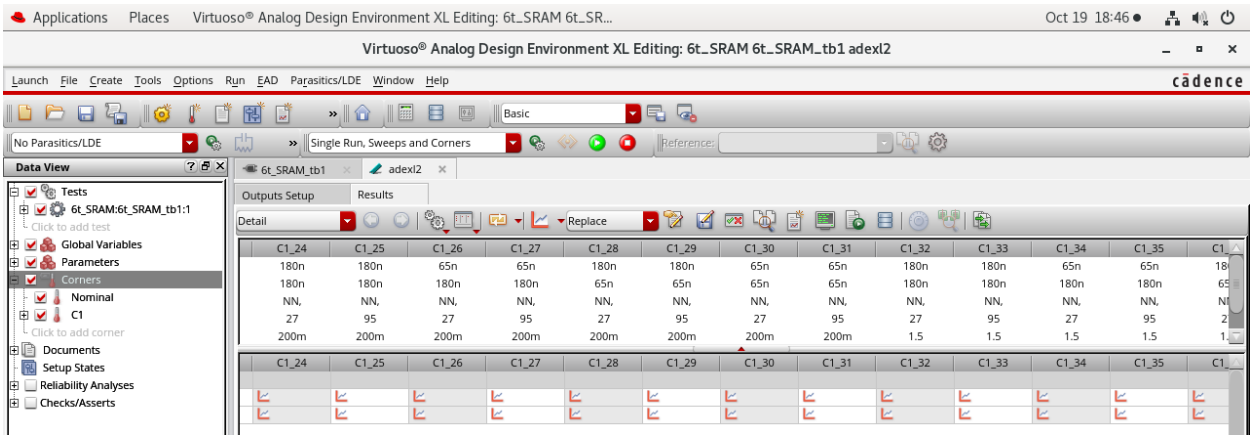
dynamic Power Dissipation of CMOS:

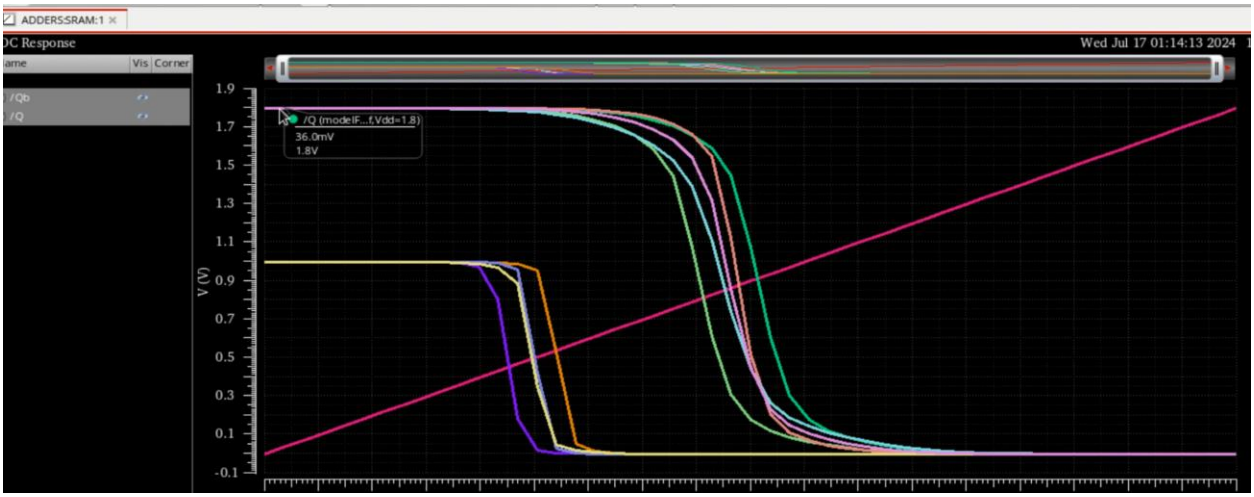


Static Power Dissipation of CMOS:



5. **Delay**: 20.03E-9 20.3e-9
6. **PVT Analysis**:
   - Use 180 nm and 65 nm process parameters.
   - Evaluate the SRAM cell's stability under varying conditions.





Observations:
The 6T SRAM cell was created in 90 nm technology, tested, and analyzed using Cadence software. The design successfully balances speed, power, and stability, with performance verified under PVT variations.

Design 4: Layout of CMOS Inverter and Transmission Gate

Objective:
To draw and verify the layout of a CMOS inverter and a transmission gate using Cadence Virtuoso.

Circuit Description:
The CMOS inverter and transmission gate are fundamental components used in digital design. The layout process ensures the physical implementation adheres to design rules for optimal performance and manufacturability.

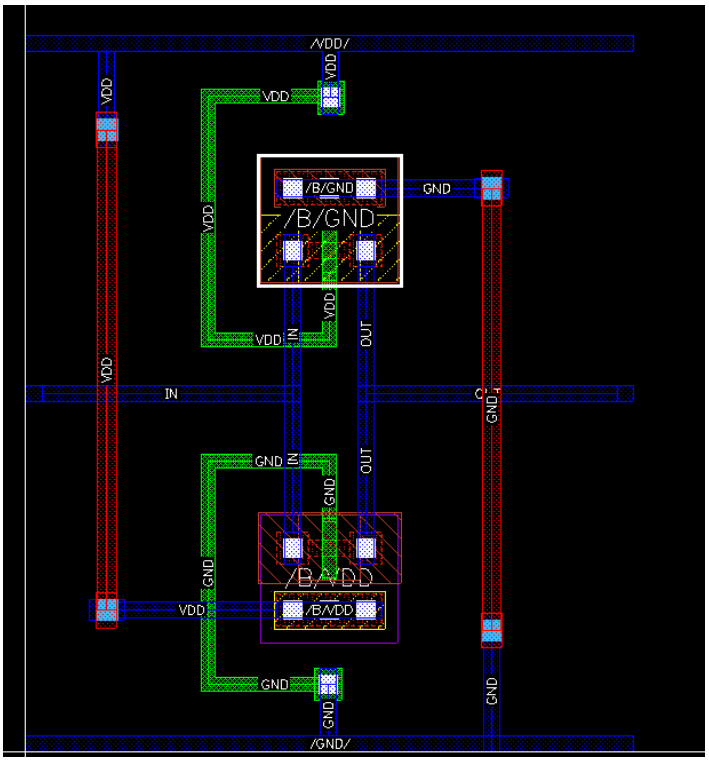
Layout Design:
The layouts for the CMOS inverter and transmission gate were created using Cadence Virtuoso. Discuss the layout strategies used to minimize parasitic effects and ensure design rule compliance.

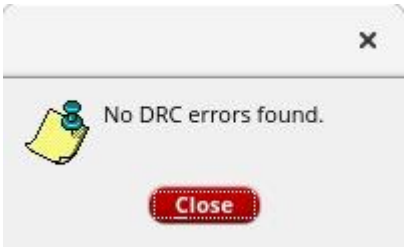
EDA Tool Setup:

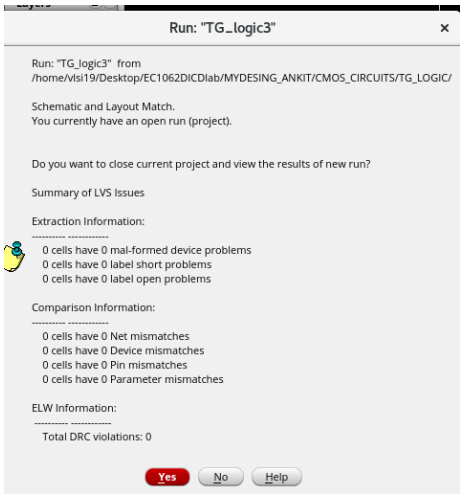
- **Layout Creation**: Cadence Virtuoso.
- **DRC and LVS Checks**: Performed to ensure design rule compliance and correct connectivity. IN RUN Assura DRC check

Experimental Results:

TG LOGIC



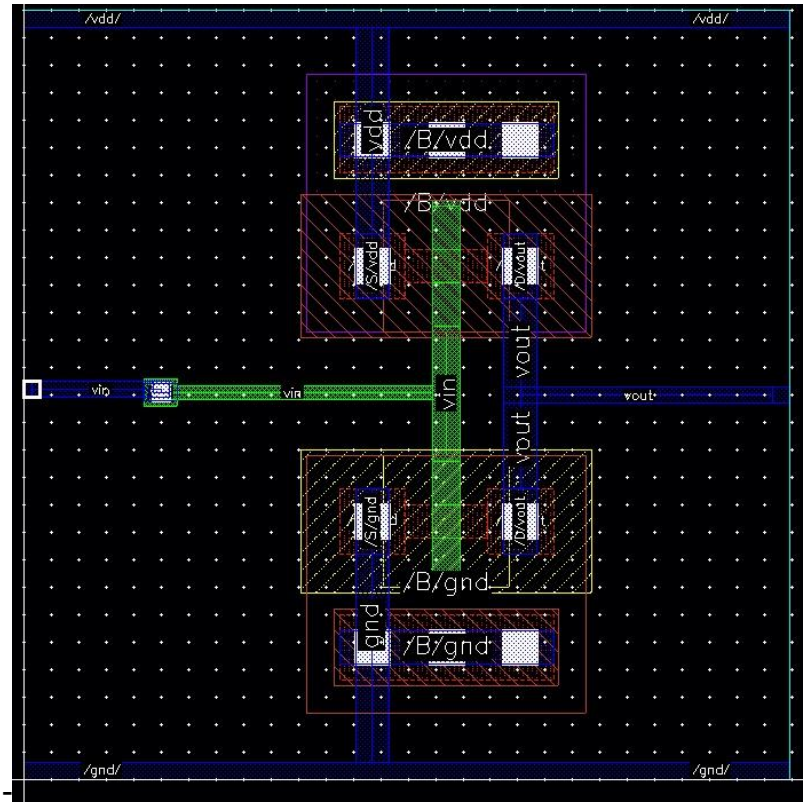


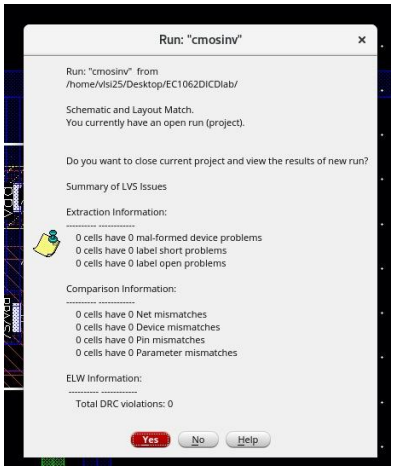


Parasitic Analysis: Ploted the impact of parasitic capacitance and resistance.using Quantus.

```
Summary for TG_Parasitic_compTG_logic/TG_logic3_rcx/av_extracted

instance count totals:

    lib             cell            view                total
    analogLib       pcapacitor      symbol                 11
    analogLib       presistor       symbol                 18
    gpdk090         nmos1v          ivpcell                 1
    gpdk090         pmos1v          ivpcell                 1


Summary for TG_logic/TG_logic3/av_extracted
```

CMOS INVERTER LOGIC





Observations:

The layouts for the CMOS inverter and transmission gate were successfully created and verified using Cadence Virtuoso. The design meets all DRC and LVS requirements, ensuring readiness for fabrication.