

10.1 INTEL 8051 SERIES OF MICROCONTROLLERS (MCS-51)

The 8051 series of microcontrollers were developed in the year 1980. They are the second generation of 8-bit microcontrollers. They are faster and more powerful than Intel 8048 series (1976) of microcontrollers. They have been provided with improved instruction set and contain a number of additional electronic circuitry for specific functions. The 8-bit microcontrollers are used for a variety of applications involving limited calculations and relatively simple control strategies. They are used for industrial and commercial control applications, appliances control, instrumentation, etc. The 8051 contains Boolean processor, full duplex serial port and power saving circuitry in addition to essential components such as 8-bit CPU, RAM, ROM/EPROM/OTPROM, timer/counter and parallel I/O lines. This series has a wide variety of versions with some of special functions such as DMA channels, A/D converter, pulse-width modulation, watch-dog timer, etc. Table 10.1 shows the details of its family members.

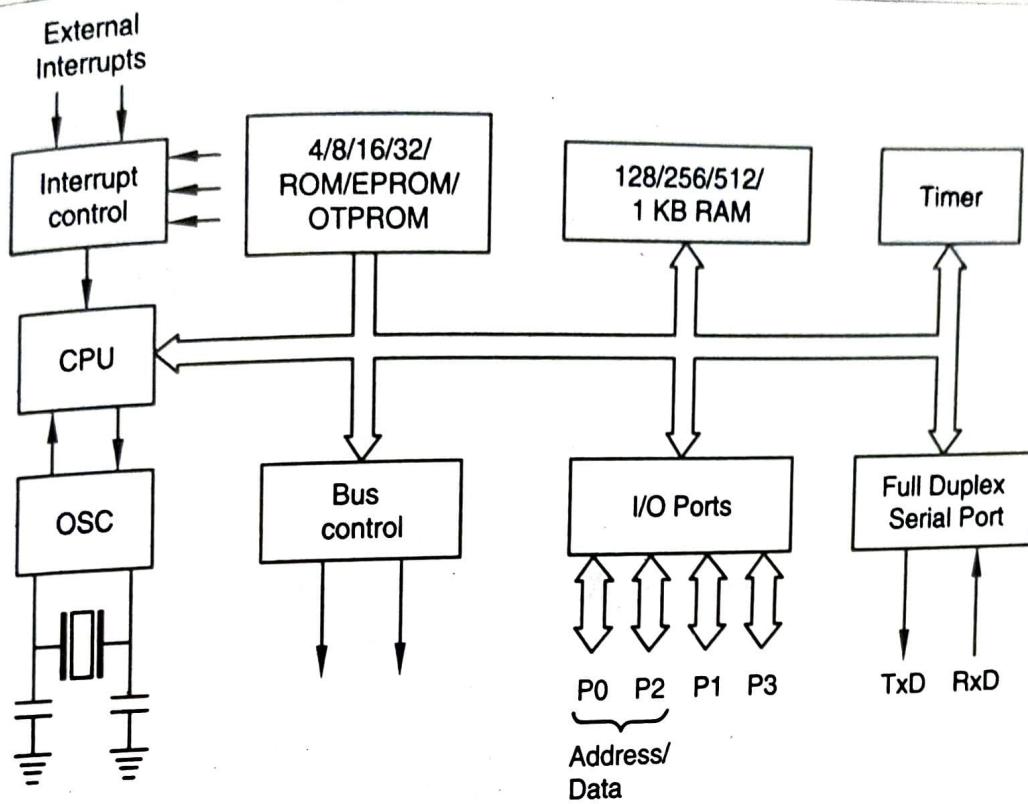


Fig. 10.1 Block Diagram of Intel 8051.

Fig. 10.1 shows the block diagram of Intel 8051. The common features of 8051 series of microcontrollers are :

- (i) 8-bit CHMOS CPU
- (ii) Most of the microcontrollers of 8051 family contain 256 bytes on-chip RAM which acts as data memory. The 8XC51RA/RB/RC and 8XC251SP/SQ contain 512 bytes, and the 8XC251SA/SB contains 1 KB RAM. A few entry level microcontrollers such as 80C51BH, 80C31BH and 87C51 contain 128 bytes RAM.
- (iii) 4/8/16/32 KB ROM/EPROM/OTPROM. The capacity varies from version to version, see Table 10.1. ROMless versions are also available. In case of ROMless versions external program memory is used. The capacity depends on the particular application.
- (iv) Most of the microcontrollers contain 3 multimode 16-bit timer/counters. The 8XC152JA/JB/JC, 80C51BH, 80C31BH and 87C51 contain 2 timers/counters.
- (v) Most of the microcontrollers contain 32 I/O lines i.e. four 8-bit ports. The 8XC152JA/JB/JC/JD, the universal communication controller contains 5 or 7 I/O ports. The 8XC51SL, keyboard controller contains 3 multifunction I/O ports.
- (vi) Boolean processing (single-bit logic) capabilities. It is needed in industrial control applications.
- (vii) Multimode, full duplex serial port. The 8XC152JA/JB/JC/JD contains UART.
- (viii) The number of interrupt sources differs from version to version. It may be 5, 6, 7, 10 or 15. Four-level interrupt priority has been provided. The important interrupt sources are : one

- from the serial port when a transmission or reception is complete, two from timers, two from input pins INT0 and INT1, etc.
- (ix) 64 KB external data memory space.
 - (x) 64 KB external program memory space.
 - (xi) Power saving modes.

Some versions are designed for specific applications, and therefore, they are provided with special features required by the typical applications. Special features are :

- (i) Pulse-width modulation. A few versions have this feature, for example, 8XC51FA/FB/FC, 8XC51GB, 8XC151SA/SB and 8XC251SA/SB/SP/SQ.
- (ii) DMA channel. A few versions have this feature, for example 8XC152JA/JB/JC/JD.
- (iii) A/D converter. A few versions have A/D converter, for example, 8XC51GB.
- (iv) Watchdog-timer. It is a dedicated internal timer which resets the system when the software does not operate properly. Some versions have been provided with this feature, for example, 8XC51GB, 8XC51RA/RB/RC, 8XC151 and 8XC251.
- (v) Programmable counter array to provide features like high-speed output, compare/capture operation, etc. Some versions have this feature, for example, 8XC51FA/FB/FC, 8XC51GB, 8XC151 and 8XC251.

The 8051 microcontrollers have two versions : COMMERCIAL and EXPRESS. The operating temperature range for commercial versions is 0°C to 70°C and that for the express version is 40°C to +85°C.

10.1.1 Registers

The 8051 is an accumulator based microcontroller. Its registers are : register A (an accumulator), PSW, register B, 8-bit stack pointer, 16-bit data pointer, program counter, program address register, 16-bit timer registers for timer/counters, instruction register, control registers, RAM address register, serial data buffer, capture registers, special function registers, etc. Register B is used during multiply and divide operations. For other instructions it is used as another scratch pad register. The data pointer consists of a high byte and a low byte. It holds 16-bit address. It can be used as a 16-bit register or two independent 8-bit registers. The serial data buffer is actually two separate registers : a transmit buffer and a receive buffer register.

The 8051 has been provided with 4 banks of working registers. Each bank consists of 8 working registers, R0-R7. Physically these banks occupy the first 32 bytes of on-chip data RAM (address 0-1F hex). Only one bank is active at a time. Bits 3 and 4 of PSW decide which bank is to be made active. As the 8051 is a bit as well as byte microcontroller, some of its registers are both bit as well as byte addressable.

Besides working registers, there are a number of special function registers (SFRs). Some of SFRs are both bit-and byte-addressable. A list of SFRs is given below:

Symbol	Name	Address	Remarks
ACC	Accumulator	E0	Both bit-and byte-addressable
B	B register	F0	do
PSW	Program Status Word	D0	do
SP	Stack Pointer	81	—
DPTR	Data Pointer (DPH & DPL)	83 and 82	Consists of DPH and DPL
P0	Port 0	80	Both bit-and byte-addressable
P1	Port 1	90	do

P2	Port 2	A0	do
P3	Port 3	B0	do
IP	Interrupt Priority Control	B8	do
IE	Interrupt Enable Control	A8	do
SCON	Serial Control	98	Both bit-and byte-addressable
SBUF	Serial Data Buffer	99	—
PCON	Power Control	97	—
TMOD	Timer/Counter 0&1 Mode Control	89	—
T2CON	Timer/Counter 2 Control	88	Both bit-and byte-addressable. It is in 8052 only.
TCON	Timer/Counter 0&1 Control	C8	—
TL0	Timer/Counter 0 (low byte)	8A	—
TH0	Timer/Counter 0 (high byte)	8C	—
TL1	Timer/Counter 1 (low byte)	8B	—
TH1	Timer/Counter 1 (high byte)	8D	—
TL2	Timer/Counter 2 (low byte)	CC	—
TH2	Timer/Counter 2 (high byte)	CD	—
RCAP2L	Timer/Counter 2 Capture Register (low byte)	CA	—
RCAP2H	Timer/Counter 2 Capture Register (high byte)	CB	—

Description of some registers are given below:

Data Pointer. It consists of DPH (a high byte) and DPL (a low byte). It holds 16-bit address. It can be used as a 16-bit register or as two independent 8-bit registers.

P0, P1, P2 and P3. These are SFR latches for Port 0, 1, 2 and 3 respectively.

Serial Data Buffer. It consists of two separate registers, a transmit buffer register and a receive buffer register.

Timer Registers. (TL0, TH0), (TL1, TH1) and (TL2, TH2) are register pairs. These register pairs are 16-bit counting registers for Timer/Counter 0, 1 and 2 respectively.

Capture Registers. RCAP2L and RCAP2H is a register pair. These registers are capture registers for the Timer2 capture mode.

Control Registers. Special Function Registers IE, IP TMOD, TCON, T2CON and SCON hold control and status bits for the interrupt system, timer/counters, and the serial port. PCON is power control register. The 8051 is provided with power-saving modes of operation. For applications where power consumption is critical, both HMOS and CMOS versions provide reduced power modes of operation. For CMOS version of the 8051 microcontroller, the reduced power modes, Idle and Power Down modes are the standard features. In HMOS versions only reduced power mode is available.

PSW (Program Status Word). PSW register contains program status information as shown in Fig. 10.2. Its bits are indicated as PSW.0, PSW.1, PSW.2,.....,PSW.7.

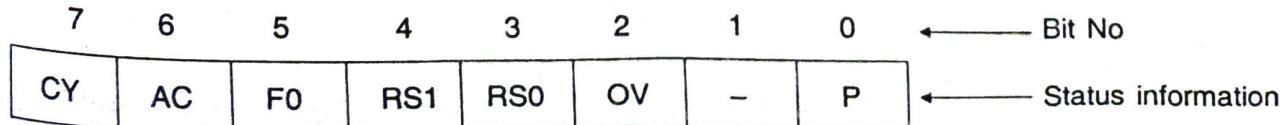


Fig. 10.2 PSW: Program Status Word Register

Bit No. 0, PSW.0. It is for parity status (parity flag, P)

Bit No. 1, PSW.1. Reserved

Bit No. 2, PSW.2. Overflow flag (OV)

Bit No. 3, PSW.3. (RS0) These bits are to select working register bank.

Bit No. 4, PSW.4. (RS1)

Bit No. 5, PSW.5. It is flag 0 (F0) available to users for general purpose.

Bit No. 6, PSW.6. It is auxiliary carry flag (AC)

Bit No. 7, PSW.7. It is carry flag (CY)

Stack Pointer (SP). Intel 8051 microcontroller contains an 8-bit stack pointer register. It is incremented before data is stored during PUSH and CALL operations. It is decremented when POP or RET (Return) operation takes place. Any area of on-chip RAM can be used as stack.

Program Counter (PC). The Intel 8051 microcontroller contains a 16-bit Program Counter (PC) register. It points to the address of the next instruction of the program, which is to be fetched and executed. It is automatically incremented after fetching an instruction. It keeps the track of memory addresses of the instructions in the program being executed. It is affected by JUMP and CALL instructions.

10.1.2 Pins of Intel 8051

Fig. 10.3 shows the pin diagram of Intel 8051 Microcontroller.

P1.0	1		40	V _{CC}
P1.1	2		39	P0.0/AD0
P1.2	3		38	P0.1/AD1
P1.3	4		37	P0.2/AD2
P1.4	5		36	P0.3/AD3
P1.5	6		35	P0.4/AD4
P1.6	7		34	P0.5/AD5
P1.7	8		33	P0.6/AD6
RST	9		32	P0.7/AD7
RXD/P3.0	10	Intel 8051	31	EA
TXD/P3.1	11		30	ALE
INT0/P3.2	12		29	PSEN
INT1/P3.3	13		28	P2.7/A15
T0/P3.4	14		27	P2.6/A14
T1/P3.5	15		26	P2.5/A13
WR/P3.6	16		25	P2.4/A12
RD/P3.7	17		24	P2.3/A11
XTAL2	18		23	P2.2/A10
XTAL1	19		22	P2.1/A9
V _{SS}	20		21	P2.0/A8

Fig. 10.3 Pin Diagram of Intel 8051 Microcontroller.

Pins 1 – 8 are for the Port 0, Pins 10 – 17 for Port 3, Pins 21 – 28 for Port 2 and Pins 32 – 39 for the Port 0. The alternate function of Pins 10 – 17 are given under the heading of I/O Lines (Next Subsection).

RST (Pin 9). It is the resetting pin for the device (8051).

XTAL2 (Pins 18). It is the output of inverting amplifier which is a part of the on-chip oscillator. When external clock is used, it is left unconnected.

- XTAL1 (Pin 19).** It is input to the inverting amplifier which is a part of the on-chip oscillator circuit. When external clock is used, it is connected to the external oscillator signal.
- V_{ss}(Pin 20).** It is the circuit ground. All the voltage are specified with respect to it.
- V_{cc}(Pin 40).** It is for power supply, +5V.
- PSEN(Pin 29).** It is program Store Enable. It is output control signal. It is a read strobe to external program memory.
- ALE (Pin 30).** It is Address Latch Enable output (control signal) for latching the low byte of the address during accesses to external memory.
- EA(Pin 31).** It is External Access. It controls the access of program memory. See Table 10.5.

10.1.3 I/O Lines

Most of the 8051 microcontrollers contain four 8-bit parallel ports : P0, P1, P2 and P3. Altogether there are 32 I/O lines. All ports in 8051 are bidirectional. The I/O lines of 8051 are not simply input/output lines, rather they are multifunctional lines. If an application does not need any external memory besides on-chip memory, then all four ports can be used as input/output ports. If external memory is used, then Port 0 and Port 2 act as a multiplexed address/data bus. When external memory is employed, two lines of Port 3 are used to generate the RD and WR signals. Two pins of Port 3 act as RXD and TXD for serial data transmission. Two pins of Port 3 can be used as external input for timers, one for Timer 0 and one for Timer 1. Two pins of Port 3 can be used as external interrupts.

Alternative function of port pins are given below:

P1.0	T2 (Timer/Counter 2 external input). P1.0 provides alternative function only on the 8052 microcontroller.
P1.1	T2EX (Timer/Counter 2 capture/reload trigger). P1.1 provides alternative function only on the 8052 microcontroller.
P3.0	RXD (Serial input port)
P3.1	TXD (Serial output port)
P3.2	<u>INT0</u> (External interrupt)
P3.3	<u>INT1</u> (External interrupt)
P3.4	T0 (Timer/Counter 0 external input)
P3.5	T1 (Timer/Counter 1 external input)
P3.6	<u>WR</u> External Data Memory Write Strobe)
P3.7	<u>RD</u> (External Data Memory Read Strobe)

Each port of Intel 8051 consists of a latch (SFR P0-P3), an output driver and an input buffer. The output drivers of Ports 0 and Port 2 and the input buffer of Port 0, are employed while accessing external memory. Port 0 sends 8 LSBs of external memory address, time-multiplexed with the byte being written or read. Port 2 sends 8 MSBs of the external memory address when address is of 16 bits. Otherwise the Port 2 pins continue to emit the P2 SFR content. In other words Port 2 acts as I/O port.

10.1.4 The 8051 Interrupts

The 8051 microcontrollers have 4-level priority interrupts. The number of interrupt sources differs from version to version. It varies from 5 to 15. The important interrupt sources are : one from the serial port, two from timers, two from external interrupts INT0 and INT1. Each of the interrupts can individually be enabled/disabled by setting/clearing a bit in the special function register IE (Interrupt Enable). The IE register also contains a global disable bit, which disables all the interrupts.

Each interrupt can also be programmed to one of the priority-level scheme by setting/clearing bits in the special function register IP (Interrupt Priority Register). A low-priority interrupt can be interrupted by a high-priority interrupt, but it can not be interrupted by another low-priority interrupt. A high-priority interrupt cannot be interrupted by a low-priority interrupt.

The 8051 microcontroller has five vectored interrupt sources namely, external interrupt 0 through the input pin INT0, external interrupt 1 through the input pin INT1, timer/counter 0 interrupt, timer/counter 1 interrupt and serial port interrupts. An interrupt for which microcontroller's hardware automatically transfers the program execution to a specific memory location is known as **vectored interrupt**. The specific memory location corresponding to each vector interrupt has a address as shown in Table 10.2. For each vectored interrupt there is an interrupt flag which is set when microcontroller's hardware detects the occurrence of an interrupt. Corresponding to above mentioned vectored interrupt sources, the 8051 has interrupt flags IE0, IE1, TF0, TF1, RI and TI respectively. Among these flags IE0, IE1, TF0 and TF1 are bits of the Timer/Counter Control Register TCON, as shown in Fig. 10.8. RI and TI are the bits of Serial Port Control Register SCON. RI is receive interrupt flag and TI transmit interrupt flag. These are connected through an OR gate and hence any one of RI or TI can send an interrupt signal to the microcontroller for the serial port. The other versions of 8051 series of microcontrollers have more number of interrupt sources for example 8052 contains 6 interrupt sources, 8XL51 FA/FB/FC has 7 interrupt sources and 8XC51 GB has 15. In 8052, Timer 2 interrupt is generated by the logical OR of TF2 and EXF2. The flags TF2 and EXF2 are not cleared by microcontroller's hardware when the service routine is vectored. The service routine determines whether TF2 or EXF2 has generated interrupt and the flag is cleared by software. Table 10.2 shows interrupts, flags, vector address and priority of interrupts within the same level.

Table 10.2 Details of Interrupts

Interrupt	Flag	Vector Address	Priority within level
External Interrupt 0, INT0	IE0	0003	Highest
Timer/Counter 0 Interrupt	TF0	000B	
External Interrupt1, INT1	IE1	0013	
Timer/Counter1 Interrupt	TF1	001B	
Serial Port, R1 or T1	R1 or T1	0023	
Timer/Counter 2 Interrupt	TF2 or EXF2	002B	Lowest

The external interrupts INT0 and INT1 can be programmed to act as a falling edge triggered or low level triggered interrupt by setting and clearing the bits IT0 and IT1 respectively in the register TCON. If an external interrupt is made edge triggered IE0 or IE1, interrupt flag is cleared by microcontroller's hardware when the service routine is vectored. If the external interrupt is level triggered, IE0 or IE1 is controlled by external requesting source of interrupt. The external interrupt source has to hold the interrupt request until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed. When the service routine is vectored, the interrupt flag is cleared by the external interrupt requesting source.

Enabling of 8051 Interrupts. The 8051 contains an interrupt enable register IE. It is a special function register (SFR). Each of interrupt sources can be individually enabled/disabled by setting/clearing a bit in the interrupt enable register IE. It also contains a global disable bit, EA which can disable all interrupts, if it is made equal to 0 i.e. EA = 0. It is a bit addressable register. To enable an interrupt, the bit EA and the bit corresponding to the desired interrupt is set. Fig. 10.4 shows the details of bits of register IE.

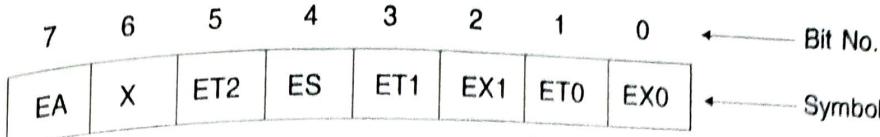


Fig. 10.4 Interrupt Enable Register IE (Bit Addressable)

- Bit No. 0, EX0. It is for External Interrupt 0 (INT0). When EX0 = 1, INT0 is enabled provided EA = 1. When EX0 = 0, INT0 is disabled.
- Bit No. 1, ET0. It is for Timer 0 Overflow interrupt. If ET0 = 1, the Timer 0 Overflow interrupt is enabled, provided EA = 1. If ET0 = 0, Timer 0 Overflow interrupt is disabled.
- Bit No. 2, EX1. It is for External Interrupt 1 (INT1). If EX1 = 1, INT1 is enabled, provided EA = 1. If EX1 = 0, INT1 is disabled.
- Bit No. 3, ET1. It is for Timer 1 Overflow interrupt. If ET1 = 1, Timer 1 Overflow interrupt is enabled, provided EA = 1. If ET1 = 0, Timer 1 Overflow interrupt is disabled.
- Bit No. 4, ES. It is for serial port interrupt. If ES = 1, the serial port interrupt is enabled, provided EA = 1. If ES = 0, the serial port interrupt is disabled.
- Bit No. 5, ET2. It is for Timer 2 Overflow or capture interrupt. If ET2 = 1, the Timer 2 Overflow or capture interrupt is enabled. If ET2 = 0, the Timer 2 Overflow or capture interrupt is disabled.
- Bit No. 6. Reserved.
- Bit No. 7, EA. It is a global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.

Interrupt Priority. By setting or clearing a bit in the special function register IP, the user can program each interrupt individually in either high-priority level or low-priority level. A low-priority interrupt can be interrupted by a high-priority interrupt, but it can not be interrupted by any other low-priority interrupt. A high-priority interrupt can not be interrupted by a low-priority interrupt. Table 10.2 shows priority level of various interrupts of Intel 8051 series of microcontrollers. If two interrupts of different priority level (i.e. one interrupt of high-priority level and another interrupt of low-priority level) occur simultaneously, the interrupt of the higher-priority level will be served first. If two interrupts of the same priority level occur simultaneously, an internal polling determines which interrupt is of higher-priority level on the basis of the priority level given in the Table 10.2.

Fig. 10.5 shows the details of the bits of Interrupt Priority Register, IP.

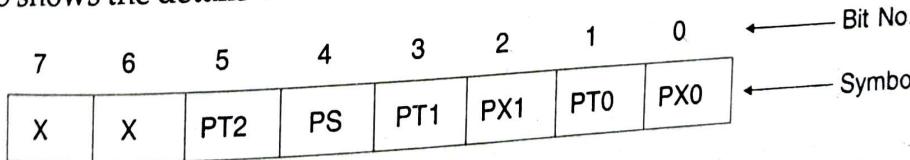


Fig. 10.5 Interrupt Priority Register

- Bit No. 0, PX0. It is for External Interrupt 0 (INT0) priority level. PX0 = 1, higher-priority. PX0 = 0, lower-priority.
- Bit No. 1, PT0. It is for Timer 0 Interrupt priority level. PT0 = 1, higher-priority. PT0 = 0, lower-priority.
- Bit No. 2, PX1. It is for External Interrupt 1 (INT1) priority level. PX1 = 1, higher-priority. PX1 = 0, lower-priority.
- Bit No. 3, PT1. It is for Timer 1 Interrupt priority level. PT1 = 1, higher-priority. PT1 = 0, lower-priority.
- Bit No. 4, PS. It is for Serial Port Interrupt priority level. PS = 1, higher-priority. PS = 0, lower-priority.