0.1 Project Title: Designing a Basic CPU on 2-bit Architecture

0.1.1 Introduction

The objective of this project is to design a basic 2-bit Central Processing Unit (CPU) using TTL (Transistor-Transistor Logic) gate integrated circuits. The CPU will consist of an Arithmetic Logic Unit (ALU) capable of performing four operations: ADD, AND, OR, and NOT. Additionally, the project will include memory registers, multiplexers (MUX), demultiplexers (DEMUX), and support for immediate operands, enabling immediate operations like ADI and ANI. Although this design could be expanded into a full-fledged CPU with an instruction decoder, ROM, and counter circuit, the scope of this project will focus on creating the fundamental building blocks of a basic CPU due to time constraints.

0.1.2 Components Required

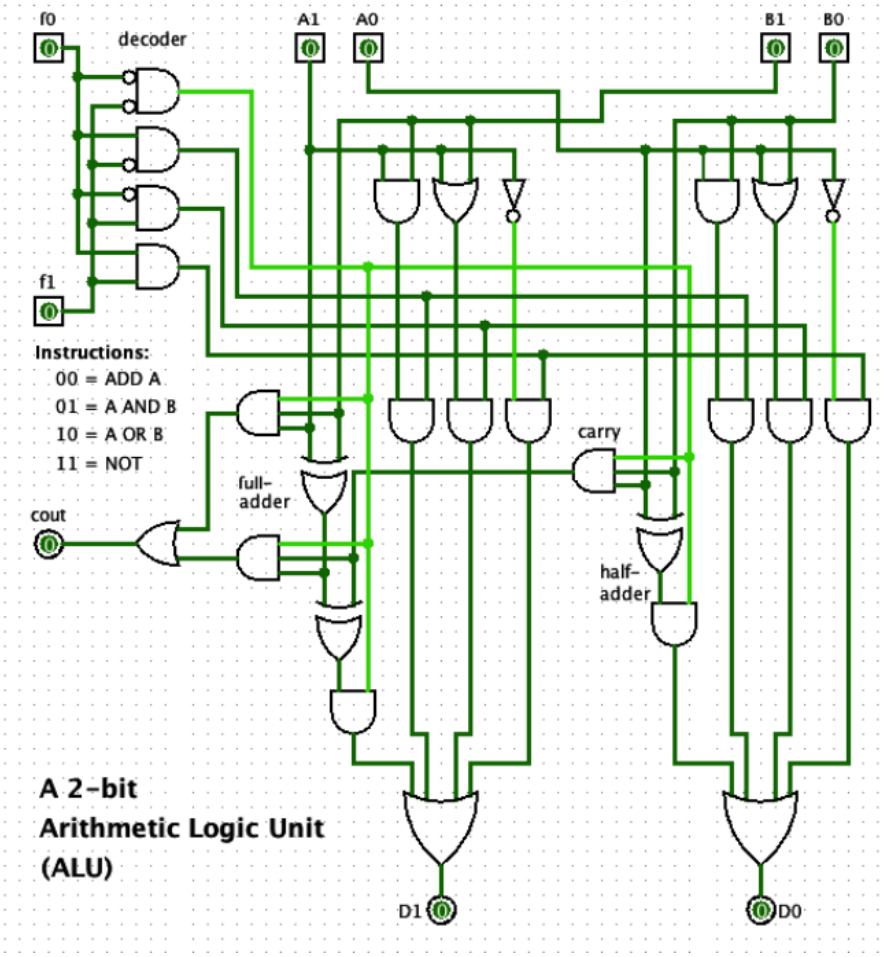
- 7404 NOT Gates (x4)
- 7408 AND Gates (x8)
- 7432 OR Gates (x4)
- 7486 XOR Gates (x2)
- 4x1 Multiplexers (MUX) (x8)
- 2x1 Demultiplexers (DEMUX) (x3)
- Push Switches (x10)
- Function Generator (optional)
- D Flip-Flops (x6)

0.1.3 Project Overview

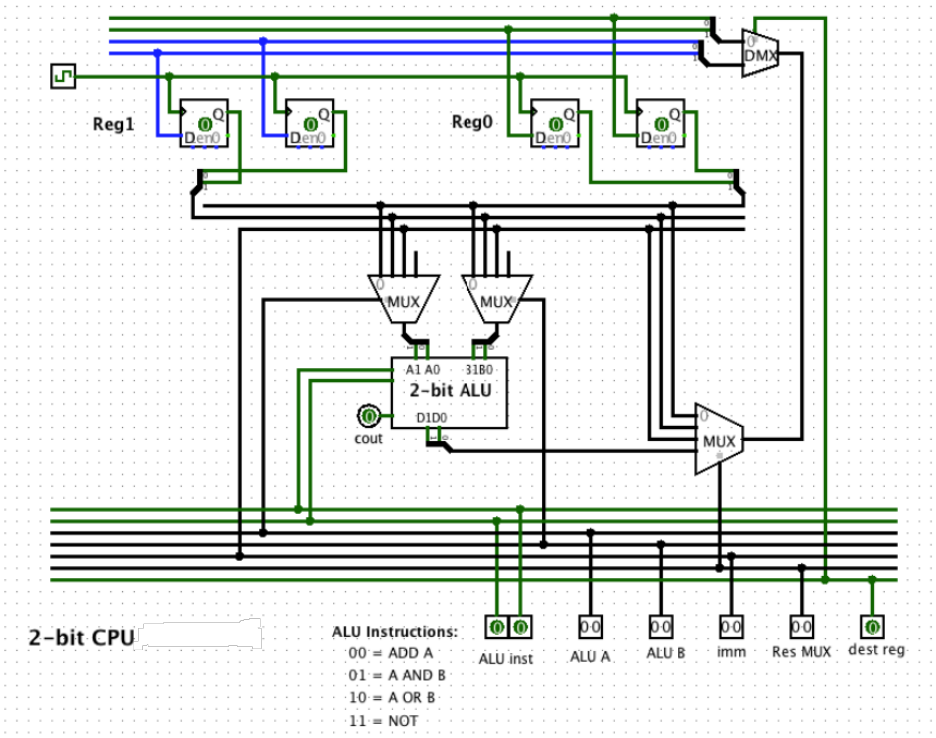
The project is divided into two main components: the ALU and the control bus. These components, along with the D flip-flops, MUX, and DEMUX, provide the essential functionality for the basic CPU.

The ALU is responsible for performing arithmetic and logic operations. In this project, it is designed to execute four functions: ADD, AND, OR, and NOT. It will take two 2-bit inputs and produce a 2-bit output, which can be used for various calculations and logical operations.

The control bus handles the control signals for various components, allowing the movement of data between registers, enabling immediate operations, and controlling the ALU's operation. While a full CPU typically includes an instruction decoder and a ROM for program execution, this project will implement a simplified control bus for the fundamental CPU operations.



The circuit diagram presented above depicts the ALU (Arithmetic Logic Unit). It is evident from the diagram that four distinct functions have been incorporated, and their execution is determined by a two-bit instruction command.



Schematic of a 2 bit CPU with Control bus, registers and an ALU.