REFNO062138 &

Roll No. .....

B.Sc. (Hons.) IV Semester Examination 2022-23

CS-104/CS-105 : Computer Organization and Architecture

Time : Three hours **Max. Marks :**

(Write your Roll No. at the top immediately on the receipt of this question paper)

Note: Answer five questions in all including Question No. 1, which is compulsory. Answers should be brief and to the point and may be supplemented with neat Sketches, wherever required. Terms and abbreviations have their standard meaning. Figures on the right-hand side margin indicate Max. Mark for each question.

Q.1 (a) A 4-way set-associative cache memory unit with a capacity of 32 KB is built using a block size of 16 words. The word length is 32 bits. The size of the physical address space is 8 GB. Find the number of bits required for the TAG field with explanation. 7

(b) Explain the stack and its operations with suitable example. Explain its relevance in computer organization. 7

Q.2 (a) Draw a block diagram of an 8-bit ALU with 4-bit status register and explain its working. 6

(b) Draw a diagram of a bus system for 4 registers of 4 bits each using multiplexer. 4

(c) Design a 4-bit adder-subtractor and explain its working. 4

Q.3 (a) An instruction is stored in a location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is 6

(i) Direct
(ii) Immediate
(iii) Relative
(iv) Register indirect

(b) What is the difference between isolated I/O and memory mapped I/O? 4

(c) Write short notes on Strobe control and Handshaking. 4

Q.4 (a) How to evaluate the arithmetic statement X = A+B+C*(D+E+F) 6

(i) Using a general register computer with three address instruction.
(ii) Using a general register computer with two address instruction.
(iii) Using a general register computer with one address instruction.

(b) Why I/O interface is required? Give any three reasons. 4

(c) What is memory hierarchy and why do we need it? Explain. 4

Q.5 (a) Explain the working of DMA (Direct Memory Access) with the block diagram. 8

(b) Differentiate between Horizontal and Vertical Microinstruction format for microprogrammed control unit. 6

P.T.O.

Q.6 (a) What are the basic differences among a branch instruction, a call sub-routine instruction and a program interrupt? 5

(b) What is an interrupt? Explain its major types. 5

(c) A computer has 32-bit instructions and 10-bit addresses. If there are 158 two-address instructions, how many one address instructions can be formulated? 4

Q.7 (a) We have to provide a memory capacity of 2048 bytes using 256 × 8 Ram chips. (i) How many chips are required? (ii) How many lines of the address bus must be used to access 2048 bytes of memory? (iii) How many of lines in (ii) will be common to all chips? (iv) How many lines must be decoded for chip select? Specify the size of decoders. 8

(b) Explain shift micro operations with suitable block diagrams and examples. Also mention how to detect overflow condition in the arithmetic shift micro operation. 6

———— o ————