NYU Tandon School of Engineering
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Project A Report

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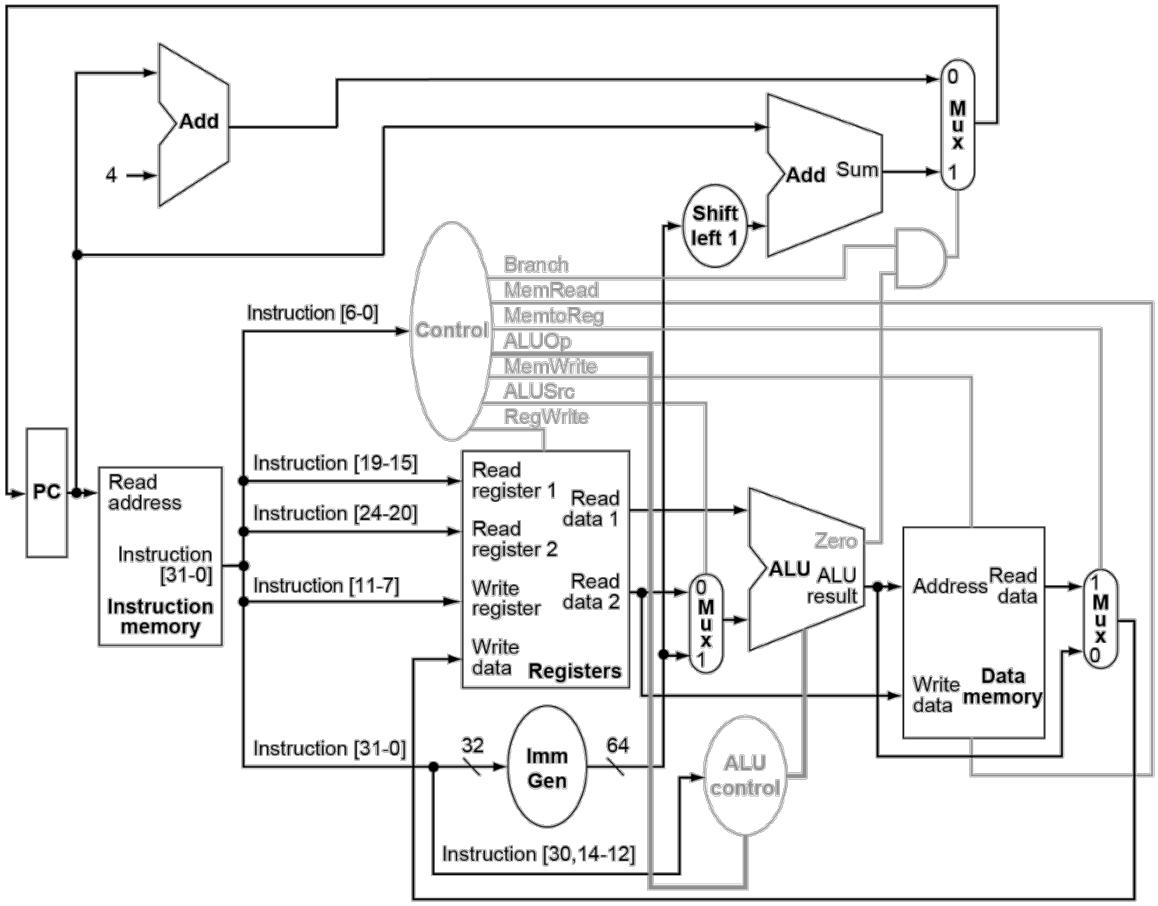
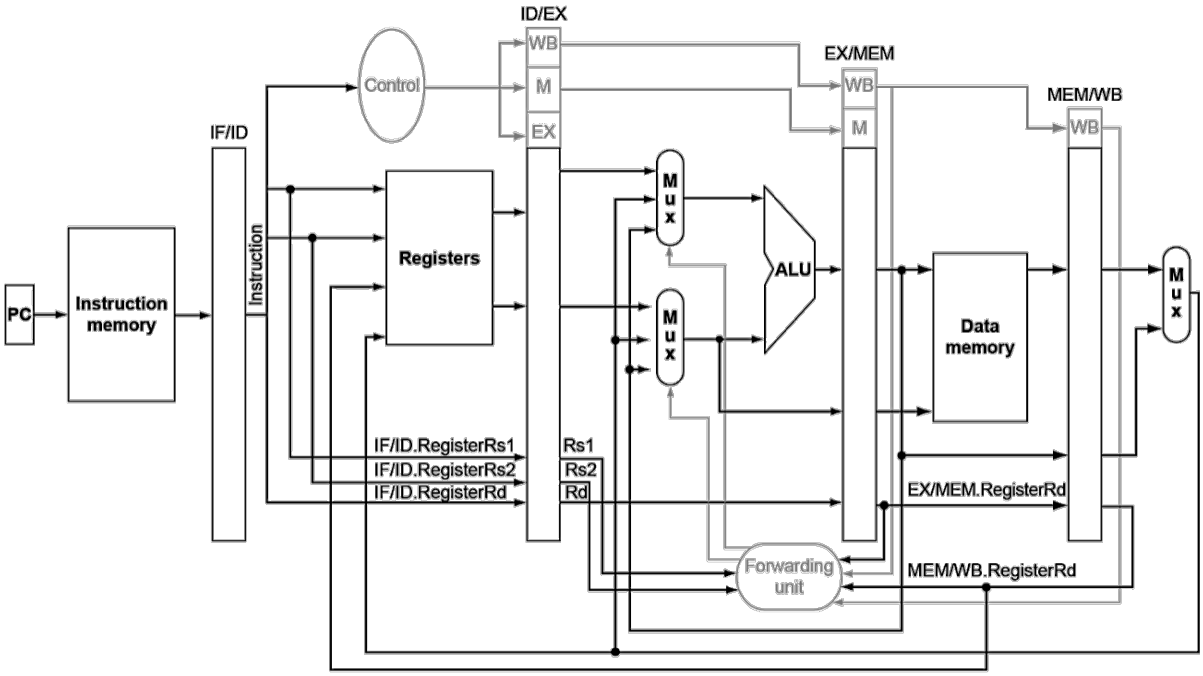
1. Schematic for a single stage processor



2. Schematic for a five stage processor



3. Performance parameter measures

Formulas Utilized –

CPI = No. of cycles/No. of instructions
Instructions per cycle = 1/Cycles per instruction

Final Grid –

# Test Case	No. of instructions	No of Cycles		Cycles per instruction (CPI)		Instructions per cycle (IPC)	
		Single Stage	Five Stage	Single Stage	Five Stage	Single Stage	Five Stage
Test Case 0	5	6	10	1.2	2	0.83	0.5
Test Case 1	39	40	46	1.02	1.18	0.98	0.85
Test Case 2	6	7	10	1.16	1.67	0.86	0.6
Test Case 3	7	8	11	1.14	1.56	0.88	0.64
Test Case 4	27	28	38	1.04	1.4	0.96	0.71

4. Compare the results from both the single stage and the five stage pipelined processor implementations and explain why one is better than the other

Five Stage Advantages –

- Throughput (rate of doing work) per instruction increases.
- No. of instructions executed simultaneously increases.
- Faster ALU can be designed when pipelining is utilized.
- Clock frequencies of pipelined CPU is higher than that of RAM. Hence, decrease in execution time is significant.
- Overall increase in performance of CPU.

Single Stage Advantages –

- Designing single stage processor is less tedious.
- Instruction latency is relatively lower.
- Prediction of throughput is also easier.
- The probability of hazard problems for branch instructions is way less.
- Total time including the execution time is lower than five stage.

5. Optimizations / Features added to improve performance (1 additional credit)

   # Not Added