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CS 2410: COMPUTER ARCHITECTURE

Project 2: Project Report

Introduction:

The purpose of this project is to evaluate **distributed directory cache coherence protocols in Chip Multi Processors (CMPs)**. Distributed directory cache coherence systems require the data being shared to be placed in a common directory that maintains the coherence between caches. The directory acts as a filter through which the processor must ask permission to load an entry from the primary memory to its cache. When an entry is changed, the directory either updates or invalidates the other caches with that entry. Thus it keeps track of the state of every block in every cache. In this project we have implemented a protocol with centralized memory and distributed directory.

Some of the common protocols implementing the above scheme are MSI, MESI and MOESI protocol. In this project we have implemented the **MSI protocol** with the following states for a block:

- **Modified/Exclusive/Dirty:** one processor (owner) has data; memory out-of-date
- **Shared/Clean:** cached in one or more processors and memory is up-to-date
- **Invalidate/Uncached:** no processor has it (not valid in any cache)

In this protocol, coherence has been enforced by exchanging messages between nodes. Three types of nodes may be involved:-

- **Local requestor node (L):** the node that reads or writes the cache block
- **Home node (H):** the node that stores the block (and its directory entry) in its memory, may be the same as L
- **Remote nodes (R):** other nodes that have a cached copy of the requested block.

When L encounters a **Read Hit**, it just reads the data. When L encounters a **Read Miss**, it sends a message to the home node, H, of the requested block – three cases may arise:
- The directory indicates that the block is “not cached / invalid”
- The directory indicates that the block is “shared/clean” and may supply the list of sharers
- The directory indicates that the block is “exclusive / modified”

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Assumptions:

Since the programmed processor does not utilize the same resources as the actual processor, several assumptions had to be made in addition to the ones specified in the project description.

- For the purpose of updating the states of the directories, message exchange between tiles is instantaneous
- For the purpose of computing the miss penalty, the delay of a message is implied by the specified NoC.
- For simplification, we are assuming that the states of a given block in all the caches are modified simultaneously and thus are always consistent.
- Data messages are calculated every time the tag of a block in L1 and L2 is updated as well as whenever a block is fetched from memory to L2.
- Control messages are calculated every time the status of a block is updated as well as whenever a control goes to the memory.
- Read and Write operations each take one cycle to complete. Rest is delay.
- Read and Write operations are not prioritized. These operations are executed as and when the instructions appear in the trace file.

Implementation:

The program for this processor was developed in Java. Below is a list of the different classes and data structures created:

Classes	Data Structures
• Start • ReadFile • GlobalVariables • Initialize • Evaluate • MemoryRead • Memory • Core • Directory • L1Block • L2Block	• L2Cache(3D Array) • L1Cache(2D Array) • memoryRead(HashTable) • core(Array) • delay(Array) • completionCycle(Array) • memFlag(Array) • count_L1_miss(Array) • delayL1(Array)

The simulation starts with reading the configuration file and input trace file which contains all the memory load and store operations. Each line in the trace file indicates the cycle and the core id that issues a read/write operation to the memory address in Hex format.

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The 32 bit memory addresses are divided into tag, index and offset as shown below:-

where
Tag is a unique identifier for a group of data. Because different regions of memory may be mapped into a block, the tag is used to differentiate between them.
Index is used to determine which cache set the address should reside in.
Offset is used to find the data within the cache block where the data was found.

For L1 Block:

Offset: (L1Cache size- L1 Set Associativity-Block size) bits
Index: L1 Set Associativity bits
Tag: Remaining bits in a 32 bit address

For L2 Block:

Offset: (L2Cache size- L2 Set Associativity-Block size) bits
Index: L2 Set Associativity bits
Tag: Remaining bits in a 32 bit address

The primary purpose of the simulator is to update the status of the cache blocks. The following conditions were handled while changing the status of the blocks:

- ***Invalidate Status in L1 cache:***

  Initially both the L1 and L2 caches are empty. When a block is not found in L1 cache (uncached/invalid status), control goes to L2 cache. In L2 cache, we can have the following three status for a block.

  - **Invalidate Status in L2 cache:**

    If the requested block is not found in the L2 cache, control goes to the memory. After the block is fetched from memory, the status of the block is updated to Shared (in case of Read operation) & Modified (in case of Write operation) in both L1 and L2 along with the tag update of the block in L1. In addition the directory of the block in L2 is updated with the cores that are currently sharing the block.

  - **Shared Status in L2 cache:**

First the tag of the block is compared to check if the requested block is a match to the block with Shared status in L2. In case of a match, the directory of the block in L2 is updated with the cores that are currently sharing the block. In addition, its tag and status is updated to Shared (in case of Read operation) & Modified (in case of Write operation) in L1 cache. In case of a mismatch, the states for all the cores present in the core list are invalidated in L1. Data is then fetched from the memory and the status of the new block is updated to Shared (in case of Read operation) & Modified (in case of Write operation) in both L1 and L2 cache. In addition, the tag of the block is updated in L1 and the directory of the block in L2 is updated with the cores that are currently sharing the block.

- **Modified Status in L2 cache:**

First the tag of the block is compared to check if the requested block is a match to the block with Shared status in L2. In case of a match, the requested block requests the block holding modified status to change to Shared (in case of Read operation) & Invalidate (in case of Write operation). Then the status of the requested block is updated to Shared (in case of Read operation) & Modified (in case of Write operation) in both L1 and L2. The directory of the block in L2 is updated with the cores that are currently sharing the block and its tag is updated in L1 cache. In case of a mismatch, the states for all the cores present in the core list are invalidated in L1. Data is then fetched from the memory and the status of the new block is updated to Shared (in case of Read operation) & Modified (in case of Write operation) in both L1 and L2 cache. In addition, the tag of the block is updated in L1 and the directory of the block in L2 is updated with the cores that are currently sharing the block (in case of Read operation) or with the core that is the owner of the block (in case of Write operation).

- ***Shared Status in L1 cache:***

- **Shared Status in L2 cache:**

First the tag of the block is compared to check if the requested block is a match to the block with Shared status in L2. In case of a match, the directory of the block in L2 is updated with the cores that are currently sharing the block. In addition, its tag and status is updated to Shared (in case of Read operation) & Invalidate (in case of Write operation) in L1 cache. In case of a mismatch, the states for all the cores present in the core list are invalidated in L1. Data is then fetched from the memory and the status of the new block is updated to Shared (in case of Read operation) & Modified (in case of Write operation) in both L1 and L2 cache. In addition, the tag of the block is updated in L1 and the directory of the block in L2 is updated with the cores that are currently sharing the block.

- **Modified Status in L2 cache:**

First the tag of the block is compared to check if the requested block is a match to the block with Modified status in L2. In case of a match, the status of the block is updated to Shared (in case of Read operation) & Modified (in case of Write operation) in both L1 and L2. The directory of the block in L2 is updated with the cores that are currently sharing the block and its tag is updated in L1 cache. In case of a mismatch, the states for all the cores present in the core list are invalidated in L1. Data is then fetched from the memory and the status of the new block is updated to Shared (in case of Read operation) & Modified (in case of Write operation) in both L1 and L2 cache. In addition, the tag of the block is updated in L1 and the directory of the block in L2 is updated with the cores that are currently sharing the block (in case of Read operation) or with the core that is the owner of the block (in case of Write operation).

▪ *Modified Status in L1 cache:*

- **Shared Status in L2 cache:**

First the tag of the block is compared to check if the requested block is a match to the block with Shared status in L2. In case of a match, the directory of the block in L2 is updated with the cores that are currently sharing the block. In addition, its tag and status is updated to Shared (in case of Read operation) & Modified (in case of Write operation) in L1 cache and L2 Cache. In case of a mismatch, the states for all the cores present in the core list are invalidated in L1. Data is then fetched from the memory and the status of the new block is updated to Shared (in case of Read operation) & Modified (in case of Write operation) both L1 and L2 cache. In addition, the tag of the block is updated in L1 and the directory of the block in L2 is updated with the cores that are currently sharing the block.

- **Modified Status in L2 cache:**

First the tag of the block is compared to check if the requested block is a match to the block with Shared status in L2. In case of a match, the status of the block is updated to Shared in both L1 and L2. The directory of the block in L2 is updated with the cores that are currently sharing the block and its tag is updated in L1 cache. In case of a mismatch, the states for all the cores present in the core list are invalidated in L1. Data is then fetched from the memory and the status of the new block is updated to Shared (in case of Read operation) & Modified (in case of Write operation) in both L1 and L2 cache. In addition, the tag of the block is updated in L1 and the directory of the block in L2 is updated with the cores that are

currently sharing the block (in case of Read operation) or with the core that is the owner of the block (in case of Write operation).

The iteration of the program stops when there are no more instructions to execute.

Analysis and Results:

Trace 1 file Output:

##
p=4

n1=14

n2=19

b=6

a1=2

a2=2

C=3

d=3

d1=100

##

Normal Conditions

##

Data Messages:794298

Control Messages:1459163

Core Id: 0

Completion Cycle :6405

L1 Miss Rate : 75.5813953488372

Average L1 miss penalty : 8.907692307692308

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Core Id: 1

Completion Cycle :1597824

L1 Miss Rate : 37.69806292917905

Average L1 miss penalty : 5.8998423141754115

Core Id: 2

Completion Cycle :3030837

L1 Miss Rate : 72.48129548016809

Average L1 miss penalty : 5.730118778280543

Core Id: 3

Completion Cycle :2910364

L1 Miss Rate : 71.76248667268105

Average L1 miss penalty : 3.6502285714285714

Core Id: 4

Completion Cycle :3211314

L1 Miss Rate : 70.20421553350283

Average L1 miss penalty : 6.7759345794392525

Core Id: 5

Completion Cycle :3264398

L1 Miss Rate : 69.00065611416386

Average L1 miss penalty : 10.186075535613467

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Core Id: 6

Completion Cycle :3239252

L1 Miss Rate : 66.65163472378805

Average L1 miss penalty : 12.782384057079591

Core Id: 7

Completion Cycle :3271229

L1 Miss Rate : 66.86475022573127

Average L1 miss penalty : 16.22504161040103

Core Id: 8

Completion Cycle :2823756

L1 Miss Rate : 52.663728605104026

Average L1 miss penalty : 26.063988790284913

Core Id: 9

Completion Cycle :3385439

L1 Miss Rate : 64.6600508488477

Average L1 miss penalty : 21.348078386605785

Core Id: 10

Completion Cycle :3140179

L1 Miss Rate : 55.88247355039777

Average L1 miss penalty : 31.985800770500827

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Core Id: 11

Completion Cycle :3422857

L1 Miss Rate : 63.386093359854414

Average L1 miss penalty : 27.896745117676513

Core Id: 12

Completion Cycle :3069288

L1 Miss Rate : 51.841220372344786

Average L1 miss penalty : 37.469625059326056

Core Id: 13

Completion Cycle :3317611

L1 Miss Rate : 54.70533975607256

Average L1 miss penalty : 40.99561600719424

Core Id: 14

Completion Cycle :3370923

L1 Miss Rate : 54.20518602029312

Average L1 miss penalty : 44.42607018605355

Core Id: 15

Completion Cycle :3374637

L1 Miss Rate : 52.75597007276827

Average L1 miss penalty : 47.37603450285581

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L2 Miss Rate: 80.66274089692239

##

Doubling the network delay

##

p=4

n1=14

n2=19

b=6

a1=2

a2=2

C=6

d=3

d1=100

##

##

Data Messages:759653

Control Messages:1396472

Core Id: 0

Completion Cycle :6789

L1 Miss Rate : 75.5813953488372

Average L1 miss penalty : 14.815384615384616

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Core Id: 1

Completion Cycle :1699041

L1 Miss Rate : 37.82105155273137

Average L1 miss penalty : 8.79740935450653

Core Id: 2

Completion Cycle :2964518

L1 Miss Rate : 69.2343958183868

Average L1 miss penalty : 8.434924206537186

Core Id: 3

Completion Cycle :2756513

L1 Miss Rate : 68.05339129008448

Average L1 miss penalty : 4.371877918712904

Core Id: 4

Completion Cycle :3204584

L1 Miss Rate : 67.81760026244567

Average L1 miss penalty : 10.605212238481075

Core Id: 5

Completion Cycle :3341470

L1 Miss Rate : 66.26753055031575

Average L1 miss penalty : 17.467945544554457

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Core Id: 6

Completion Cycle :3426041

L1 Miss Rate : 64.6407707287076

Average L1 miss penalty : 22.61363564293642

Core Id: 7

Completion Cycle :3499759

L1 Miss Rate : 63.452533439724505

Average L1 miss penalty : 29.577867496194322

Core Id: 8

Completion Cycle :3242350

L1 Miss Rate : 50.068668648150044

Average L1 miss penalty : 49.030950626381724

Core Id: 9

Completion Cycle :3717077

L1 Miss Rate : 60.71311408185024

Average L1 miss penalty : 39.741008409037185

Core Id: 10

Completion Cycle :3492449

L1 Miss Rate : 49.083490527351756

Average L1 miss penalty : 60.68937716696604

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Anuradha Kulkarni
Ankita Mohapatra

Core Id: 11

Completion Cycle :3818791

L1 Miss Rate : 57.99864573193957

Average L1 miss penalty : 52.956364697727025

Core Id: 12

Completion Cycle :4030316

L1 Miss Rate : 53.19035512179119

Average L1 miss penalty : 72.01873409914424

Core Id: 13

Completion Cycle :4256475

L1 Miss Rate : 53.82187147688839

Average L1 miss penalty : 78.96008683398713

Core Id: 14

Completion Cycle :4401998

L1 Miss Rate : 53.41805882955826

Average L1 miss penalty : 85.83568687643898

Core Id: 15

Completion Cycle :4384694

L1 Miss Rate : 51.33545147073896

Average L1 miss penalty : 91.71753713464302

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L2 Miss Rate: 80.3033323839362

##

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Comments

1. Average L1 miss penalty increases with the increase in network delay as expected and it is significant.

2. There is fluctuation in the L1 and L2 miss rates but the difference is not significant, the decrease in miss rates might be due to the delay in the status updates especially when the blocks are invalidated.

3. As expected the number of cycles taken by each core increases with the increase in network delay if that core is requesting data from remote tile.

4. Data and control message is less compared to the normal network delay, this might be because of delay in the status updates especially when the blocks are invalidated.

##
p=4

n1=14

n2=19

b=6

a1=2

a2=4

C=3

d=3

d1=100

##

Doubling the L2 associativity

##

Data Messages:794298

Control Messages:1459163

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Core Id: 0

Completion Cycle :6405

L1 Miss Rate : 75.5813953488372

Average L1 miss penalty : 8.907692307692308

Core Id: 1

Completion Cycle :1597824

L1 Miss Rate : 37.69806292917905

Average L1 miss penalty : 5.8998423141754115

Core Id: 2

Completion Cycle :3030837

L1 Miss Rate : 72.48129548016809

Average L1 miss penalty : 5.730118778280543

Core Id: 3

Completion Cycle :2910364

L1 Miss Rate : 71.76248667268105

Average L1 miss penalty : 3.6502285714285714

Core Id: 4

Completion Cycle :3211314

L1 Miss Rate : 70.20421553350283

Average L1 miss penalty : 6.7759345794392525

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Core Id: 5

Completion Cycle :3264398

L1 Miss Rate : 69.00065611416386

Average L1 miss penalty : 10.186075535613467

Core Id: 6

Completion Cycle :3239252

L1 Miss Rate : 66.65163472378805

Average L1 miss penalty : 12.782384057079591

Core Id: 7

Completion Cycle :3271229

L1 Miss Rate : 66.86475022573127

Average L1 miss penalty : 16.22504161040103

Core Id: 8

Completion Cycle :2823756

L1 Miss Rate : 52.663728605104026

Average L1 miss penalty : 26.063988790284913

Core Id: 9

Completion Cycle :3385439

L1 Miss Rate : 64.6600508488477

Average L1 miss penalty : 21.348078386605785

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Core Id: 10

Completion Cycle :3140179

L1 Miss Rate : 55.88247355039777

Average L1 miss penalty : 31.985800770500827

Core Id: 11

Completion Cycle :3422857

L1 Miss Rate : 63.386093359854414

Average L1 miss penalty : 27.896745117676513

Core Id: 12

Completion Cycle :3069288

L1 Miss Rate : 51.841220372344786

Average L1 miss penalty : 37.469625059326056

Core Id: 13

Completion Cycle :3317611

L1 Miss Rate : 54.70533975607256

Average L1 miss penalty : 40.99561600719424

Core Id: 14

Completion Cycle :3370923

L1 Miss Rate : 54.20518602029312

Average L1 miss penalty : 44.42607018605355

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Core Id: 15

Completion Cycle :3374637

L1 Miss Rate : 52.75597007276827

Average L1 miss penalty : 47.37603450285581

L2 Miss Rate: 80.66274089692239

##

****

Comments

1. No changes in the number cycles taken when compared to the normal L2 associativity.

2. No changes in the Data and Control messages exchanged between the tiles.

3. No changes in the L1 miss penalty.

4. No changes in the L1 miss rate and L2 miss rates.

##

Doubling the L2 cache size

##

p=4

n1=14

n2=20

b=6

a1=2

a2=2

C=3

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d=3

d1=100

Data Messages:723111

Control Messages:1345359

Core Id: 0

Completion Cycle :6405

L1 Miss Rate : 75.5813953488372

Average L1 miss penalty : 8.907692307692308

Core Id: 1

Completion Cycle :1946496

L1 Miss Rate : 45.20651839704827

Average L1 miss penalty : 5.916205676974698

Core Id: 2

Completion Cycle :2569876

L1 Miss Rate : 58.45444296402583

Average L1 miss penalty : 5.665252305642248

Core Id: 3

Completion Cycle :2174241

L1 Miss Rate : 59.60592143032888

Average L1 miss penalty : 3.7816036600048157

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Core Id: 4

Completion Cycle :2682584

L1 Miss Rate : 60.04879849093742

Average L1 miss penalty : 6.906750435346741

Core Id: 5

Completion Cycle :2631887

L1 Miss Rate : 57.0450258344952

Average L1 miss penalty : 10.429911580763426

Core Id: 6

Completion Cycle :2772234

L1 Miss Rate : 58.29455775340781

Average L1 miss penalty : 12.89475719962024

Core Id: 7

Completion Cycle :2775054

L1 Miss Rate : 57.535224576360164

Average L1 miss penalty : 16.422591240875914

Core Id: 8

Completion Cycle :3016087

L1 Miss Rate : 56.394383519524446

Average L1 miss penalty : 26.125581564408257

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Core Id: 9

Completion Cycle :2930810

L1 Miss Rate : 56.71081768227672

Average L1 miss penalty : 21.396435156730178

Core Id: 10

Completion Cycle :3120382

L1 Miss Rate : 55.04387763470844

Average L1 miss penalty : 31.970349400283098

Core Id: 11

Completion Cycle :2907849

L1 Miss Rate : 54.80341952685259

Average L1 miss penalty : 28.033476195992122

Core Id: 12

Completion Cycle :3007369

L1 Miss Rate : 50.02870499466907

Average L1 miss penalty : 37.41651639344262

Core Id: 13

Completion Cycle :3251967

L1 Miss Rate : 53.24792456697755

Average L1 miss penalty : 40.968818570273704

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Ankita Mohapatra

Core Id: 14

Completion Cycle :3376832

L1 Miss Rate : 54.026852516142256

Average L1 miss penalty : 44.42508631483098

Core Id: 15

Completion Cycle :3358911

L1 Miss Rate : 52.430050220354616

Average L1 miss penalty : 47.37239033544452

L2 Miss Rate: 79.48411821794417

##

__Doubling the L2 cache size__

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__Comments__

1. L2 miss rate decreases(hit rate improves) by more than 2%, as expected as the size of L2 cache increases less blocks are replaced.

2. In many of the L1 cores, miss rate decreases significantly(hit rate improves) as the L2 cache associated with each core increases. That means more data is present in the L2 and more data is read into L1 cache(as L1 is subset of L2 cache)

3. There is no significant changes in L1 miss penalty, but there is slight improvement as the network hoping decreases as the L2 chache size is increased.

4. Both data and control messages decreases as L2 cache size is doubled and more data is held in L2 cache hence less message exchanged between remote and memory block.

##

Trace 2 File Output:

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##

Normal Conditions

##

p=4

n1=14

n2=19

b=6

a1=2

a2=2

C=3

d=3

d1=100

##

Data Messages:53561

Control Messages:96701

Core Id: 0

Completion Cycle :0

Core Id: 1

Completion Cycle :35977

L1 Miss Rate : 52.34986945169713

Average L1 miss penalty : 6.635910224438903

Core Id: 2

Completion Cycle :239950

L1 Miss Rate : 59.741417744092736

Average L1 miss penalty : 6.0

Core Id: 3

Completion Cycle :228223

L1 Miss Rate : 55.75205104831358

Average L1 miss penalty : 4.789404839764552

Core Id: 4

Completion Cycle :273174

L1 Miss Rate : 48.489140698772424

Average L1 miss penalty : 7.258033106134372

Core Id: 5

Completion Cycle :144197

L1 Miss Rate : 57.588279489105936

Average L1 miss penalty : 9.575342465753424

Core Id: 6

Completion Cycle :310080

L1 Miss Rate : 51.55856423173803

Average L1 miss penalty : 13.090076335877862

Core Id: 7

Completion Cycle :0

Core Id: 8

Completion Cycle :286853

L1 Miss Rate : 41.26909148165643

Average L1 miss penalty : 26.190766882869134

Core Id: 9

Completion Cycle :321092

L1 Miss Rate : 48.66183879093199

Average L1 miss penalty : 21.57360077644775

Core Id: 10

Completion Cycle :246420

L1 Miss Rate : 47.78203107408241

Average L1 miss penalty : 32.30301602262017

Core Id: 11

Completion Cycle :0

Core Id: 12

Completion Cycle :335081

L1 Miss Rate : 41.04219143576826

Average L1 miss penalty : 39.0

Core Id: 13

Completion Cycle :129398

L1 Miss Rate : 60.07088009450679

Average L1 miss penalty : 40.339233038348084

Core Id: 14

Completion Cycle :302634

L1 Miss Rate : 56.963855421686745

Average L1 miss penalty : 44.743654822335024

Core Id: 15

Completion Cycle :291190

L1 Miss Rate : 57.45727602278612

Average L1 miss penalty : 46.8400180261379

L2 Miss Rate: 78.13695167780772

##

__Doubling the L2 cache size__

Data Messages:53561

Control Messages:96698

Core Id: 0

Completion Cycle :0

Core Id: 1

Completion Cycle :35977

L1 Miss Rate : 52.34986945169713

Average L1 miss penalty : 6.635910224438903

Core Id: 2

Completion Cycle :239950

L1 Miss Rate : 59.741417744092736

Average L1 miss penalty : 6.0

Core Id: 3

Completion Cycle :228223

L1 Miss Rate : 55.75205104831358

Average L1 miss penalty : 4.789404839764552

Core Id: 4

Completion Cycle :273174

L1 Miss Rate : 48.489140698772424

Average L1 miss penalty : 7.258033106134372

Core Id: 5

Completion Cycle :144197

L1 Miss Rate : 57.588279489105936

Average L1 miss penalty : 9.575342465753424

Core Id: 6

Completion Cycle :310080

L1 Miss Rate : 51.55856423173803

Average L1 miss penalty : 13.090076335877862

Core Id: 7

Completion Cycle :0

Core Id: 8

Completion Cycle :286853

L1 Miss Rate : 41.26909148165643

Average L1 miss penalty : 26.190766882869134

Core Id: 9

Completion Cycle :321092

L1 Miss Rate : 48.66183879093199

Average L1 miss penalty : 21.57360077644775

Core Id: 10

Completion Cycle :246420

L1 Miss Rate : 47.78203107408241

Average L1 miss penalty : 32.30301602262017

Core Id: 11

Completion Cycle :0

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Core Id: 12

Completion Cycle :335081

L1 Miss Rate : 41.04219143576826

Average L1 miss penalty : 39.0

Core Id: 13

Completion Cycle :129398

L1 Miss Rate : 60.07088009450679

Average L1 miss penalty : 40.339233038348084

Core Id: 14

Completion Cycle :302634

L1 Miss Rate : 56.963855421686745

Average L1 miss penalty : 44.743654822335024

Core Id: 15

Completion Cycle :291190

L1 Miss Rate : 57.45727602278612

Average L1 miss penalty : 46.8400180261379

L2 Miss Rate: 78.13695167780772

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*** **Comments***

1. No changes in the number cycles taken when compared to the normal L2 associativity.

2. No changes in the Data and Control messages exchanged between the tiles.

3. No changes in the L1 miss penalty.

4. No changes in the L1 miss rate and L2 miss rates.

##

Doubling the L2 associativity

Data Messages:53561
Control Messages:96701

Core Id: 0
Completion Cycle :0

Core Id: 1
Completion Cycle :35977
L1 Miss Rate : 52.34986945169713
Average L1 miss penalty : 6.635910224438903

Core Id: 2
Completion Cycle :239950
L1 Miss Rate : 59.741417744092736
Average L1 miss penalty : 6.0

Core Id: 3
Completion Cycle :228223
L1 Miss Rate : 55.75205104831358
Average L1 miss penalty : 4.789404839764552

Core Id: 4
Completion Cycle :273174
L1 Miss Rate : 48.489140698772424
Average L1 miss penalty : 7.258033106134372

Core Id: 5
Completion Cycle :144197
L1 Miss Rate : 57.588279489105936
Average L1 miss penalty : 9.575342465753424

Core Id: 6

Completion Cycle :310080
L1 Miss Rate : 51.55856423173803
Average L1 miss penalty : 13.090076335877862

Core Id: 7
Completion Cycle :0

Core Id: 8
Completion Cycle :286853
L1 Miss Rate : 41.26909148165643
Average L1 miss penalty : 26.190766882869134

Core Id: 9
Completion Cycle :321092
L1 Miss Rate : 48.66183879093199
Average L1 miss penalty : 21.57360077644775

Core Id: 10
Completion Cycle :246420
L1 Miss Rate : 47.78203107408241
Average L1 miss penalty : 32.30301602262017

Core Id: 11
Completion Cycle :0

Core Id: 12
Completion Cycle :335081
L1 Miss Rate : 41.04219143576826
Average L1 miss penalty : 39.0

Core Id: 13
Completion Cycle :129398
L1 Miss Rate : 60.07088009450679
Average L1 miss penalty : 40.339233038348084

Core Id: 14
Completion Cycle :302634
L1 Miss Rate : 56.963855421686745
Average L1 miss penalty : 44.743654822335024

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Core Id: 15
Completion Cycle :291190
L1 Miss Rate : 57.45727602278612
Average L1 miss penalty : 46.8400180261379

L2 Miss Rate: 78.13695167780772

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*** **Comments***
1. No changes in the number cycles taken when compared to the normal L2 associativity.
2. No changes in the Data and Control messages exchanged between the tiles.
3. No changes in the L1 miss penalty.
4. No changes in the L1 miss rate and L2 miss rates.
##
Doubling the network delay

Data Messages:53264
Control Messages:96601

Core Id: 0
Completion Cycle :0

Core Id: 1
Completion Cycle :32177
L1 Miss Rate : 44.25587467362924
Average L1 miss penalty : 10.504424778761061

Core Id: 2
Completion Cycle :236663
L1 Miss Rate : 57.445385644226484
Average L1 miss penalty : 9.0

Core Id: 3
Completion Cycle :187580
L1 Miss Rate : 45.26891522333637
Average L1 miss penalty : 7.371325010068466

Core Id: 4
Completion Cycle :299709

L1 Miss Rate : 50.94428706326723
Average L1 miss penalty : 11.398517145505098

Core Id: 5
Completion Cycle :171453
L1 Miss Rate : 64.27498121712998
Average L1 miss penalty : 16.03448275862069

Core Id: 6
Completion Cycle :329119
L1 Miss Rate : 50.20465994962217
Average L1 miss penalty : 23.238946378174976

Core Id: 7
Completion Cycle :0

Core Id: 8
Completion Cycle :395317
L1 Miss Rate : 47.677531097464964
Average L1 miss penalty : 49.60700132100396

Core Id: 9
Completion Cycle :359668
L1 Miss Rate : 46.06423173803527
Average L1 miss penalty : 40.21189336978811

Core Id: 10
Completion Cycle :367182
L1 Miss Rate : 57.35194775951362
Average L1 miss penalty : 61.840989399293285

Core Id: 11
Completion Cycle :0

Core Id: 12
Completion Cycle :430122
L1 Miss Rate : 42.222921914357684
Average L1 miss penalty : 74.98657718120805

Core Id: 13

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Completion Cycle :154959
L1 Miss Rate : 55.7590076786769
Average L1 miss penalty : 77.42161016949153

Core Id: 14
Completion Cycle :403699
L1 Miss Rate : 57.18072289156626
Average L1 miss penalty : 86.48925410872313

Core Id: 15
Completion Cycle :349642
L1 Miss Rate : 51.320559295701706
Average L1 miss penalty : 90.40867810292633

L2 Miss Rate: 77.44020254513958

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__Comments__

1. Average L1 miss penalty increases with the increase in network delay as expected and it is significant.
2. In some cores there is significant decrease in L1 miss rate, this might be due to delay in the status updates especially when the blocks are invalidated.
3. As expected the number of cycles taken by each core increases with the increase in network delay if that core is requesting data from remote tile but there are few cores where the completion cycle decreases, this might be due to the fact that other cores might have loaded the data in L2 already and because of delay in the status updates especially when the blocks are invalidated
4. Data and control message is less compared to the normal network delay, this might be because of delay in the status updates especially when the blocks are invalidated.
5. Slight decrease in L2 miss rate might be due to the delay in invalidated status updates.

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