DESIGN OF FAULT-TOLERANT DECODER CIRCUIT FOR RESILIENT FPGA SYSTEMS

SUMMER INTERNSHIP IN ELECTRONICS AND COMMUNICATION ENGINEERING

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ABSTRACT:

In **Digital Electronics**, **Decoders** are pivotal components that translate encoded signals into a comprehensive set of outputs, facilitating the control and operation of various digital systems. A decoder, typically used within digital circuits, is a combinational logic circuit that converts binary information from `n` input lines to a maximum of `2^n` unique output lines. This functionality is integral to a wide array of applications, including memory address decoding, data multiplexing, and communication systems.

Field-Programmable Gate Arrays (FPGAs) are highly versatile semiconductor devices that offer reprogrammable logic for a variety of digital designs. They are composed of an array of **Configurable Logic Blocks (CLBs**), which contain both combinational and sequential logic elements. Decoders are fundamental elements within these CLBs, playing a crucial role in routing and managing signals across the FPGA fabric. The ability to reconfigure FPGAs allows for the implementation of complex, customized digital circuits, making them indispensable in modern digital design.

Given the increasing complexity and critical nature of digital systems, ensuring the reliability and robustness of decoders is necessary. **Fault tolerance in decoders** is essential to maintain the integrity and performance of digital circuits, especially in safety-critical applications. A fault-tolerant decoder circuit can detect and correct errors, thereby enhancing the reliability of the entire digital system.

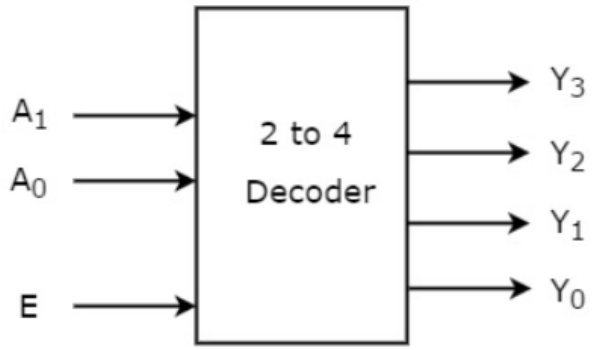
My work focuses on the **Design and Implementation of a Fault-Tolerant Decoder circuit** for use in fault-tolerant FPGA architectures. By integrating fault detection and correction mechanisms within the decoder, this design aims to ensure continuous and accurate operation even in the presence of faults. This project addresses the challenges of implementing robust fault-tolerant solutions in FPGA technology, contributing to the development of more reliable digital systems.

CONTENTS:

INTRODUCTION:

Digital electronics is the foundation of modern computing and communication systems. Within this field, **Decoders** play a crucial role in translating binary information into a format that can be used by various digital components. **Field Programmable Gate Arrays (FPGAs**) are **versatile** and powerful devices used in a wide range of applications, from **consumer electronics** to **aerospace systems**. Central to the functionality of an FPGA are **Configurable Logic Blocks (CLBs),** which contain the lookup table, multiplexers, decoders and other essential components needed to perform logic operations.

Decoders within CLBs are responsible for interpreting configuration data and routing signals appropriately. Ensuring these decoders function correctly is vital for the **reliability** and **efficiency** of the entire FPGA. Faults in decoders can lead to incorrect operations, signal routing errors, and system failures. This makes the design of fault-tolerant decoders a critical area of focus.



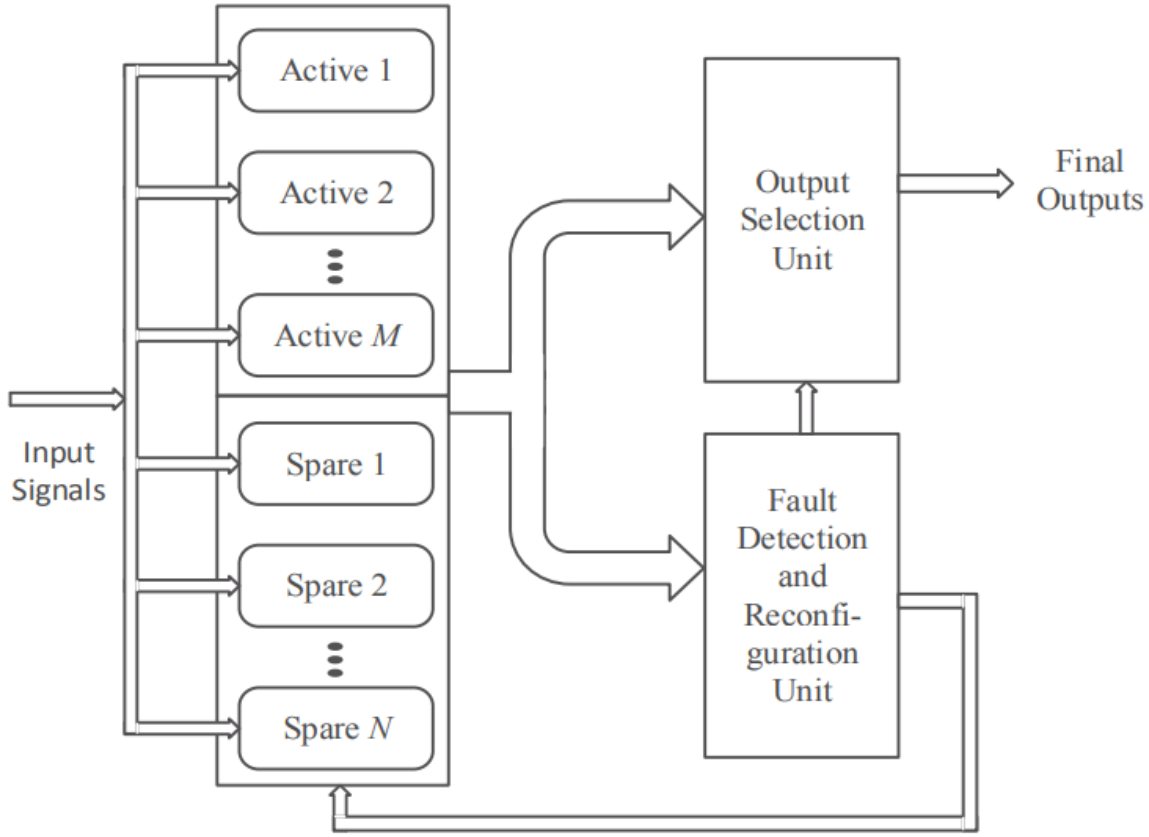
Inputs			Outputs			
E	A0	A1	Q0	Q1	Q2	Q3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Inputs and Outputs for Active Low Decoder

The importance of fault-tolerant design in decoders lies in its ability to enhance the reliability and robustness of FPGAs. By incorporating fault-tolerant mechanisms, such as **redundancy** and error detection, it is possible to minimize the impact of faults and ensure continuous, correct operation even in the presence of hardware defects. This is particularly important in critical applications where system failure can lead to significant damages.

My work primarily focuses on the design of a **Fault-tolerant Decoder** circuit by using **Dynamic Redundancy** reconfiguration mechanism designed for use in FPGAs. By improving the resilience of the decoders within the CLBs, this project aims to contribute to the development of more **reliable and robust FPGA systems**. This approach ensures that FPGA-based applications can maintain functionality even in the presence of faults, significantly enhancing their dependability. Ultimately, this work seeks to pave the way for more advanced and fault-tolerant digital systems in various critical applications.

Dynamic recovery involves automated self-repair where the system consists of some identical spare modules along with the active modules and a Fault Detection and Reconfiguration unit, that is assumed to be capable of detecting any erroneous output produced by the active module, disconnecting the faulty active module, and connecting instead a fault-free spare. The approach is generally more hardware-efficient than voted systems. But this technique is a little bit time consuming and not efficient to protect against transient errors.



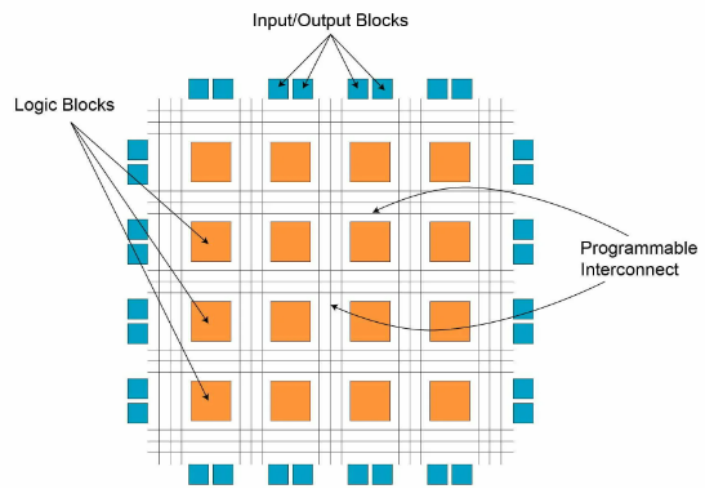
Block Diagram for dynamic reconfiguration

In this approach, redundant parts are dynamically activated only if some currently active modules are identified as faulty. Therefore, power is not consumed constantly for the passive redundancies, leading to much better resource utilization compared to static methods, like voted approaches such as TMR, DMR, etc. Thus, dynamic redundancy mechanism not only enhances the fault tolerance of FPGA systems but also contributes to their **energy efficiency** and longevity, making it a valuable advancement in resilient FPGA design

BACKGROUND:

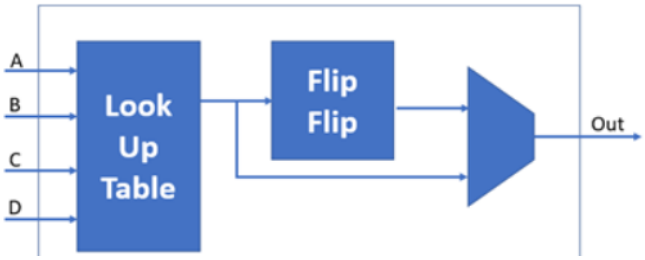
I conducted extensive research on existing work or techniques to implement this project. My study encompassed a comprehensive review of IEEE papers that elucidate various fault-tolerant techniques and their practical applications. Key topics explored include fault-tolerant ripple carry adders, conditional sum adders, fault-tolerant comparators, and the application of hot and cold standby topologies. These techniques are crucial in enhancing the reliability and resilience of digital circuits against faults.

- FPGA architecture
  A field-programmable gate array (**FPGA**) is an **integrated circuit** designed to be configured by a customer or a designer after manufacturing (hence the term field-programmable). The FPGA is programmed during the manufacturing process but can later be **re-programmed** to reflect any changes made to the device. An FPGA is based on a matrix of **configurable logic blocks (CLBs)** connected via programmable interconnects.



Internal Architecture of FPGA

- Configurable Logic Block (CLB)
  CLBs are the fundamental logic blocks in a FPGA. It consists of logic elements (LE), Lookup tables (LUT), multiplexers and flip flops. LUTs consist of input pins (receive input from surroundings), memory cell to store the precomputed output and the truth table that maps the output for the combination of input. CLBs can be made resilient or fault tolerant by various means like triple modular redundancy (TMR), Error detection and Correction, Built-in Self-Test (BIST) etc. One CLB consists of lookup tables, flip flops and mux stages.



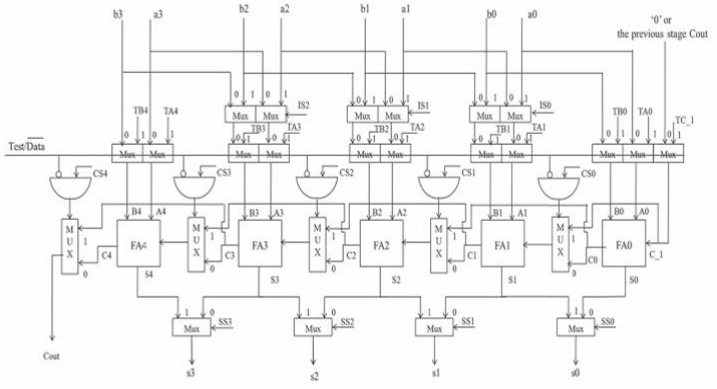
Rough Block Diagram of CLB

- Fault Tolerance Techniques

  A **fault** is a flaw within the system caused by an unintended discrepancy between the behavior of the implemented hardware and the expected behavior. They may be stuck-at faults, bridging faults, memory faults, delay faults etc.
  Fault tolerance is the ability of a system to retain of its normal operation even if some parts of it become non-operative. There are two main approaches for fault-tolerant design: **static** and **dynamic**.
  Static methods are robust and has higher fault coverage rate, but has a high area and power overhead. On the contrary, a more economical way of fault tolerance in terms of area and power is dynamic recovery, where spare modules become active on identification of faulty modules. But this method requires an efficient testing methodology and a proper reconfiguration unit to bypass the faulty modules.
  Static redundancy techniques include- Triple Modular Redundancy (TMR)**,** Dual Modular Redundancy (DMR)**,** N-Modular Redundancy (NMR)**,** Hamming Code**,** Parity Bits**,** Error-Correcting Codes (ECC) etc.
  Dynamic redundancy techniques include detecting, locating and eliminating an error by using spare modules along with active modules, such that a fault detected by the fault detection and reconfiguration unit, will bypass the faulty module and replace it with a fault free spare.

- Design of a self-reconfigurable adder for VLSI architecture

  Here we use a **ripple carry adder** and make it fault tolerant by using dynamic fault recovery. Ripple carry adder is an adder where the cout of one adder is the cin for the next adder, making it slower and increasing the latency.
  Dynamic fault recovery is automated fault recovery where the system works and when it encounters a fault the fault detection and reconfiguration unit, activates the spare module bypassing the faulty one.
  If only the sum bit is affected due to fault in one FA, the error is not carried over to the next FA. But if the carry bit of the faulty FA is affected, then the error is carried over to the next FAs and all FAs seem to be faulty as compared with the desired outputs.
  A 4-bit ripple carry adder has 1 spare and can thus handle one fault. If we have an 8-bit RCA then also it'll handle only one fault. But if we use two cascadable 4-bit RCA, 2 spare modules will be present so it can handle two faults.
  If we have a 64-bit RCA that is divided into k sub-blocks then the number of faults it can tolerate is 64/k. As the value of k increases, area overhead (extra silicon space required for additional components) decreases and the number of faults tolerated decreases.



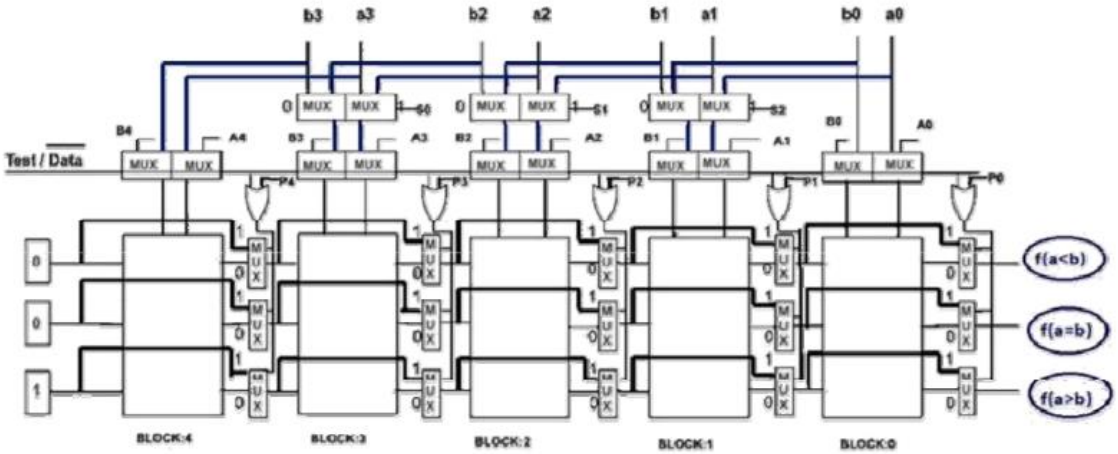
Single Fault Tolerant RCA

- Real time fault tolerance with hot standby topology for Conditional Sum Adder

  Real time fault tolerance means that the system must detect and counter a fault in a predefined time period within specified time constraints.
  Adders are basic functional blocks and here **Conditional Sum Adder** is used for parallel processing and high computational speed.
  Hot standby topology is a method where two systems- main system and spare system work parallelly so that when the main system encounters a fault the spare system directly takes over, reducing latency (delay).
  Here it uses dynamic redundancy technique where the spare modules are activated only when the active modules fail to operate or encounters a fault and is thus power efficient.
  In conditional sum adder it precomputes the output for both c=0 and c=1 and depending on the output of the previous block which becomes the select line of the MUX, the corresponding carry value is selected.
  During testing of a CSC (conditional selection cell- One CSC consists of two CC-conditional cell and 4 MUX) the inputs to the CSC is neglected and outputs are not considered, that is it is bypassed. If a fault is found then the CSC is bypassed and the inputs is routed to spare modules present.
  If the number of spares remains fixed but the system size increases then failure probability increases
  The system must be designed by **DFT (design for testability**) technique and it must be **C-testable**, i.e. the number of test vectors (test vectors are the values which are used to ensure proper working of the system), is independent of the size of ILA (iterative logic array).

- Fault tolerant architecture of 4-bit comparator

  Comparators are widely used in digital electronics, such as in CPUs and microcontrollers (MCUs). A magnitude digital comparator is a combinational circuit that compares two binary numbers and determines their relative magnitudes to find out whether one number is equal to, less than, or greater than the other number.
  Fault-tolerant comparator makes use of dynamic redundancy technique where it uses a spare comparator to bypass the faulty module in case of a fault being detected.



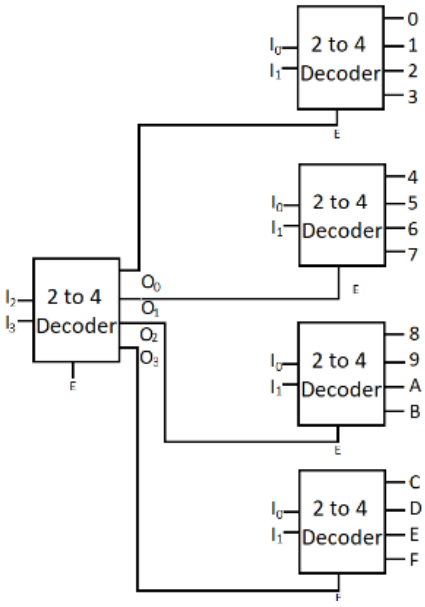
Circuit of 4-bit comparator

I made a detailed study of this circuit, including the test pattern generation circuit and the MUX select line circuit and to apply the knowledge as well for hands on application, I

designed a 2-bit comparator, with its very own test pattern generation circuit and MUX select line generation circuit.

- 4 to 16 decoder using 2 to 4 decoders

Decoders are one of the most integral parts of the Configurable Logic Blocks (CLBs) in FPGA. Decoders are combinational circuits that take n inputs and give 2^n outputs. In digital electronics, it is possible to design a 4:16 decoder by using 2:4 decoders.



Circuit diagram for a 4:16 decoder using 2:4 decoder

I1	I2	I1	I0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	YA	YB	YC	YD	YE	YF
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Truth table for Active Low 4:16 decoder

IMPLEMENTATION:

To implement this project, I have used Verilog language and Xilinx Vivado 2022.2 software. By using the concept of designing 4:16 decoder from 2:4 decoder, and dynamic redundancy, I designed a **Fault- tolerant 4:16 decoder** circuit by using a spare module to bypass the faulty module in case of fault.

The circuit design consists of 2 stages- **primary decoder stage** and the **secondary decoder** stage. From the truth table, it can be observed that when I3 and I2 were given as inputs to the primary decoder, it will produce the output for an active low 2:4 decoder. This output can be taken as the enable for the secondary stage decoders. The secondary decoder with enable as low, is activated and will produce the output for input I0 and I1.

For implementing this design as a fault-tolerant circuit, I added a spare decoder in the primary stage and a spare decoder in the secondary stage to take over if any one of the original or active module produces a faulty output.

For the primary stage,

```
decoder2to4 primary_decoder (
    .in({in[2],in[3] && x}),
    .out(primary_out)
);

decoder2to4 primary_decoder_spare (
    .in(in[3:2]),
    .out(primary_spare_out)
);

assign expected_out = (in == 2'b00) ? 4'b0111 :(in == 2'b01) ? 4'b1011 :(in == 2'b10) ? 4'b1101 :(in == 2'b11) ? 4'b1110 : 4'b0000;
assign primary_fault= |(primary_out ^ expected_out);
assign enable = primary_fault ? primary_spare_out : primary_out;
```

Here I have designed a primary decoder and a spare primary decoder. The same inputs in[3] and in[2] are given to both these decoders. One of the inputs in[3] is ANDed with ‘x’ which is an input taken for stuck at fault. If there is stuck-at 1 fault then the inputs to the decoder would not be affected, however if the input is stuck-at 0 or the output is affected by a fault anywhere else like if the decoder is faulty or if the wire connecting the decoder to the MUX input is faulty then it would produce a faulty output. To check if the output is faulty or not we take expected_out that will store the expected output for input values of in[3] and in[2]. If the output produced does not match the expected output (comparator stage is required here and is implemented by using a XOR gate (^) which is an inequality detector), then primary_fault bit becomes high, i.e., fault has been detected. If primary fault is 1 the MUX stage selects and assigns enable with the output from primary spare decoder otherwise it proceeds with the output from primary_decoder.

For the secondary stage,

```
genvar i;
 generate
     for (i = 0; i < 4; i = i + 1) begin: secondary_decoders
         decoder2to4 secondary_decoder (
             .in({cd[0], cd[1] && y}),
             .out(secondary_out[i])
         );
       end

         //Expected output based on the inputs
         assign expected_secondary_out[i] = (cd == 2'b00) ? 4'b0111 :
                                            (cd == 2'b01) ? 4'b1011 :
                                            (cd == 2'b10) ? 4'b1101 :
                                            (cd == 2'b11) ? 4'b1110 : 4'b0000;

         // Check for faults
         assign secondary_fault[i] = |(secondary_out[i] ^ expected_secondary_out[i]);
 endgenerate

 decoder2to4 secondary_decoder_spare (
     .in(cd[1:0]),
     .out(secondary_spare_out)
 );
```

Here I have used a generate block to instantiate four secondary decoders and handle fault detection efficiently. Inside the generate block, a for loop iterates four times to create instances of the decoder2to4 module. The input to each decoder is formed by cd[0] and the logical AND of cd[1] and ‘y’, which is the input stuck-at fault, with the outputs stored in the secondary_out array. Expected outputs for each decoder are calculated based on the input cd using a series of ternary operations, resulting in active-low outputs. Fault detection is performed by comparing the actual output of each decoder with its expected output through a bitwise XOR operation. The result is reduced to a single bit indicating a fault if any mismatch is detected. Additionally, a spare secondary decoder is instantiated outside the generate block, providing a fallback option in case any active secondary decoder fails.

```
always @(*)begin
   case(secondary_fault)
   4'b0001: begin
     mux_out[0]=secondary_out[1];
     mux_out[1]=secondary_out[2];
     mux_out[2]=secondary_out[3];
     mux_out[3]=secondary_spare_out;
    end
    4'b0010: begin
     mux_out[0]=secondary_out[0];
     mux_out[1]=secondary_out[2];
     mux_out[2]=secondary_out[3];
     mux_out[3]=secondary_spare_out;
    end
    4'b0100: begin
     mux_out[0]=secondary_out[0];
     mux_out[1]=secondary_out[1];
     mux_out[2]=secondary_out[3];
     mux_out[3]=secondary_spare_out;
    end
    4'b1000: begin
     mux_out[0]=secondary_out[0];
     mux_out[1]=secondary_out[1];
     mux_out[2]=secondary_out[2];
     mux_out[3]=secondary_spare_out;
    end
    default:begin
     mux_out[0]=secondary_out[0];
     mux_out[1]=secondary_out[1];
     mux_out[2]=secondary_out[2];
     mux_out[3]=secondary_out[3];
    end
    endcase
    end
```

Here I have created an always block that continuously monitors changes and dynamically reconfigures the output `mux_out` based on the status of secondary_fault. The case statement evaluates the 4-bit secondary_fault signal, where each bit represents a fault condition for one of the secondary decoders. Depending on which bit is set, the mux_out array is adjusted to reassign the outputs of the remaining operational secondary decoders and the spare decoder.

If the least significant bit of secondary_fault (4'b0001) is set, it indicates that the first secondary decoder has failed. In this case, the outputs from the second, third, and fourth secondary decoders are assigned to mux_out[0], mux_out[1], and mux_out[2] respectively, while mux_out[3] is assigned the output of the spare secondary decoder.

Similarly, if the second bit (4'b0010) is set, the first secondary decoder remains active, but the outputs from the third and fourth secondary decoders, along with the spare decoder, are reassigned accordingly.

If the third bit (4'b0100) is set, the first and second secondary decoders continue to provide outputs, while the fourth secondary decoder and the spare decoder are used for mux_out[2] and mux_out[3].

If the most significant bit (4'b1000) is set, the first three secondary decoders remain operational, and the spare decoder is used for mux_out[3].

If none of the bits in secondary_fault are set (default case), all secondary decoders are functioning correctly, and mux_out directly receives their outputs without any reassignment.

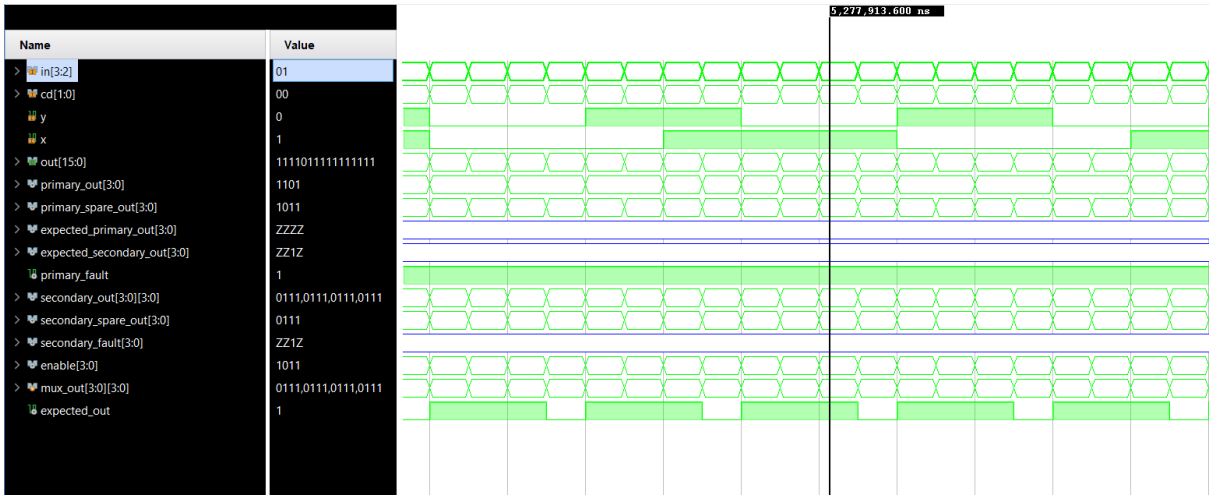
For the final output stage,

```
    always @(*) begin
        out[3:0]   = enable[0] ? 4'b1111 : mux_out[0];
        out[7:4]   = enable[1] ? 4'b1111 : mux_out[1];
        out[11:8]  = enable[2] ? 4'b1111 : mux_out[2];
        out[15:12] = enable[3] ? 4'b1111 : mux_out[3];
    end
endmodule
```

This part of ternary operators has been used to connect the primary decoder stage and the secondary decoder stage. The always @(*) block continuously monitors changes in any of the signals inside it, assigning values to the output out based on the conditions specified by the enable signals. For each 4-bit segment of the out signal, the block checks the corresponding enable signal to determine if a fault is present. If an enable signal is 1, indicating a fault in the primary decoder output, the code assigns 4'b1111 (all high, indicating a fault) to that segment of out. If the enable signal is 0, the code assigns the corresponding value from mux_out, which is the output from the secondary decoder after fault handling. This process is repeated for each 4-bit segment (out[3:0], out[7:4], out[11:8], and out[15:12]). This design effectively merges the output of the primary and secondary decoders and produces the corresponding output.

SIMULATION AND VALIDATION:

To verify the working of our circuit, we test it for a particular case and observe the simulation output. Let the input be 0100,



Simulation observed for the given input

If the input is given as 0100, that means inputs to the primary decoder are 01. Here we also inject stuck-at 0 fault (x=0) and observe the enable. According to the truth table for an active low 2:4 decoder, the output for 01 is 1011. So here we can observe that due to the stuck-at fault, output produced by primary decoder is 1101 which is faulty so the MUX chooses the primary_spare_out(1011) so the final output at the end of the primary decoder stage i.e, enable, is 1011 and is fault-free.

Next inputs to the secondary decoder are 00 (cd), and here we inject stuck-at fault 1, the expected output of the secondary decoder for the input 00 would normally be 4'b0111. However, due to the stuck-at fault, the actual output may deviate from this expected value. The fault detection mechanism compares the actual output with the expected output, and the MUX output is selected accordingly.

The final output is generated by combining both enable and output of secondary decoder stage, and the output produced is 1111011111111111 which is same as the expected output from a 4:16 decoder with inputs as 0100.

As the expected solution matches our circuit output, hence the circuit design is validated.

CONCLUSION:

The design and implementation of a fault-tolerant decoder circuit for FPGAs have demonstrated the effectiveness of dynamic redundancy reconfiguration in maintaining system reliability. By integrating spare decoders and dynamically switching to these spares upon fault detection, the system ensures uninterrupted functionality even in the presence of faults. This approach not only enhances the resilience of FPGA-based systems but also optimizes resource utilization, offering a significant improvement over traditional static redundancy method. The rigorous validation process, including fault injection and performance evaluation, confirms the robustness of the design. This project contributes to the advancement of fault-tolerant techniques in digital circuits, paving the way for more reliable and efficient FPGA systems in critical applications.

Future scope includes optimizing resource utilization and power consumption, enhancing fault detection and correction mechanisms, exploring scalability, and evaluating the economic impact of fault-tolerant designs. These areas offer promising opportunities for further research and innovation, paving the way for more reliable and efficient FPGA systems.

Overall, this project successfully meets its goals and lays a strong groundwork for future progress in designing fault-tolerant digital circuits. As FPGA technology continues to grow and improve, the insights and methods developed in this project will be essential in tackling the challenges of future increasingly complex and vital applications.

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