



Department of Computer Science & Engineering
Microprocessor & Computer Architecture
MPCA-Laboratory/Assignment/Hands-on/Project
UE20CS252

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SECTION: K

Sl. No	Programs
Week No.3	<p>1 Write a program in ARM7TDMI-ISA to find the sum of N data items at alternate [odd or even positions] locations in the memory. Store the result in the memory location.</p> <p>a. Use Pre-indexing addressing mode</p> <pre>.DATA A:.WORD 1,2,3,4 SUM:.WORD 0 .TEXT MOV R2,#0 LDR R1,=A LDR R3,=SUM MOV R5,#0 MOV R4,#1 ;counter Loop: LDR R6,[R1,R5] ;PREINDEXING WITHOUT WRITEBACK ADD R2,R2,R6 ADD R5,R5,#8 ADD R4,R4,#1 CMP R4,#3 BNE Loop STR R2,[R3]</pre>

SWI 0X011

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 0
R1 : 4156
R2 : 0
R3 : 4172
R4 : 1
R5 : 0
R6 : 0
R7 : 0
R8 : 0
R9 : 0
R10 (s1) : 0
R11 (fp) : 0
R12 (ip) : 0
R13 (sp) : 21504
R14 (lr) : 0
R15 (pc) : 4116

CPSR Register

Negative (N) : 0
Zero (Z) : 0
Carry (C) : 0
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1
Thumb (T) : 0
CPU Mode : Sy

0x000000df

pre.s

```
.DATA
0000103C: A: .WORD 1,2,3,4
0000104C: SUM: .WORD 0

.TEXT
00001000:E3A02000 MOV R2,#0
00001004:E59F1028 LDR R1,=A
00001008:E59F3028 LDR R3,=SUM
0000100C:E3A05000 MOV R5,#0
00001010:E3A04001 MOV R4,#1 ;counter

00001014:E7916005 Loop: LDR R6,[R1,R5] ;PREINDEXING WITHOUT WRITEBACK
00001018:E0822006 ADD R2,R2,R6
0000101C:E2855008 ADD R5,R5,#8
00001020:E2844001 ADD R4,R4,#1
00001024:E3540003 CMP R4,#3
00001028:1AFFFFF9 BNE Loop
0000102C:E5832000 STR R2,[R3]
SWI 0X011
```

MemoryView0

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file C:\Users\ankit\Downloads\pre.s

b. Use Post- Indexing addressing mode

;post indexing

.DATA

A: .WORD 1,2,3,4

SUM: .WORD 0

.TEXT

MOV R2,#0

LDR R1,=A

LDR R3,=SUM

MOV R5,#8

Loop: LDR R6,[R1],R5 ;post indexing or(SR1,#4)

ADD R2,R2,R6

ADD R4,R4,#1

CMP R4,#3
 BNE Loop
 STR R2,[R3]
 SWI 0X011

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose f

Hexadecimal
Unsigned Decimal
Signed Decimal

R0	: 0
R1	: 4148
R2	: 0
R3	: 4164
R4	: 0
R5	: 8
R6	: 0
R7	: 0
R8	: 0
R9	: 0
R10 (s1)	: 0
R11 (fp)	: 0
R12 (ip)	: 0
R13 (sp)	: 21504
R14 (lr)	: 0
R15 (pc)	: 4112

CPSR Register

Negative (N) : 0

Zero (Z) : 0

Carry (C) : 0

Overflow (V) : 0

IRQ Disable: 1

FIQ Disable: 1

Thumb (T) : 0

CPU Mode : Sy

0x000000df

post.s

```

;post indexing
.DATA
00001034:      A: .WORD 1,2,3,4
00001044:      SUM: .WORD 0

.TEXT
00001000:E3A02000  MOV R2,#0
00001004:E59F1020  LDR R1,=A
00001008:E59F3020  LDR R3,=SUM
0000100C:E3A05008  MOV R5,#8

00001010:E6916005  Loop: LDR R6,[R1],R5 ;post indexing or(SR1,#4)
00001014:E0822006          ADD R2,R2,R6
00001018:E2844001          ADD R4,R4,#1
0000101C:E3540003  CMP R4,#3
00001020:1AFFFFFFA  BNE Loop
00001024:E5832000  STR R2,[R3]
SWI 0X011
  
```

MemoryView0

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file C:\Users\ankit\Downloads\post.s

c. Use Auto-indexing addressing mode

```

.DATA
A:.WORD 1,2,3,4
SUM:.WORD 0

.TEXT
MOV R2,#0
LDR R1,=A
LDR R3,=SUM
MOV R5,#8
MOV R4,#1 ;counter
SUB R1,R1,#8
  
```

```

Loop: LDR R6,[R1,R5]! ;PREINDEXING WITH WRITEBACK
      ADD R2,R2,R6
      ADD R4,R4,#1
      CMP R4,#3
      BNE Loop
      STR R2,[R3]
      SWI 0X011

```

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 0

R1 : 4148

R2 : 0

R3 : 4172

R4 : 1

R5 : 8

R6 : 0

R7 : 0

R8 : 0

R9 : 0

R10 (s1) : 0

R11 (fp) : 0

R12 (ip) : 0

R13 (sp) : 21504

R14 (lr) : 0

R15 (pc) : 4120

CPSR Register

Negative (N) : 0

Zero (Z) : 0

Carry (C) : 0

Overflow (V) : 0

IRQ Disable : 1

FIQ Disable : 1

Thumb (T) : 0

CPU Mode : Sy

0x000000df

auto.s

```

.DATA
0000103C: A: .WORD 1,2,3,4
0000104C: SUM: .WORD 0

.TEXT
00001000:E3A02000 MOV R2,#0
00001004:E59F1028 LDR R1,=A
00001008:E59F3028 LDR R3,=SUM
0000100C:E3A05008 MOV R5,#8
00001010:E3A04001 MOV R4,#1 ;counter
00001014:E2411008 SUB R1,R1,#8

00001018:E7B16005 Loop: LDR R6,[R1,R5]! ;PREINDEXING WITH WRITEBACK
0000101C:E0822006 ADD R2,R2,R6
00001020:E2844001 ADD R4,R4,#1
00001024:E3540003 CMP R4,#3
00001028:1AFFFFFFA BNE Loop
0000102C:E5832000 STR R2,[R3]
SWI 0X011

```

MemoryView0

OutputView

Console Stdin/Stdout/Stderr

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