MPCA LAB WEEK-1

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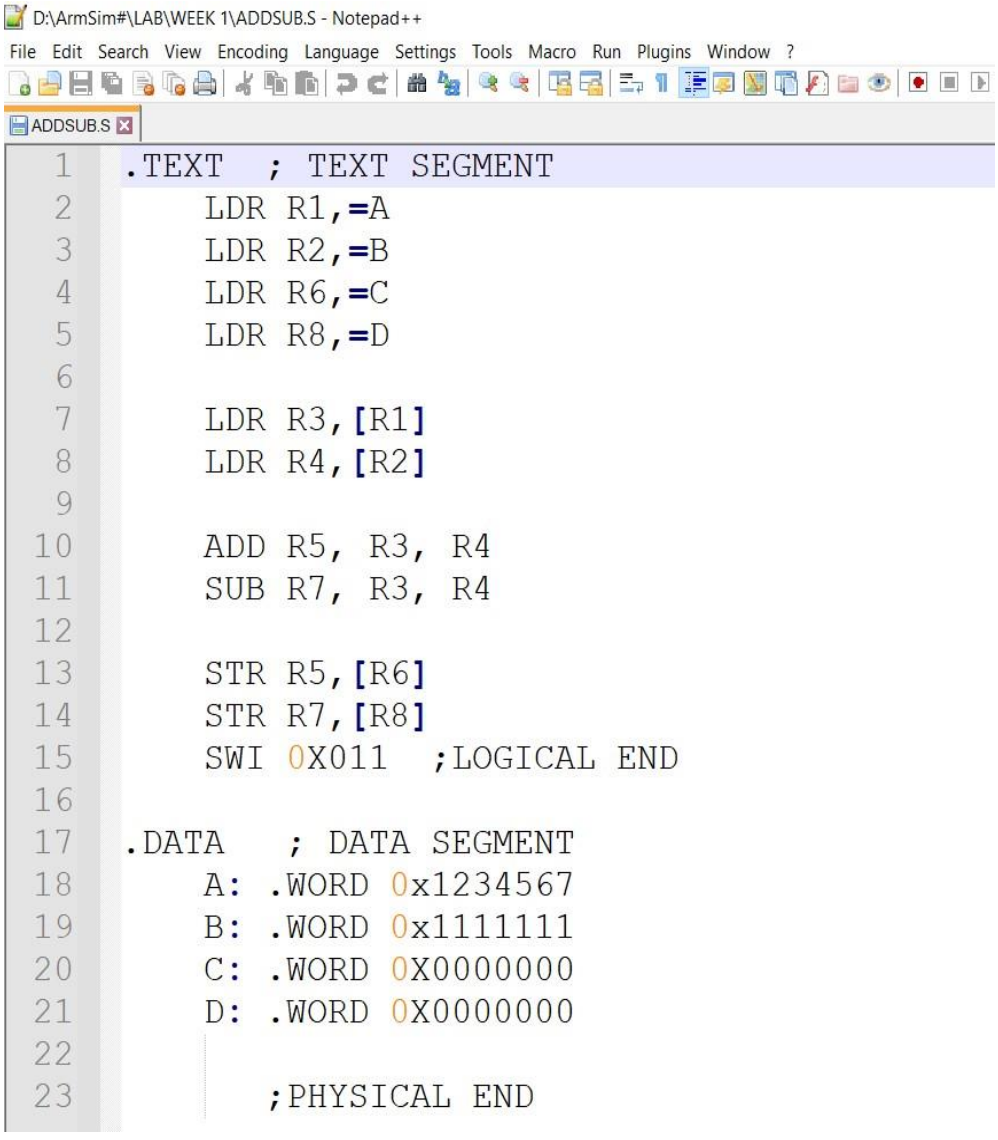
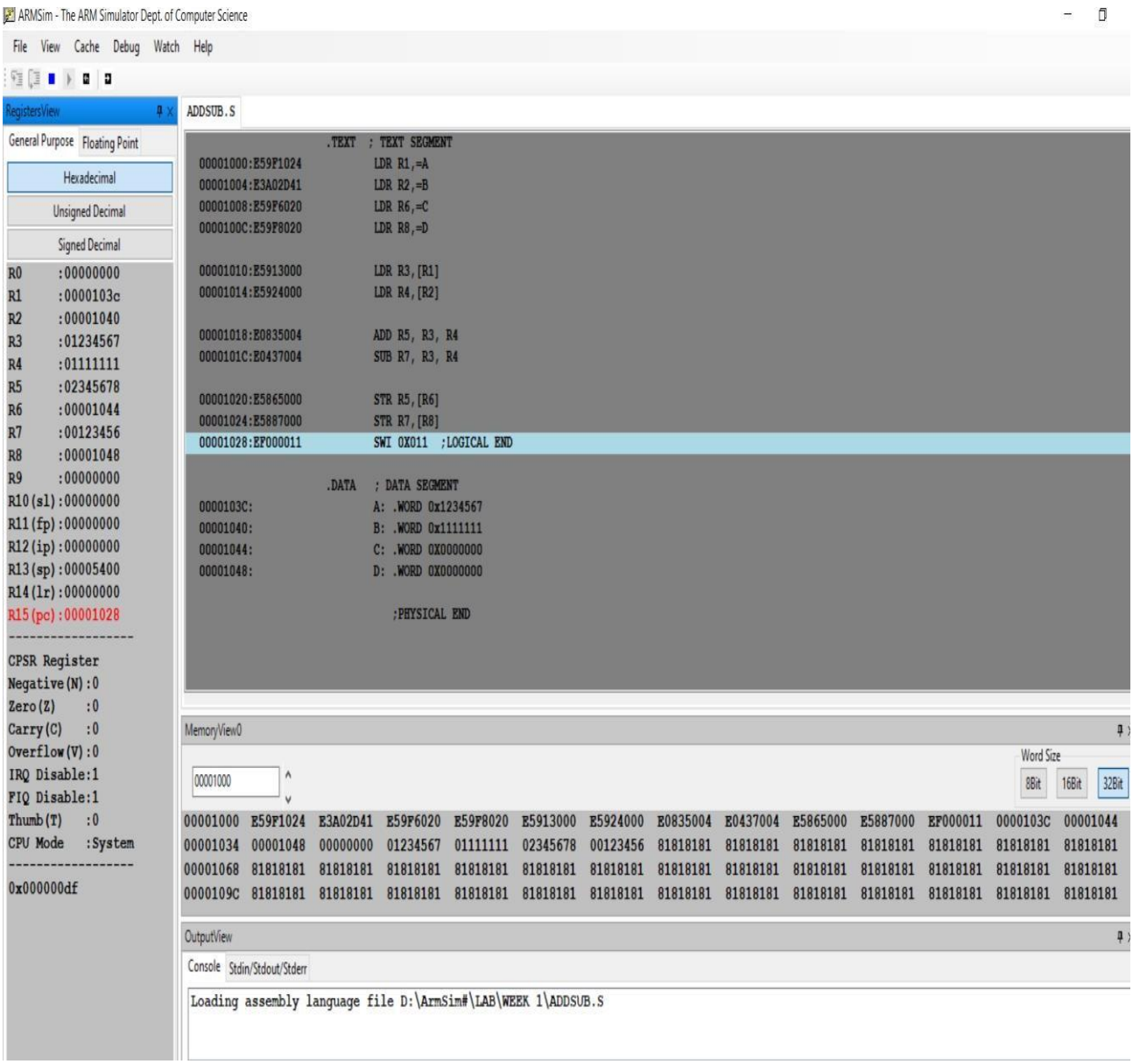
SRN: PES1UG20CS626

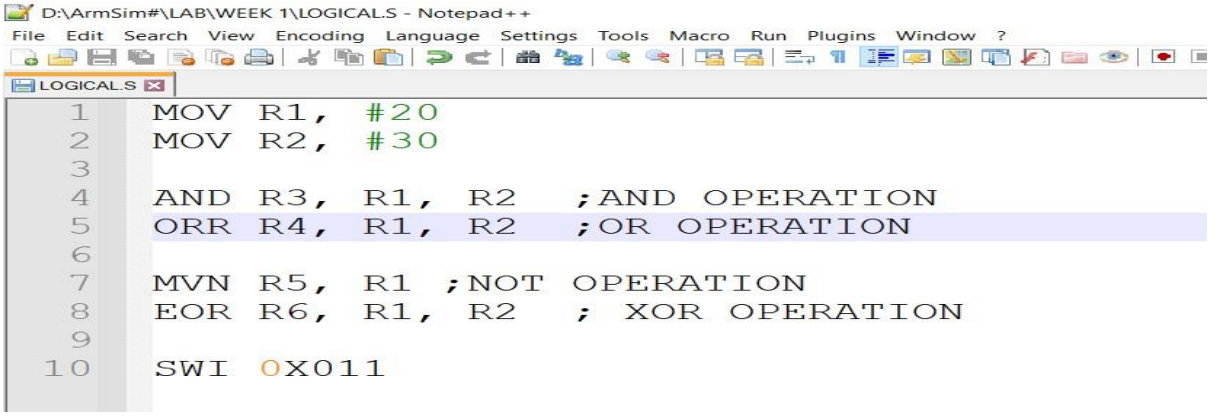
SECTION: K

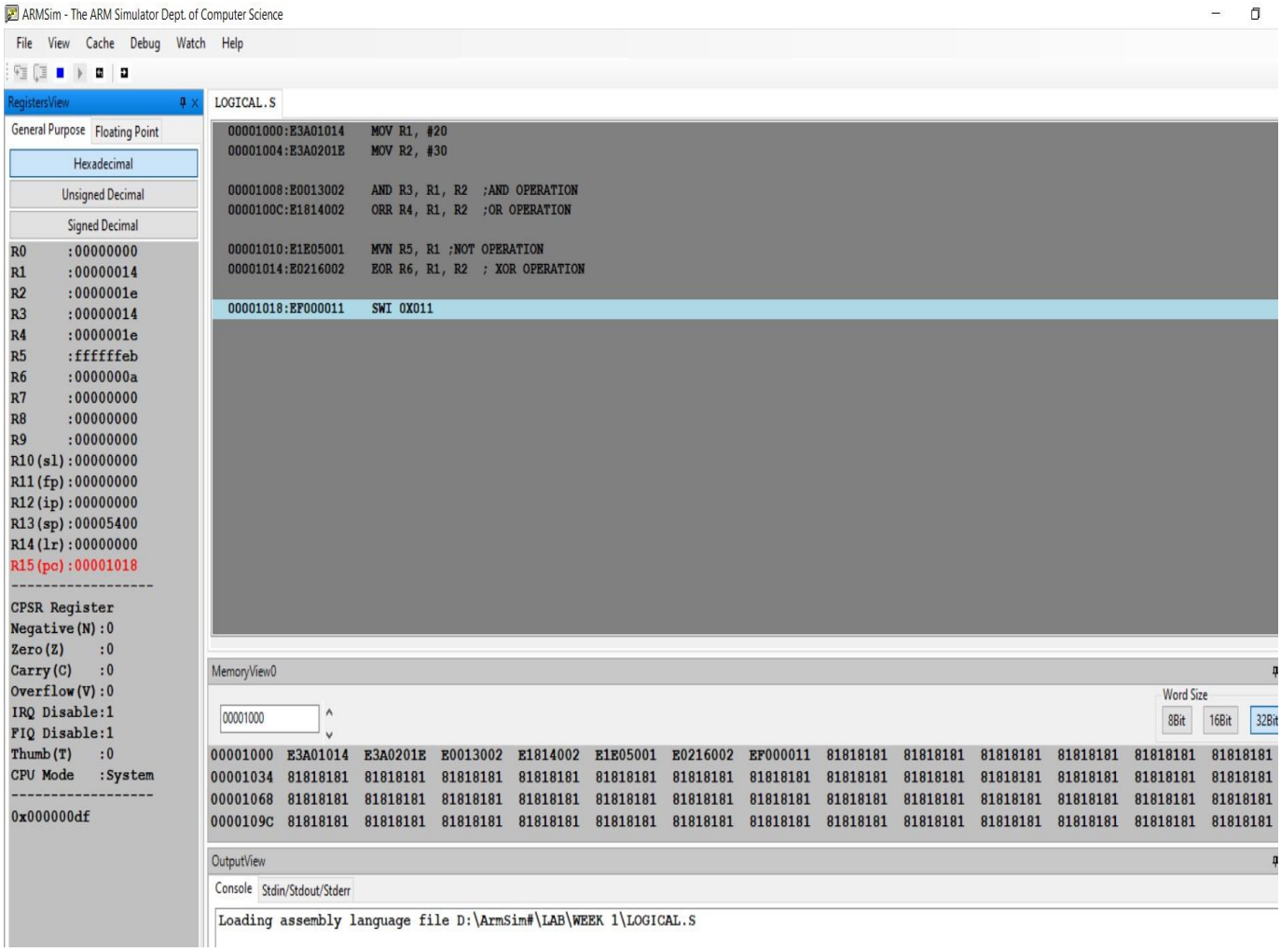
a. Write an ALP using ARM instruction set to add and subtract two 32 bit numbers. Both numbers are in registers.



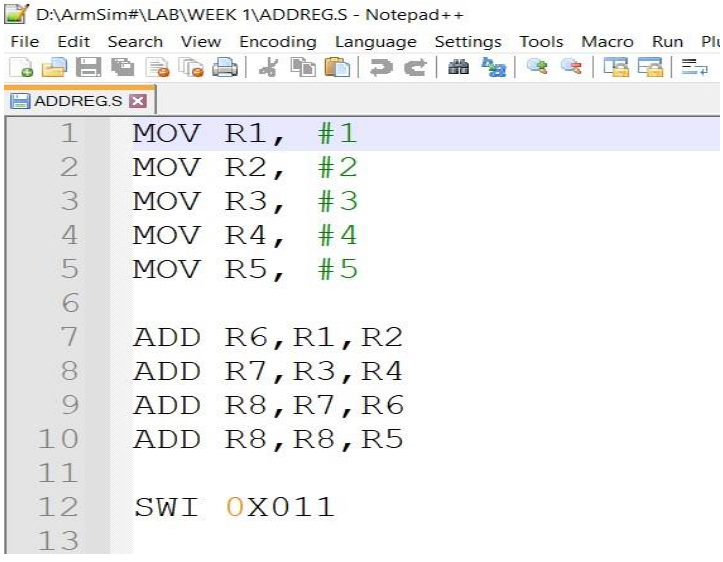


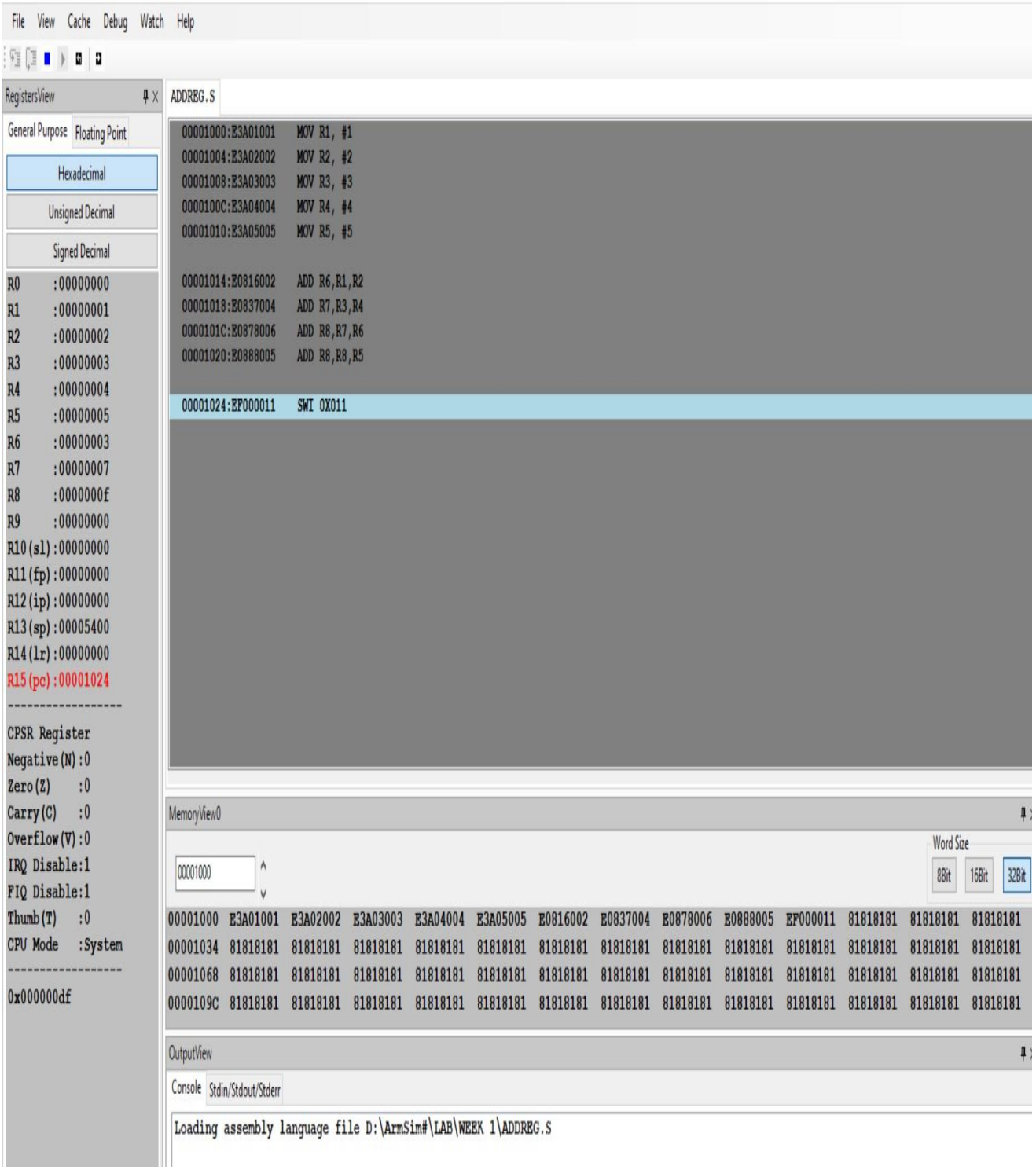
b. Write an ALP to demonstrate logical operations. All operands are in registers.





c. Write an ALP to add 5 numbers where values are present in registers.





2. Assignment:

d. Write an ALP using ARM instruction set to check if a number stored in a register is even or odd.

D:\ArmSim#\LAB\WEEK 1\EVENORODD.S - Notepad++

File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?

EVENORODD.S

```
1   .TEXT
2           ;Loading number and setting Zero Flag
3
4           MOV R0, #10
5           ANDs R0, R0, #1
6
7           ;condition entered if Z=1 -> odd number
8
9           BEQ CONDITION
10                  MOV R1, #1
11                  B EXIT
12          CONDITION:
13                  MOV R2, #1
14          EXIT:
15                  SWI 0x011
16  .END
```

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose | Floating Point

Hexadecimal | Unsigned Decimal | Signed Decimal

```
R0      :00000000
R1      :00000000
R2      :00000001
R3      :00000000
R4      :00000000
R5      :00000000
R6      :00000000
R7      :00000000
R8      :00000000
R9      :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):00001018
----------------
CPSR Register
Negative(N):0
Zero(Z)    :1
Carry(C)   :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
----------------
0x400000df
```

EVENORODD.S

```
                .TEXT
                        ;Loading number and setting Zero Flag

00001000:E3A0000A       MOV R0, #10
00001004:E2100001       ANDs R0, R0, #1

                        ;condition entered if Z=1 -> odd number

00001008:0A000001       BEQ CONDITION
0000100C:E3A01001               MOV R1, #1
00001010:EA000000               B EXIT
00001014:               CONDITION:
00001014:E3A02001               MOV R2, #1
00001018:               EXIT:
00001018:EF000011               SWI 0x011
                .END
```

MemoryView0

00001000 | Word Size: 8Bit | 16Bit | 32Bit

```
00001000 E3A0000A E2100001 0A000001 E3A01001 EA000000 E3A02001 EF000011 81818181 81818181 81818181 81818181 81818181 81818181
00001034 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
00001068 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
0000109C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
```

OutputView

Console | Stdin/Stdout/Stderr

```
Loading assembly language file D:\ArmSim#\LAB\WEEK 1\EVENORODD.S
```

e. Write an ALP to compare the value of R0 and R1, add if R0 = R1, else subtract.

D:\ArmSim#\LAB\WEEK 1\COMPARE.S - Notepad++

File Edit Search View Encoding Language Settings Tools Ma

COMPARE.S

```
1    MOV  R0,#1
2    MOV  R1,#1
3
4    CMP  R0,R1
5
6    BEQ  L1
7    SUB  R3,R0,R1
8    SWI  0X011
9
10   L1:  ADD  R2,R0,R1
11
```

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File View Cache Debug Watch Help

RegistersView

General Purpose | Floating Point

Hexadecimal | Unsigned Decimal | Signed Decimal

```
R0      :00000001
R1      :00000001
R2      :00000002
R3      :00000000
R4      :00000000
R5      :00000000
R6      :00000000
R7      :00000000
R8      :00000000
R9      :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):0000104c
----------------
CPSR Register
Negative(N):0
Zero(Z)    :1
Carry(C)   :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
----------------
0x600000df
```

COMPARE.S

```
00001000:E3A00001   MOV R0,#1
00001004:E3A01001   MOV R1,#1

00001008:E1500001   CMP R0,R1

0000100C:0A000001   BEQ L1
00001010:E0403001   SUB R3,R0,R1
00001014:EF000011   SWI 0X011

00001018:E0802001   L1: ADD R2,R0,R1
```

MemoryView0

00001000

Word Size: 8Bit 16Bit 32Bit

```
00001000 E3A00001 E3A01001 E1500001 0A000001 E0403001 EF000011 E0802001 81818181 81818181 81818181 81818181 81818181 81818181
00001034 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
00001068 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
0000109C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
```

OutputView

Console | Stdin/Stdout/Stderr

```
Loading assembly language file D:\ArmSim#\LAB\WEEK 1\COMPARE.S
```

f. **Based on the value of the number in R0, Write an ALP to store 1 in R1 if R0 is zero, Store 2 in R1 if R0 is positive, Store 3 in R1 if R0 is negative.**

D:\ArmSim#\LAB\WEEK 1\W106.S - Notepad++

File Edit Search View Encoding Language Settings

W106.S

```
1   MOV  R0,#5
2
3   CMP  R0,#0
4   BEQ  L1
5   BGT  L2
6   MOV  R1,#3
7   SWI  0X011
8
9   L1:MOV  R1,#1
10  L2:MOV  R1,#2
11
12
```

RESULT: >0

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File View Cache Debug Watch Help

RegistersView

General Purpose | Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

```
R0      :00000005
R1      :00000002
R2      :00000000
R3      :00000000
R4      :00000000
R5      :00000000
R6      :00000000
R7      :00000000
R8      :00000000
R9      :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):0000101c
-----------------
CPSR Register
Negative(N):0
Zero(Z)    :0
Carry(C)   :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
-----------------
0x200000df
```

W106.S

```
00001000:E3A00005   MOV R0,#5

00001004:E3500000   CMP R0,#0
00001008:0A000001   BEQ L1
0000100C:CA000001   BGT L2
00001010:E3A01003   MOV R1,#3


00001014:E3A01001   L1:MOV R1,#1
00001018:E3A01002   L2:MOV R1,#2
0000101C:EF000011   SWI 0X011
```

MemoryView0

00001000

Word Size: 8Bit 16Bit 32Bit

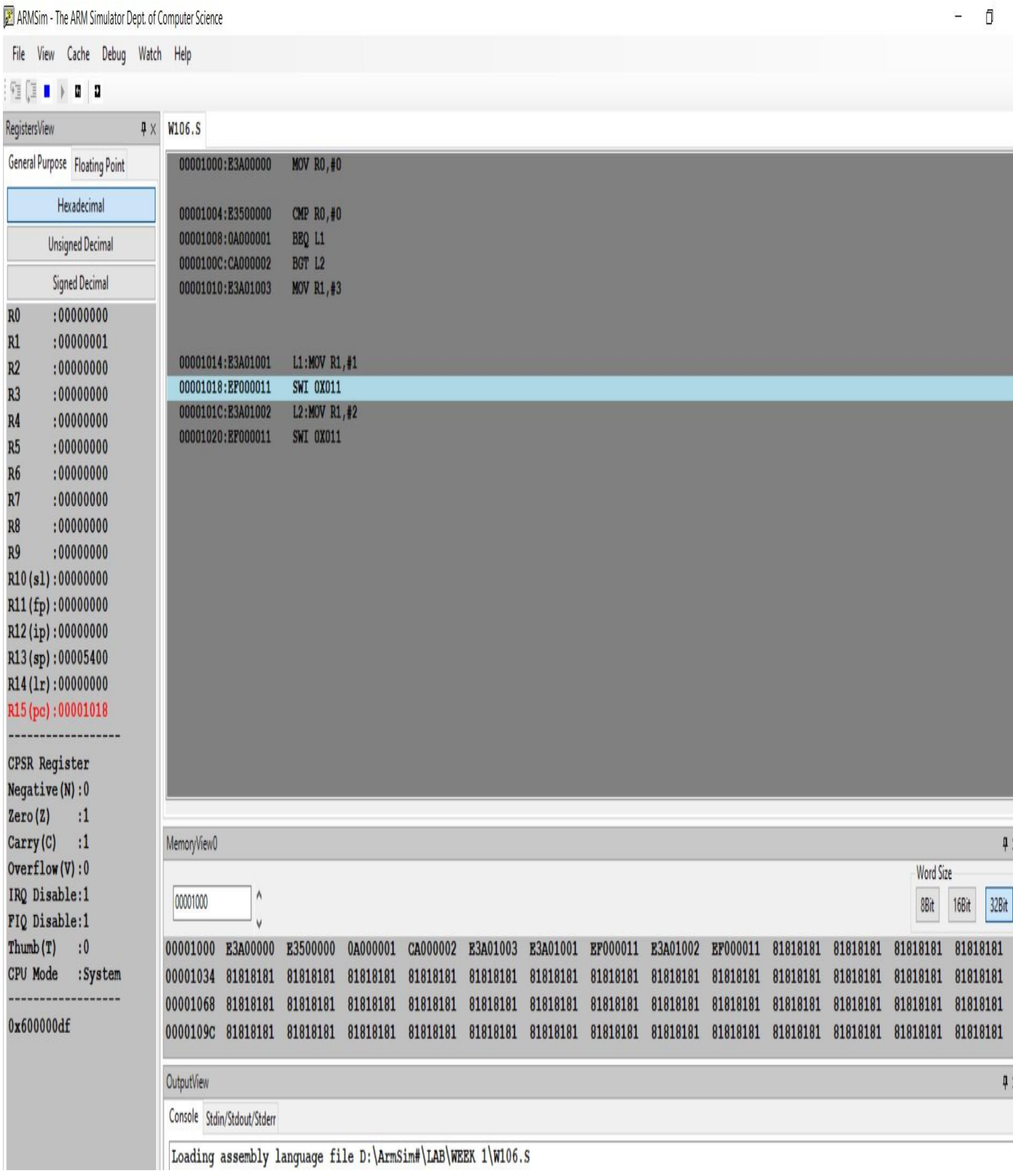
```
00001000 E3A00005 E3500000 0A000001 CA000001 E3A01003 E3A01001 E3A01002 EF000011 81818181 81818181 81818181 81818181 81818181
00001034 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
00001068 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
0000109C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
```

OutputView

Console | Stdin/Stdout/Stderr

```
Loading assembly language file D:\ArmSim#\LAB\WEEK 1\W106.S
```

RESULT = 0



RESULT <0

*D:\ArmSim#\LAB\WEEK 1\W106.S - Notepad++

File Edit Search View Encoding Language Settin

W106.S

```
1   MOV R0,#-1
2   CONDITION:
3   CMP R0,#0
4   BEQ L1
5   BGT L2
6   ELSE:
7   MOV R1,#3
8   SWI 0X011
9
10  L1:MOV R1,#1
11  L2:MOV R1,#2
12
```

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File View Cache Debug Watch Help

RegistersView

General Purpose | Floating Point

Hexadecimal | Unsigned Decimal | Signed Decimal

```
R0      :ffffffff
R1      :00000003
R2      :00000000
R3      :00000000
R4      :00000000
R5      :00000000
R6      :00000000
R7      :00000000
R8      :00000000
R9      :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):00001014
----------------
CPSR Register
Negative(N):1
Zero(Z)    :0
Carry(C)   :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
----------------
0xa00000df
```

W106.S

```
00001000:E3E00000   MOV R0,#-1
00001004:           CONDITION:
00001004:E3500000   CMP R0,#0
00001008:0A000002   BEQ L1
0000100C:CA000002   BGT L2
00001010:           ELSE:

00001010:E3A01003   MOV R1,#3
00001014:EF000011   SWI 0X011

00001018:E3A01001   L1:MOV R1,#1
0000101C:E3A01002   L2:MOV R1,#2
```

MemoryView0

00001000

Word Size: 8Bit | 16Bit | 32Bit

```
00001000 E3E00000 E3500000 0A000002 CA000002 E3A01003 EF000011 E3A01001 E3A01002 81818181 81818181 81818181 81818181 81818181 81818181
00001034 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
00001068 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
0000109C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
```

OutputView

Console | Stdin/Stdout/Stderr

```
Loading assembly language file D:\ArmSim#\LAB\WEEK 1\W106.S
```