

Development of Virtual lab :Round 3 -Lab Manual - Template (Worksheet)

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Discipline to which the Lab belongs: Information Technology

Name of the Lab: Welcome to logic design and computer organisation virtual lab

Name of experiment:CARRY LOOK AHEAD ADDER

(only one Experiment per worksheet):

Kindly Refer these documents before filling the worksheet

Coursework (MOOC) on Pedagogy , Storyboard , Lab Manual : <http://bit.ly/Vlabs-MOOC>

Additional Documentation booklet for reference. <http://vlabs.iitb.ac.in/vlabs-dev/document.php>

Sample Git Repository. : <http://github.com/ankitkuntal18/virtual-lab.git>

Round 2

1. Aim and Objective

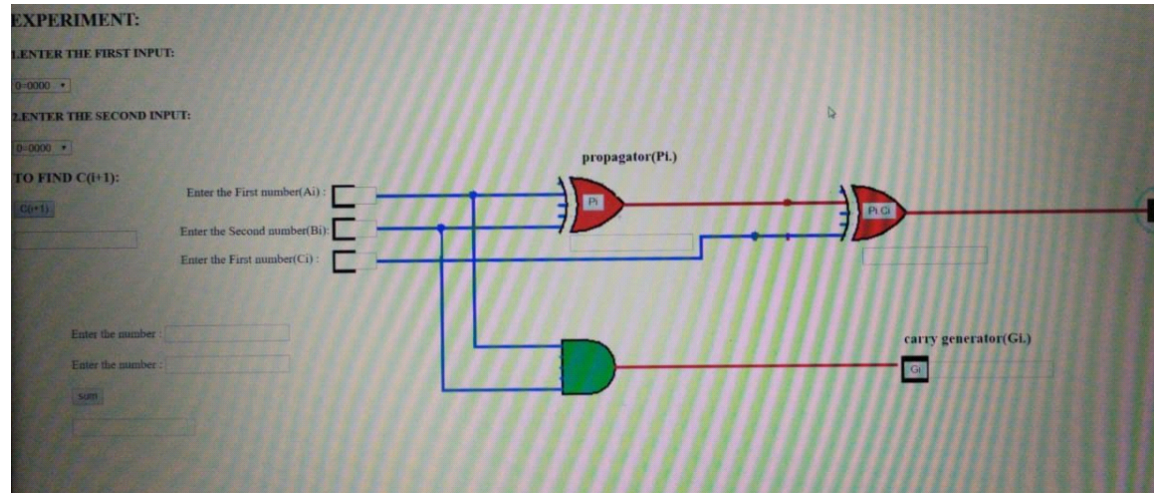
aim of the experiment is to perform the addition using carry look ahead adder in less time.

objective of this experiment is to acknowledge the carry generate and carry propagate.

2. Theory

the idea to look at the lower adder bits is to see if a higher order carry is to be generated which uses two functions carry generate G_i and carry propagate P_i . Even to execute the experiment as directed in the procedure.

3. Procedure (Protocol for navigating through the simulator with screenshots)



First select the inputs A and B and after that choose the last digit of them which will give A_i and B_i and thus you can calculate P_i and then even select the value of $C_i(0,1)$ than after this you will get the value of G_i as the inputs A and B through AND gate.

4. Pre test Assessments (Highlight the correct option with bold text)

Question 1 Which adder is best to perform the addition operation in less time

Option 1 N-bit parallel adder

Option 2 Carry look ahead adder

Option 3 both of the above

Option 4 None of the above

(Correct answer)Option 2

5. Post test Assessments (Write least one question for each learning objective from round 1)

For Learning Objective 1

Question 1 Correct formula of G_i used

Option 1 $A * C_i$

Option 2 $A_i * B_i$

Option 3 $B_i * C_{i+1}$

Option 4 $A_i * B$

For Learning Objective 2

Question 2 The P_i is calculated using which logic gate

Option 1 XOR

Option 2 AND

Option 3 OR

Option 4 NAND

6. References: Mr Dhananjay Bisen