

AXI Write Channel Specification

Revision 1.0

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1. AXI Protocol Overview

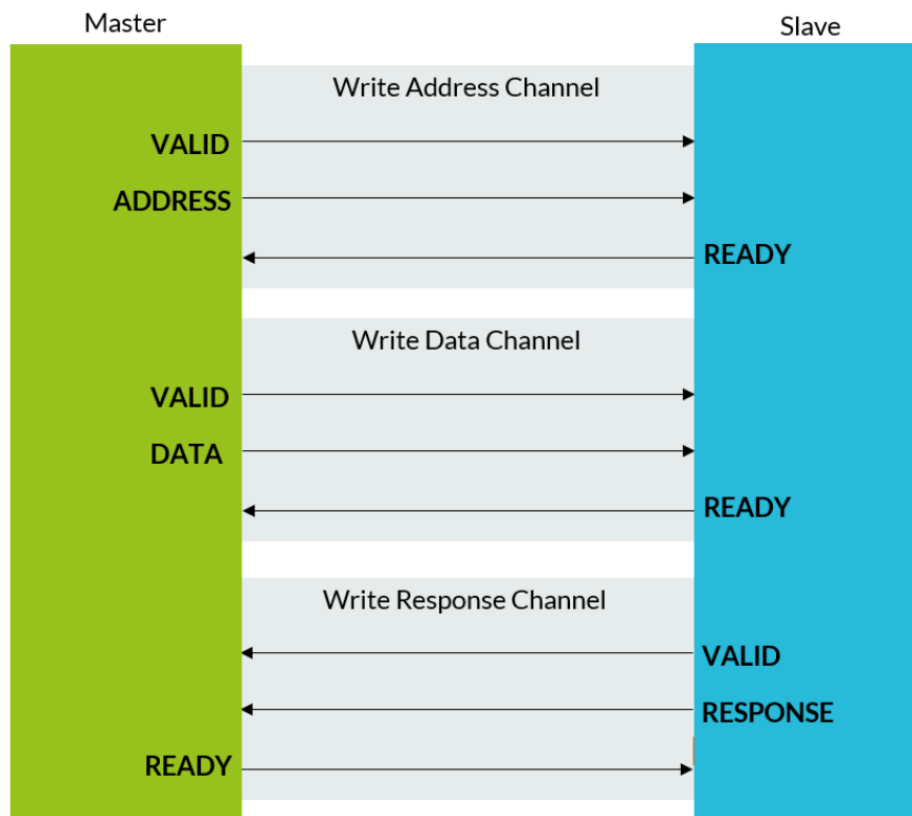


Fig.1. AXI write channel overview

AXI offers three different type of channels, write, read and snoop channel. This specification sheet is solely for write channel. Above figure shows three different type of channels present in the AXI write channel. This revision includes offered signals for our requirements. Write address channel (write request channel) is used for transferring address to from the manager/master to the subordinate/slave. Write data channel is used to transfer data from the manager/master to the subordinate/slave. Response data channel sends the information about the transfer or the transactions made by the write request/data channel

Brief description of these channels can be referred from signal description.

2. Channel Transfers and Transactions

For channel handshake waveforms please refer signal description

* Response channel waveforms are not added in this revision

3. Channel Signals

The channel used for transaction are:

- Write Request
- Write Data
- Write Response

Write Request(AW) channel Signals	AXI Signal Description		
AWVALID	Asserted by master which shows master is ready to send data or the data which is sent is valid. It is a write request valid indicator		
AWREADY	Asserted by slave which shows slave is ready to accept the data from the master. It is a request ready indicator		
AWADDR[31:0]	32-bit address which is sent by master		
AWSIZE[1:0]	It indicates maximum number of bytes in each data transfer		
AWBURST[1:0]	Describes how the address increments between transfers in a transaction.		
	AxBURST	Label	Meaning
	2'b00	Fixed	Fixed Burst
	2'b01	Incr	Incrementing Burst
	2'b10	Wrapping	Wrapping Burst
	2'b11	Burst Reserved	-
Write Data (W) channel signals	AXI Signal Description		
WVALID	Write data valid indicator		
WREADY	Write data ready indicator		
WLAST	Indicates the last write data transfer of a transaction		
WDATA[x:0]	The data signal which can be 8, 16, 32, 64, 128, 256, 512, 1024 bits.		
Write Response (B) channel signals	AXI signal Description		
BVALID	Write response valid indicator		
BREADY	Write response ready indicator		

4. Feature List

Following features will be covered in the design. Kindly adhere to same.

1. Write address channel

1.1. Handshake mechanism

a) Reset assertion and de-assertion

- **ARESETn** is active-low asynchronous reset. De-assertion must be synchronous with **ACLK**.
- Following conditions should be met with master/ manager.
 1. Master/manager must drive **AWVALID**, **WVALID** to zero.
 2. Slave/subordinate must drive **BVALID** low.
 3. All other signals can be driven to another value.

b) Channel Handshake

All AXI channels use the same **VALID/READY** handshake process to transfer address, data and control information. Transfer only occurs when both the signals are **HIGH**.

Following three scenarios should be considered for **VALID** and **READY**.

- Valid before ready handshake

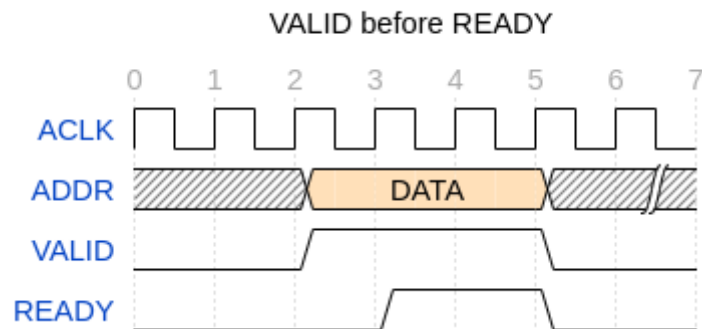


fig.2 VALID before READY signal

The source presents **DATA** after **T2** along with **VALID**. The **READY** is recognized at **T4**. Therefore the source must keep this information stable until **READY** assertion is sampled. Valid data is considered at **T4** when both **VALID** and **READY** are **HIGH**

- Ready before valid handshake

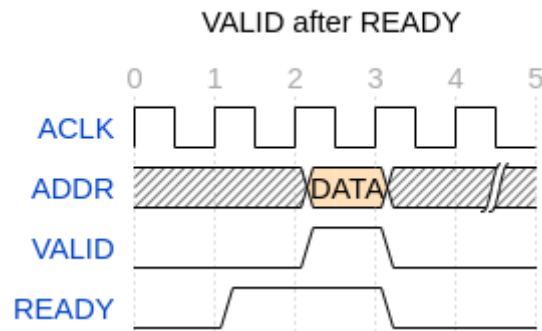


fig.3 VALID after READY signal

The destination is ready to accept the data. This assertion is recognized at T3 and source asserts **VALID** after T2 along with data. Both signals are sampled at T3 and transfer occurs. This transfer is a single cycle transfer.

- Valid with ready handshake

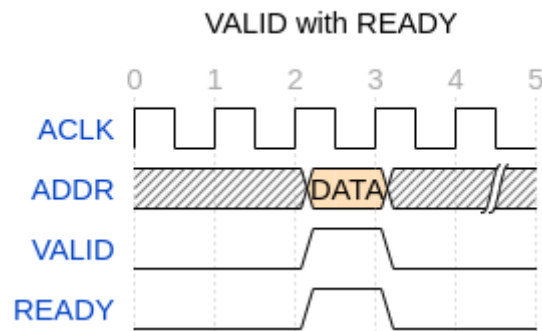


fig.4 VALID with READY signal

Both source and destination indicate they are ready to transfer the data, address or control after T2. This assertion is sampled at T3 which commences the transfer at T3 cycle.

- 1.2. 32-bit address for writing data
Address size is of 32-bit.

- 1.3. Support of 1 to 8 bytes of data in each data transfer.
 Size indicates maximum number of bytes in each data transfer.
 For write transactions size indicates how many data byte lanes are permitted to be active.
 The write strobes indicate which of those bytes are valid in each transfer.

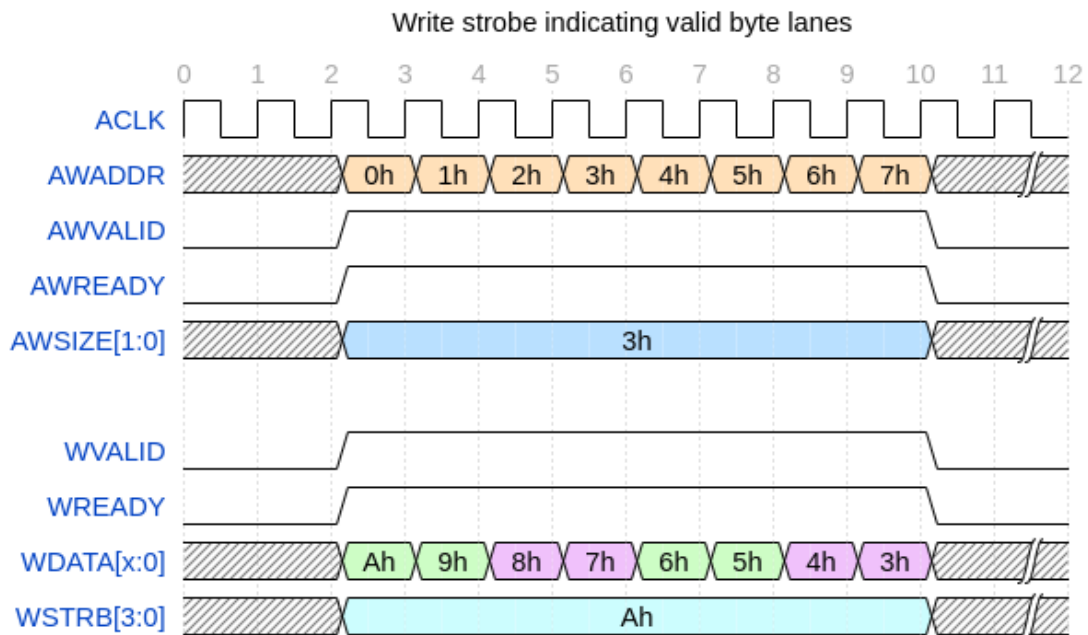


Fig.5. Write strobe indicating valid byte lanes

In the above diagram the address is varying and source and destination (write request channel) are ready to send and accept address. The **AWSIZE[1:0]** has value 3h which means that the valid transfer size is 4bytes. **AWSIZE[1:0]** denotes number of bytes in a transfer. Minimum value is 1 byte maximum value is 4 bytes.

Similarly in write data channel source and destination are ready to send and receive data. **WDATA[x:0]** has varying data. The **WSTRB[3:0]** indicates valid data byte lanes in the transfer. Value of **WSTRB[3:0]** is Ah which means that payload 1 and 2 are valid and rest are invalid.

* For this revision write data channel strobe is not included.

- 1.4. Support for fixed burst
 * For this revision fixed burst transfers are supported.
 Burst attribute describes how the address increments between transfers in a transaction.

Fixed burst is used for repeated access to same set of locations for example while loading or emptying a FIFO

Following points should be taken care of

- Same address for data or control transfer.
- The length of the burst can be up to 16 bytes.

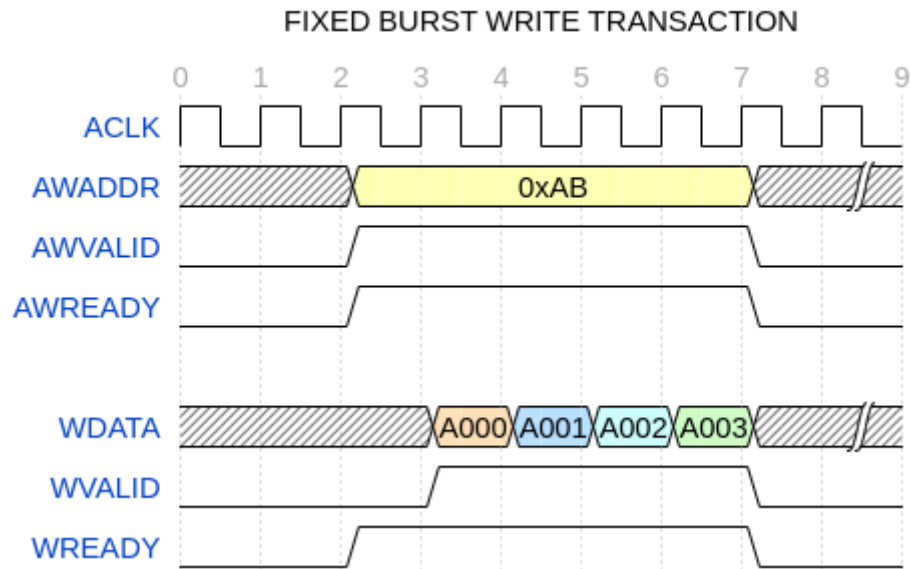


fig.6. Fixed Burst write transaction

Above diagram depicts fixed burst transaction with a fixed address of 0xABh. In write control channel the source is ready (**AWVALID** HIGH) with the address (0xABH) and destination is ready to accept data by asserting **AWREADY** HIGH.

Similarly in write data channel the destination is ready to accept data. The source commences transaction by pulling up the **WVALID** with **WDATA**.

This can be considered one fixed burst transaction type, many such combinations can also be considered depending upon source and destination.

4. Simulation/Synthesis diagram

* In this revision waveforms are not added. Will add in the future revisions