Design of AMBA Based AHB2APB Bridge

Project Report

Submitted by
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Industry Defined Project/Training

Under the guidance of
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AHB2APB Bridge:

The AHB to APB bridge is an AHB slave, providing an interface between the high speed AHB and the low-power APB.

Read and write transfers on the AHB are converted into equivalent transfers on the APB.

As the APB is not pipelined, then wait states are added during transfers to and from the APB where the AHB is required to wait for the APB.

Bridge Description:

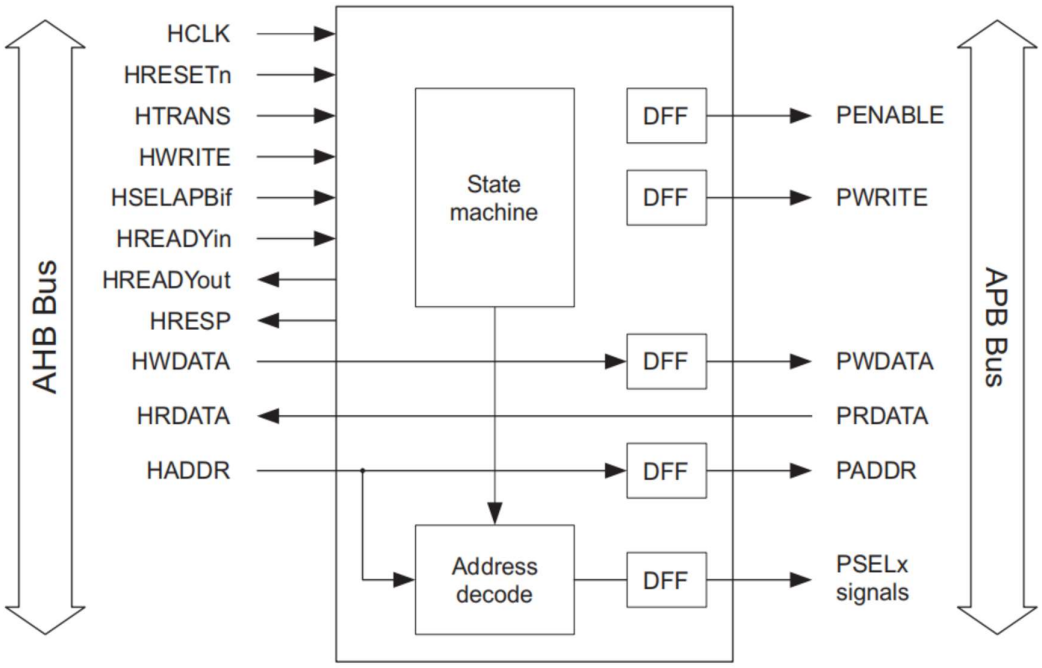


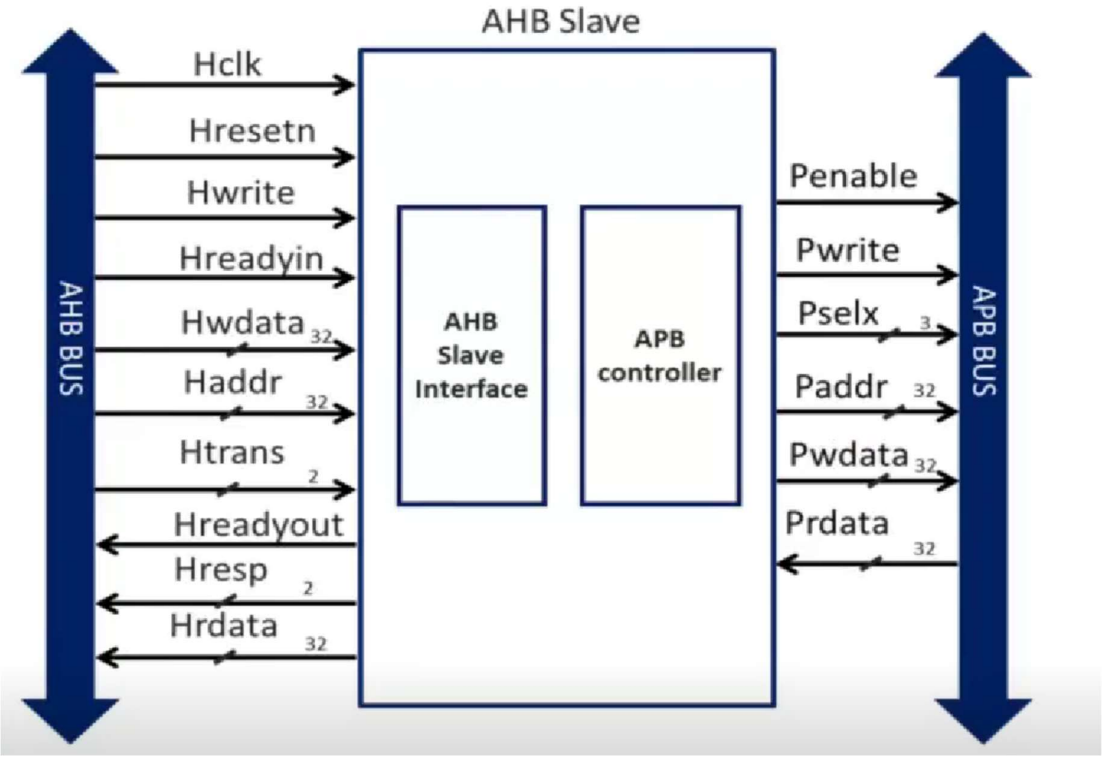
Fig.Block Diagram of AHB2APB Bridge

The main sections of this module are:
- AHB slave bus interface
- APB transfer state machine, which is independent of the device memory map
- APB output signal generation.

Bridge unit converts system bus transfers into APB transfers and performs the following functions:

- Latches the address and holds it valid throughout the transfer.
- Decodes the address and generates a peripheral select, PSELK. Only one select signal can be active during a transfer.
- Drives the data onto the APB for a write transfer.
- Drives the APB data onto the system bus for a read transfer.
- Generates a timing strobe, PENABLE, for the transfer.

Bock Diagram of AHB2APB Bridge:



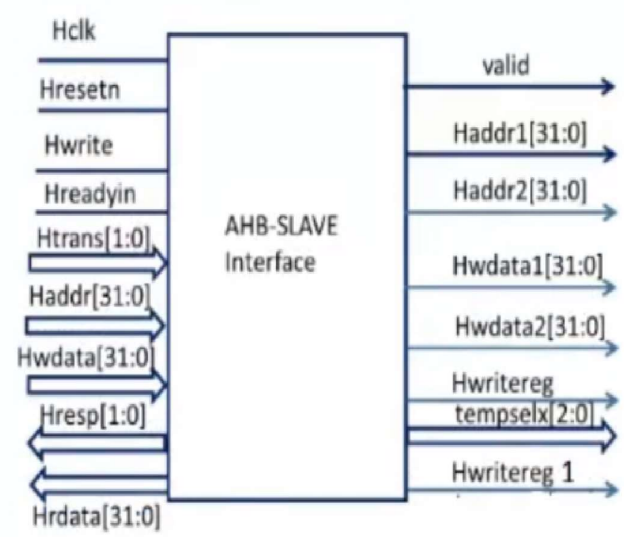
The AHB slave is composed of 2 individual units:

1. **AHB Slave Interface**
2. **APB Controller**

AHB Slave Interface:

It has some functionalities like:

- It does **pipelining** on the address data on the write signal.
- It generates a **'temp_selx'** signal which is used further by APB Controller to generate the **Pselx**.
- It generates one **'Hresp'** signal. when **Hresp=0** continuously, it means any transfer that happens with this bridge (AHB slave) is a successful transfer.
- It also generates **'valid'** signal to indicate a valid transfer happening. The signal will go to the APB controller.

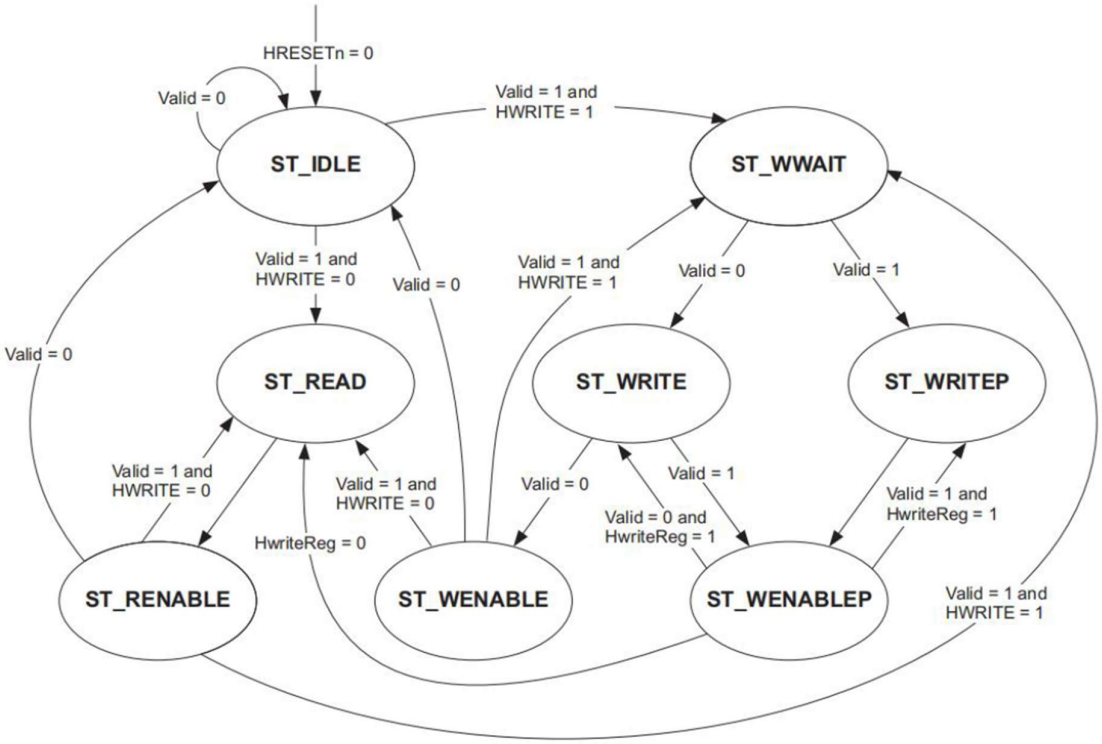


APB Controller:

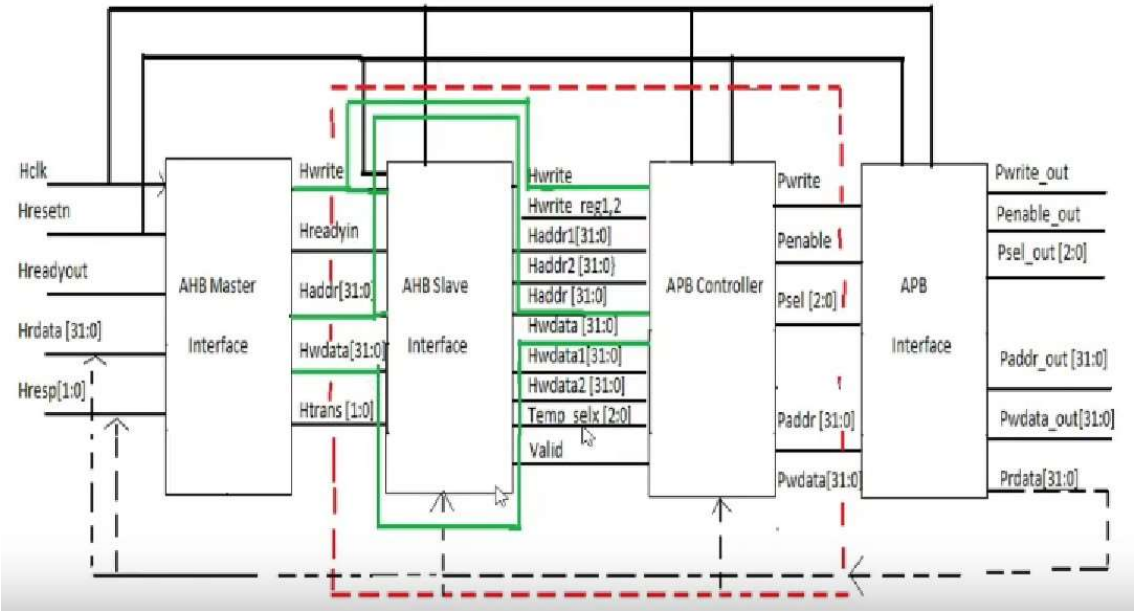
It's a FSM state diagram.

This controller basically controls the operation that converts the AHB to APB transfer.

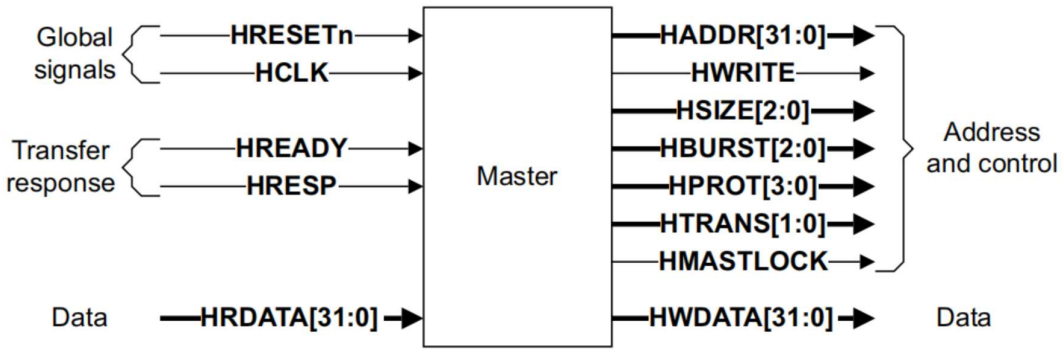
APB Controller State Diagram:



Detailed View of AHB2APB bridge:



AHB Master:



A master provides address and control information to initiate read and write operations.

The AHB module provides appropriate control signals, address, and data to the AHB2APB Bridge. Monitors the input data from the bridge so that an AHB master environment can be created.

This module also contains the HCLK generating block, which is distributed to module AHB2APB Bridge, and the RESET generation block, which is distributed to two other modules, AHB2APB Bridge and APB module, and these two signals are evidently used in this module as well.

APB Interface:

The APB module is the module that provides appropriate data to the AHB2APB Bridge and also monitors the control signals, address, and data received from the bridge in order to build the APB Slave environment. Depending on whether it is a write or a read operation, the control signals, address, and data received from the bridge are appropriately employed for the data transaction from bridge to this module or vice versa.

This module has a PCLK generation block that is distributed to the AHB2APB bridge module, and the PCLK generated is clearly utilised in this module as well.

Top Module:

Out of all the modules present, this module is simplest and also very prominent. All the signals are taken as wire to interconnect various modules present under this top module. In this module all the three modules namely:

- AHB Driver/Monitor
- AHB2APB bridge
- APB Driver/Monitor

These modules are all instantiated using Positional assignments which is again simple compared to naming assignment which is little tedious.

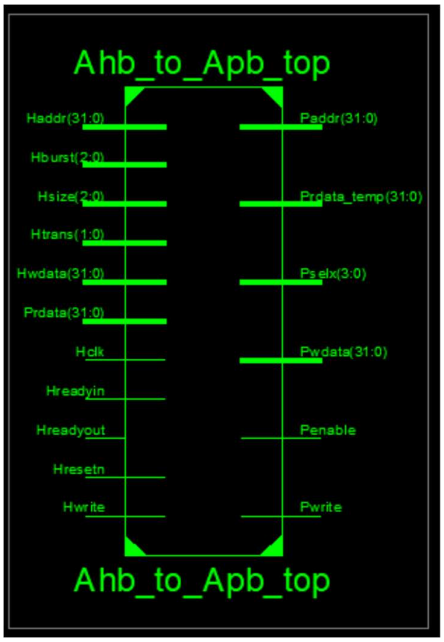


Fig. RTL Schematic of TOP Module

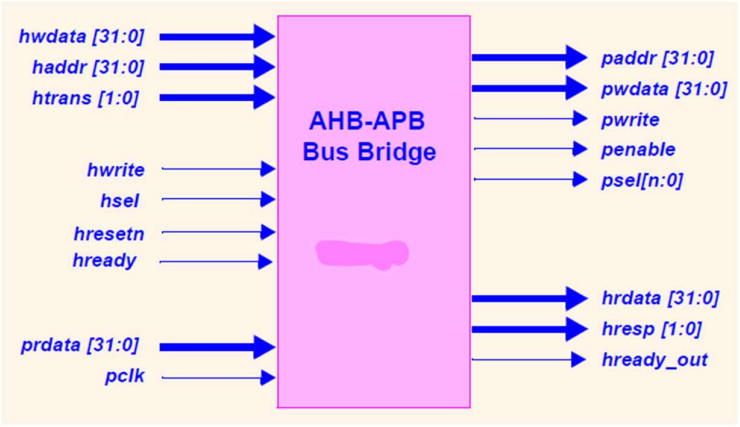


Fig. Block Diagram of TOP Module

Simulation results

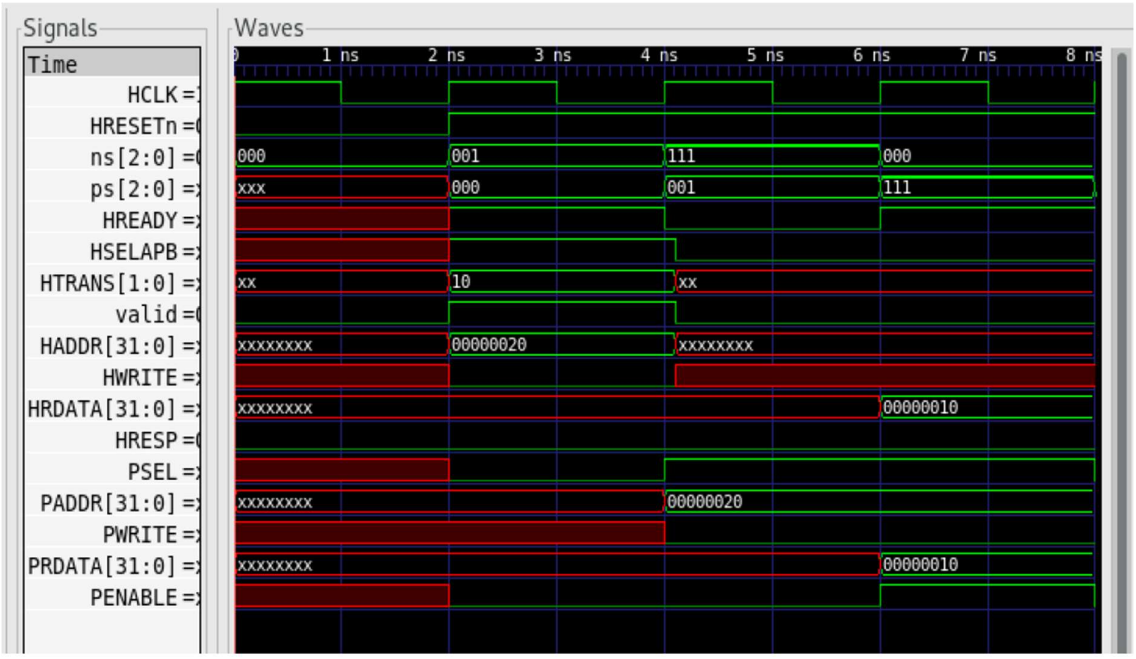


Figure: Single read transfer

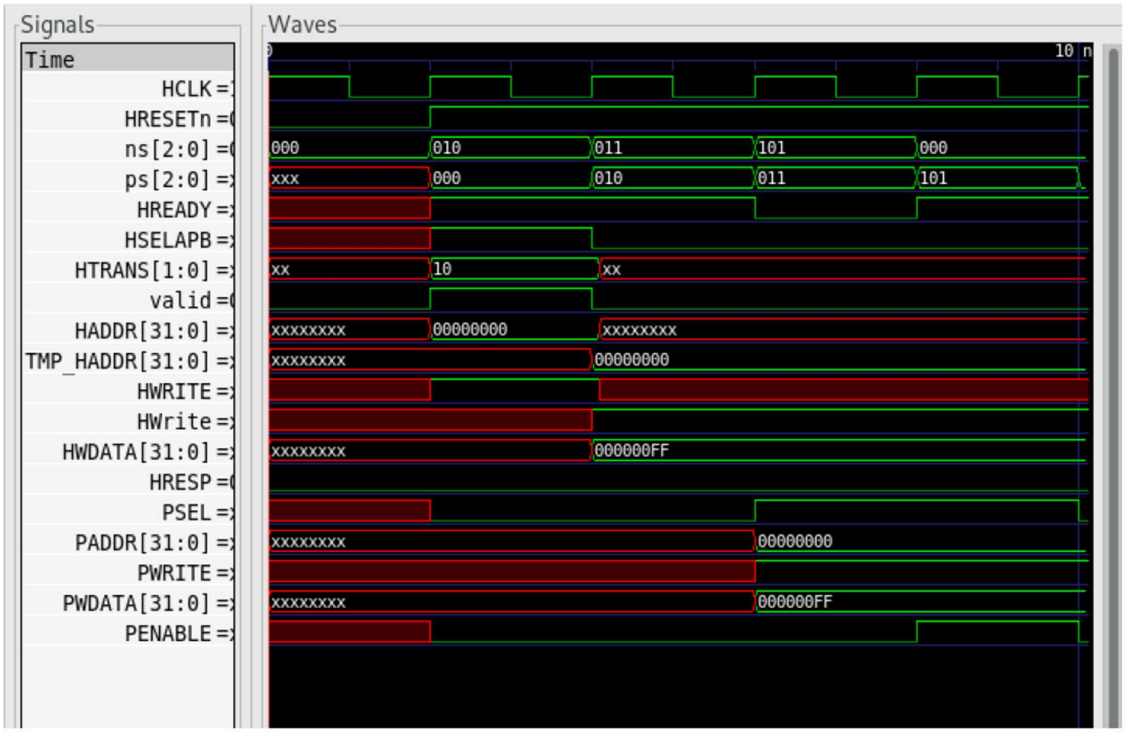


Figure: Single write transfer

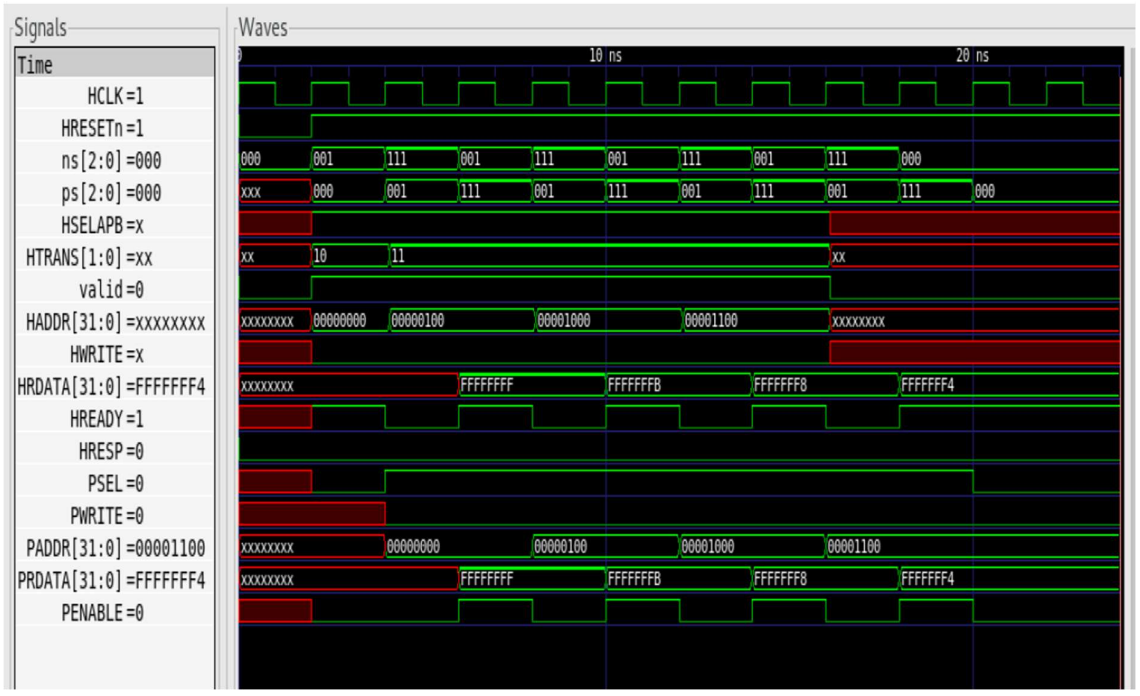


Figure: Burst read transfer

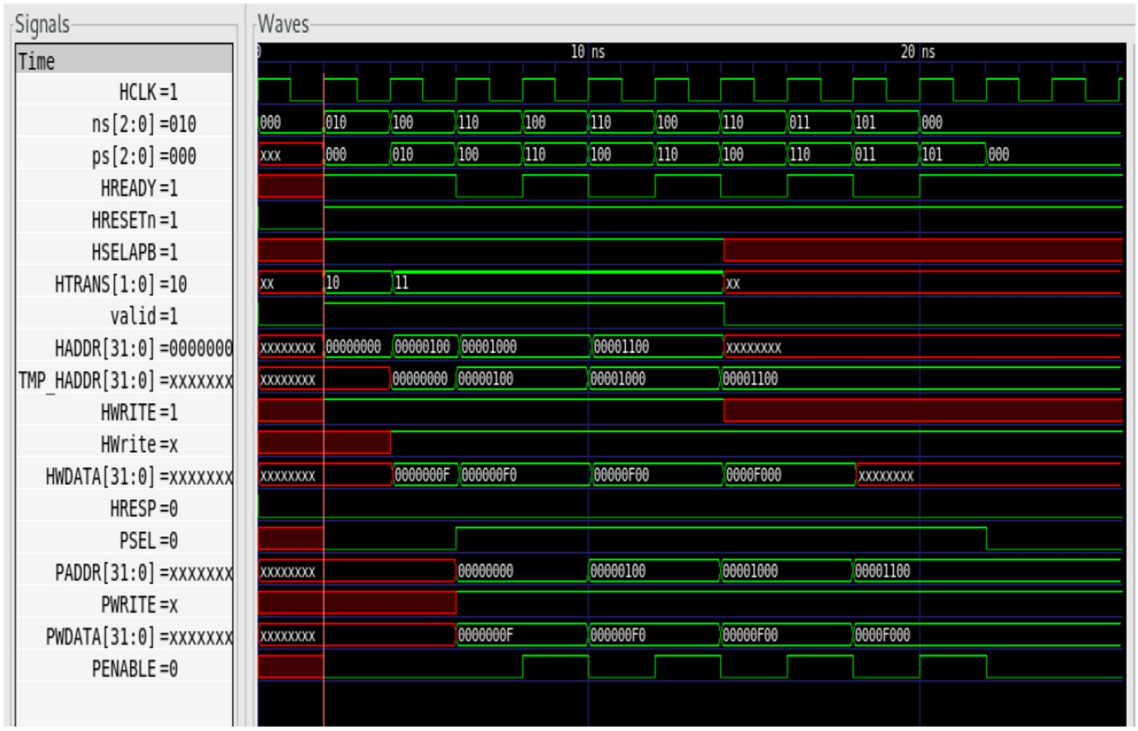


Figure: Burst write transfer

Conclusion:

The development of the synthesizable AHB to APB Bridge in Verilog HDL was done. The HCLK and PENABLE mechanism was implemented for making it the low-power consuming system. The functional verification of the bridge was done by driving various testcases to the design for testing the features. The multimaster and multislave AHB to APB bridge is one of the future scopes.