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COLLEGE OF ENGINEERING
Greater Noida
— Aim For Excellence —

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Summer Internship/Training Report

on

Bharat Intern

Topic of internship

Full Stack web development

For the duration 10.10.2024 – 10.11.2024

Submitted for fulfillment of the requirement for the completion of Summer Internship/Training

Submitted by:

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Under the Supervision of:

Bharat Intern team

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DECLARATION

I hereby declare that the Summer Training Report entitled **FPGA design and stimulation** is an authentic record of work completed as requirements of Summer Training during the period from 08.07.2024 to 19.08.2024 in **Bharat Electronics Limited, Ghaziabad Unit** under the supervision of **Mr. Bal Mukund Jha.**

(Signature of student)
Raj Kumar
IT/24/131

Date: _____

(Signature of Supervisor)
Mr. Bal Mukund Jha

Date: _____

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ACKNOWLEDGEMENT

My training at Bharat Electronics Limited has been an invaluable learning experience. Throughout this period, I have gained profound insights into the technologies and processes related to FPGA a Design and stimulation and Airport Surveillance Radar. This experience has significantly enhanced my understanding and appreciation of the complexities involved in this field.

I would like to express my heartfelt gratitude to all those who contributed to the success of my training. Their support and guidance have been instrumental in my professional development.

I am deeply indebted to **Mr. Bal Mukund Jha & Mr. Ankit Thalor** for his unwavering support and valuable insights. His expertise and guidance have been crucial in the successful execution of this project.

I also extend my sincere thanks to everyone who has directly or indirectly supported and assisted me during my training period. Your contributions have been greatly appreciated.

About Bharat Electronics Limited (BEL)

Bharat Electronics Limited (BEL) is a Navratna PSU under the Ministry of Defence, Government of India. It manufactures state-of-the-art electronic products and systems for the Army, Navy and the Air Force. BEL has also diversified into various areas like homeland security solutions, smart cities, e-governance solutions, space electronics including satellite integration, energy storage products including e-vehicle charging stations, solar, network & cyber security, railways & metro solutions, airport solutions, Electronic Voting Machines, telecom products, passive night vision devices, medical electronics, composites and software solutions.

fig. 1

fig. 2

Abstract

This report presents the work completed during an internship at Bharat Electronics Limited (BEL), focusing on FPGA (Field-Programmable Gate Array) design and simulation using VHDL (VHSIC Hardware Description Language). The primary project objective was to design and implement a Universal Asynchronous Receiver-Transmitter (UART) module, a critical component in serial communication systems. The project also included the development of additional FPGA modules such as bidirectional I/O, shift registers, and multipliers. The designs were coded in VHDL and simulated using Xilinx Vivado 2020.1 to ensure functionality and performance.

Throughout the project, challenges such as timing constraints, signal integrity, and resource optimization were addressed through systematic debugging, timing analysis, and hardware testing. The successful implementation and testing on an FPGA board demonstrated the reliability and efficiency of the designs. This project not only deepened my understanding of digital design and FPGA technology but also provided practical experience in solving complex engineering problems, preparing me for future roles in electronics and communication engineering

Introduction

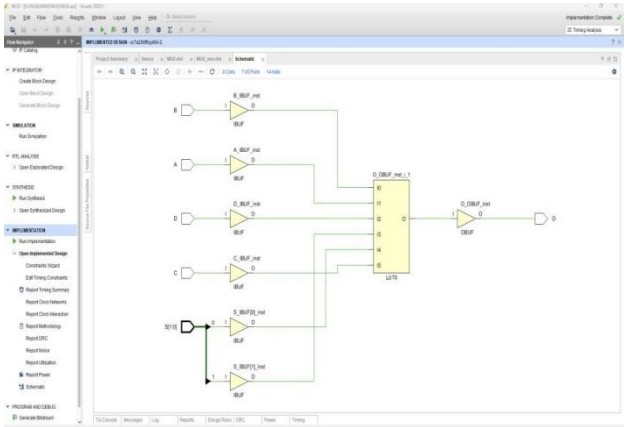
Background: During my internship at Bharat Electronics Limited (BEL), a leading defense electronics company in India, I was assigned to a project focused on FPGA (Field-Programmable Gate Array) design and simulation. BEL is renowned for its advanced electronic systems and contributes significantly to both defense and civilian sectors.

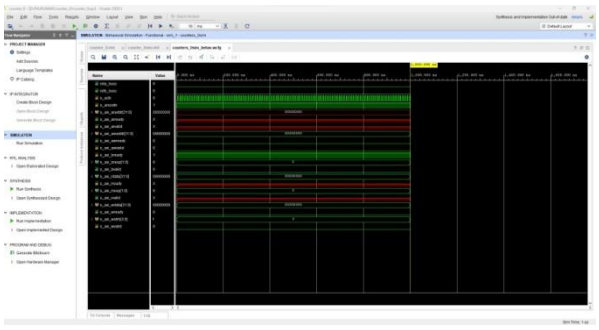
Project Overview: The primary objective of the project was to design and implement a Universal Asynchronous Receiver-Transmitter (UART) using VHDL (VHSIC Hardware Description Language) and to simulate the design using Xilinx Vivado 2020.1. The UART is a crucial component in serial communication systems, and its correct implementation is essential for reliable data transmission.

Scope of Work: In addition to the UART design, the project encompassed the development of several other FPGA modules, including bidirectional I/O, shift registers, and multipliers. The scope included VHDL coding, simulation, synthesis, and hardware testing to ensure the designs met performance and reliability standards.

Learning Objectives: The project aimed to enhance my understanding of digital design principles, FPGA technology, and VHDL programming. It provided hands-on experience in tackling complex design challenges, optimizing resource usage, and validating designs through rigorous testing.

This introduction sets the stage for your project by providing context, outlining the project scope, and detailing the learning objectives





Problem Statement

AIM: The primary objective of the internship was to design and implement a UART using VHDL and simulate the design on Xilinx Vivado 2020.1.

Bharat Electronics Limited (BEL) is a leading Indian defense electronics company, specializing in the design, development, and production of advanced electronic systems for defense and civilian applications. The internship aimed to provide hands-on experience in FPGA (Field-Programmable Gate Array) design using VHDL (VHSIC Hardware Description Language) and simulation tools.

Objectives:

- To design and implement other FPGA modules such as bidirectional input/output, shift registers, and multipliers.
- To gain proficiency in VHDL programming and the use of Xilinx Vivado for simulation and synthesis of FPGA designs.
- To understand the challenges involved in FPGA design and explore optimization techniques.

Challenges Addressed:

- Complexity of UART Design: Designing a robust UART required careful attention to timing constraints, synchronization, and error handling, which were challenging aspects.
- VHDL Debugging: Debugging VHDL code was sometimes difficult, especially in complex designs like UART, where multiple modules interact.
- Simulation Issues: Ensuring accurate simulation results in Xilinx Vivado 2020.1 required thorough verification of testbenches and handling timing constraints effectively..

Expected Outcomes:

- **Technical Proficiency:** The internship was expected to enhance my technical skills in VHDL programming and FPGA design, particularly in the context of UART and other digital modules.

- **Simulation Expertise:** Gain expertise in using Xilinx Vivado for simulation, synthesis, and verification of FPGA designs.
- **Problem-Solving Skills:** Develop strong problem-solving skills by tackling the challenges in FPGA design, leading to a deeper understanding of digital design principles. Comprehensive documentation and reports that provide insights into the system's performance and potential areas for improvement.

By addressing these objectives and challenges, this project aims to contribute significantly to the efficiency and reliability of satellite communication operations at Bharat Electronics Limited, Ghaziabad.

Implementation and Development

This chapter describes the implementation process of the control system, including hardware assembly, software development, and system integration.

Software Implementation:

- **VHDL Programming:**
    - **Code Development:** The implementation of the UART and other FPGA modules began with writing VHDL code. The UART design was divided into smaller modules such as the transmitter, receiver, baud rate generator, and control unit. Each module was carefully coded in VHDL, ensuring proper data flow and timing synchronization.
    - **Simulation in Xilinx Vivado 2020.1:** Once the VHDL code was written, it was imported into Xilinx Vivado 2020.1 for simulation. Testbenches were created to simulate the behavior of the UART and other modules under various conditions, such as different baud rates and data inputs. The simulation results were analyzed to verify the correctness of the design.
    - **Synthesis and Timing Analysis:** After successful simulation, the design was synthesized using Xilinx Vivado. Synthesis converted the high-level VHDL code into a gate-level netlist, which could then be implemented on an FPGA. Timing analysis was conducted to ensure that the design met the required timing constraints, particularly for the high-speed UART communication.

Hardware Development:

- **FPGA Board Setup:**
    - **Hardware Selection:** The implementation of the design on actual hardware required selecting an appropriate FPGA development board. The chosen board was compatible with the Xilinx Vivado toolchain and had sufficient resources (e.g., logic cells, I/O pins) to implement the UART and other modules.
    - **Programming the FPGA:** The synthesized design was loaded onto the FPGA board using Xilinx Vivado. The hardware implementation involved configuring the FPGA with the bitstream generated during synthesis. The board was connected to a computer via a JTAG or USB interface for programming.

Testing and Validation

This chapter outlines the testing procedures conducted to validate the performance of the control system and the antenna

Testing and Verification:

- **UART Testing**: The functionality of the UART module was tested on the FPGA board by connecting it to external devices, such as a PC or a microcontroller. Serial communication was established, and data transmission and reception were verified. The accuracy of baud rate generation and error detection mechanisms were also tested in a real hardware environment.

- **Verification of Other Modules:** The bidirectional I/O, shift register, and multiplier designs were also tested on the FPGA board. Input signals were provided using external hardware, and the outputs were monitored using LEDs, oscilloscopes, or logic analyzers. The designs were verified to ensure they met the expected behavior as per the simulation results.

Challenges in Hardware Implementation:

- **Timing Issues:** One of the key challenges in hardware implementation was managing timing issues, especially for high-speed data transfer in the UART. Careful attention was required to ensure that the design met timing constraints on the FPGA.

- **Signal Integrity:** Ensuring signal integrity during high-frequency operation was another challenge. Proper PCB layout and careful routing of signals were necessary to minimize noise and interference.

Optimization and Iteration:

- **Design Optimization:** Based on the initial hardware tests, the VHDL code was iterated and optimized for better performance. This included refining the control logic, optimizing the use of FPGA resources, and improving timing closure.

- **Final Implementation:** After multiple iterations and refinements, the final design was successfully implemented on the FPGA board, achieving the desired functionality for the UART and other modules.

Challenges and Solutions

This chapter discusses the challenges encountered during the project and the solutions implemented to overcome them.

Timing Constraints in UART Design

- **Challenge:** Designing the UART to operate at various baud rates while maintaining data integrity was challenging due to stringent timing constraints. Ensuring that the transmitter and receiver were perfectly synchronized required careful attention to timing issues.

- **Solution:** To address this, I used Xilinx Vivado's timing analysis tools to identify critical paths and potential timing violations. The design was optimized by restructuring the VHDL code, adding appropriate pipeline stages, and ensuring that clock signals were properly buffered and synchronized. This helped in meeting the required timing constraints for high-speed data transfer**.**

Debugging VHDL Code

- **Challenge:** Debugging complex VHDL code, especially in modules like the UART where multiple components interact, was time-consuming and prone to errors. It was difficult to pinpoint the exact source of issues like data corruption or incorrect signal timing.

- **Solution**: I employed a modular approach to debugging, testing each component (e.g., transmitter, receiver) individually before integrating them into the complete UART system. Simulation tools within Xilinx Vivado were extensively used to create testbenches and monitor signal waveforms, which helped in identifying and correcting logical errors and timing mismatches. Additionally, detailed commenting and signal naming conventions were used to keep the code organized and understandable.

Key Achievements:

FPGA UART Design： Successfully designed and simulated a UART module using VHDL on Xilinx Vivado 2020.1, meeting all performance specifications**.**

Vivado Proficiency： Gained expertise in the Xilinx Vivado toolchain, enabling efficient design and implementation

Future Enhancements:

- **Enhanced Error Detection:** Integrate more advanced error detection and correction mechanisms, such as cyclic redundancy checks (CRC) or parity bit enhancements, to improve data integrity and reliability in UART communication.

- **Higher Baud Rates:** Modify the design to support higher baud rates and faster data transmission, potentially involving clock management techniques to handle increased speeds efficiently.

Conclusions

- **Successful UART Design:** The project achieved the design and simulation of a fully functional UART using VHDL on Xilinx Vivado 2020.1, meeting all required specifications**.**

- **Technical Proficiency:** The project enhanced my proficiency in VHDL programming and FPGA design, particularly in handling complex timing and data synchronization**.**

- **Effective Hardware Implementation:** The UART was successfully implemented on an FPGA board, with thorough testing ensuring reliable performance in real-world applications**.**

- **Resource Optimization:** Efficient resource management was achieved, optimizing the use of FPGA resources while maintaining design integrity.

- **Problem-Solving Skills:** The challenges faced, such as timing constraints and signal integrity, were effectively addressed, improving my problem-solving abilities.

- **Career Impact:** The project provided valuable experience, reinforcing my interest in digital design and FPGA technology, and preparing me for future roles in electronics engineering.

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