Simulink Design Verifier Report

WDGBrakingLogic

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Simulink Design Verifier Report: WDGBrakingLogic

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Chapter 1. Summary

Analysis Information.

Model:	WDGBrakingLogic
Release:	R2022a Prerelease
Checksum:	3577721506 719747852 3275326579 2347090401
Mode:	Design error detection
Model Representation:	Built on 22-Sep-2021 19:05:11
Status:	Completed normally
PreProcessing Time:	10s
Analysis Time:	16s

Objectives Status.

Number of Objectives:	**48**	
Objectives Valid:	1	(2%)
Dead Logic:	0	(0%)

Chapter 2. Analysis Information

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Model Information

File:	WDGBrakingLogic
Version:	4.0
Time Stamp:	Wed Sep 22 18:13:35 2021
Author:	mabualqu

Analysis Options

Mode:	DesignErrorDetection
Rebuild Model Representation:	IfChangeIsDetected
Detect dead logic (partial):	on
Run exhaustive analysis for dead logic:	off
Detect integer overflow:	on
Detect division by zero:	on
Detect specified minimum and maximum value violations:	on
Detect out of bound array access:	on
Detect non-finite and NaN floating-point values:	off
Detect subnormal floating-point values:	off
Detect data store access violations:	off
Detect specified block input range violations:	off
Detect usage of remainder and reciprocal operations (hisl_0002):	off
Detect usage of square root operations (hisl_0003):	off
Detect usage of log and log10 operations (hisl_0004):	off

Detect usage of Reciprocal Square Root blocks (hisl_0028):	off
Maximum Analysis Time:	300s
Block Replacement:	off
Parameters Analysis:	off
Include expected output values:	off
Randomize data that do not affect the outcome:	off
Additional analysis to reduce instances of rational approximation:	on
Save Data:	on
Save Harness:	off
Save Report:	on

Constraints

Design Min Max Constraints

Name	Design Min Max Constraint
FCWtime	[0..40]
PB1time	[0..40]
PB2time	[0..40]
FBtime	[0..40]

Chapter 3. Dead Logic

Simulink Design Verifier proved these decisions and conditions to be unreachable or dead logic. This can be a side effect of parameter configurations or minimum and maximum constraints specified on inputs. Simulink Design Verifier ran a partial check for dead logic. Consider enabling the 'Dead logic > Run exhaustive analysis' configuration option in order to perform an exhaustive analysis.

Chapter 4. Design Error Detection Objectives Status

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Objectives Valid

#	Type	Model Item	Description	Analysis Time (sec)
1	Design Range	BrakingLogic/ SFunction	Design Range: [0..9.8]	7

Chapter 5. Derived Ranges

Signal	Derived Ranges
BrakingLogic/ SFunction - Outport 2	[0..9.8]
Constant- Outport 1	0.1
RelationalOperator- Outport 1	[F..T]
decel- Outport 1	[0..9.8]
FCWtime- Outport 1	[0..40]
PB1time- Outport 1	[0..40]
PB2time- Outport 1	[0..40]
FBtime- Outport 1	[0..40]