Simulink Design Verifier Report

EstimateLaneCenter

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Simulink Design Verifier Report: EstimateLaneCenter

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Table of Contents

Chapter 1. Summary

Analysis Information.

Model:	EstimateLaneCenter
Release:	R2022a Prerelease
Checksum:	1687050490 2689641277 3534688094 1410458477
Mode:	Design error detection
Model Representation:	Built on 22-Sep-2021 19:04:14
Status:	Completed normally
PreProcessing Time:	10s
Analysis Time:	24s

Objectives Status.

Number of Objectives:	**19**	
Objectives Falsified with Counterexamples:	2	(11%)
Objectives Falsified - Needs Simulation:	2	(11%)
Dead Logic:	0	(0%)

Chapter 2. Analysis Information

Table of Contents

Model Information

File:	EstimateLaneCenter
Version:	4.0
Time Stamp:	Wed Sep 22 18:13:14 2021
Author:	mabualqu

Analysis Options

Mode:	DesignErrorDetection
Rebuild Model Representation:	IfChangeIsDetected
Detect dead logic (partial):	on
Run exhaustive analysis for dead logic:	off
Detect integer overflow:	on
Detect division by zero:	on
Detect specified minimum and maximum value violations:	on
Detect out of bound array access:	on
Detect non-finite and NaN floating-point values:	off
Detect subnormal floating-point values:	off
Detect data store access violations:	off
Detect specified block input range violations:	off
Detect usage of remainder and reciprocal operations (hisl_0002):	off
Detect usage of square root operations (hisl_0003):	off
Detect usage of log and log10 operations (hisl_0004):	off
Detect usage of Reciprocal Square Root blocks (hisl_0028):	off

Maximum Analysis Time:	300s
Block Replacement:	off
Parameters Analysis:	off
Include expected output values:	off
Randomize data that do not affect the outcome:	off
Additional analysis to reduce instances of rational approximation:	on
Save Data:	on
Save Harness:	off
Save Report:	on

Approximations

Simulink Design Verifier performed the following approximations during analysis. These can impact the precision of the results generated by Simulink Design Verifier. Please see the product documentation for further details.

#	**Type**	**Description**
1	Rational approximation	The model includes floating-point arithmetic. Simulink Design Verifier approximates floating-point arithmetic with rational number arithmetic. Specifying minimum and maximum values that mimic environmental constraints on root-level Inport blocks may reduce instances of rational approximation.

Chapter 3. Dead Logic

Simulink Design Verifier proved these decisions and conditions to be unreachable or dead logic. This can be a side effect of parameter configurations or minimum and maximum constraints specified on inputs. Simulink Design Verifier ran a partial check for dead logic. Consider enabling the 'Dead logic > Run exhaustive analysis' configuration option in order to perform an exhaustive analysis.

Chapter 4. Design Error Detection Objectives Status

Table of Contents

Objectives Falsified with Counterexamples

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
27	Division by zero	CenterFromLeft/Divide	Division by zero	22	2 [0]
38	Division by zero	CenterFromRight/Divide	Division by zero	20	1 [0]

Objectives Falsified - Needs Simulation

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
30	Division by zero	CenterFromLeft/Divide1	Division by zero	24	4 [0]
41	Division by zero	CenterFromRight/Divide1	Division by zero	22	3 [0]

Chapter 5. Derived Ranges

Signal	Derived Ranges
CenterFromLeftAndRight/Add- Outport 1	[-Inf..Inf]
CenterFromLeftAndRight/Add1- Outport 1	[-Inf..Inf]
CenterFromLeftAndRight/Add2- Outport 1	[-Inf..Inf]
CenterFromLeftAndRight/Add3- Outport 1	[-Inf..Inf]
CenterFromLeftAndRight/Gain- Outport 1	[-Inf..Inf]
CenterFromLeftAndRight/Gain1- Outport 1	[-Inf..Inf]
CenterFromLeftAndRight/Gain2- Outport 1	[-Inf..Inf]
CenterFromLeftAndRight/Gain3- Outport 1	[-Inf..Inf]
CenterFromLeft/Constant- Outport 1	1
CenterFromLeft/HalfLaneWidthEstimate- Outport 1	1.8
CenterFromLeft/HalfLaneWidthEstimate2- Outport 1	1.8
CenterFromLeft/Product- Outport 1	[-Inf..Inf]
CenterFromLeft/Subtract- Outport 1	[-Inf..Inf]
CenterFromLeft/Divide- Outport 1	{ [-Inf..Inf] NaN }
CenterFromLeft/Product1- Outport 1	[0..Inf]
CenterFromLeft/Divide1- Outport 1	{ [-Inf..Inf] NaN }
CenterFromLeft/Subtract1- Outport 1	[-Inf..3.4028e+38]
CenterFromRight/HalfLaneWidthEstimate- Outport 1	1.8
CenterFromRight/HalfLaneWidthEstimate2- Outport 1	1.8
CenterFromRight/Product- Outport 1	[-Inf..Inf]
CenterFromRight/Bias- Outport 1	[-Inf..Inf]
CenterFromRight/Divide- Outport 1	{ [-Inf..Inf] NaN }
CenterFromRight/Product1- Outport 1	[0..Inf]
CenterFromRight/Divide1- Outport 1	{ [-Inf..Inf] NaN }
CenterFromRight/Subtract1- Outport 1	[-3.4028e+38..Inf]

Chapter 6. Design Errors

Table of Contents

CenterFromLeft/Divide

Summary.

Model Item:	CenterFromLeft/Divide
Type:	Division by zero
Status:	Falsified

Test Case.

Time	**0**
Step	**1**
LaneDetections.Left.Curvature	0.55556
LaneDetections.Left.CurvatureDerivative	-
LaneDetections.Left.HeadingAngle	-
LaneDetections.Left.LateralOffset	-
LaneDetections.Left.Strength	1
LaneDetections.Right.Curvature	0
LaneDetections.Right.CurvatureDerivative	-
LaneDetections.Right.HeadingAngle	-
LaneDetections.Right.LateralOffset	-
LaneDetections.Right.Strength	0

CenterFromLeft/Divide1

Summary.

Model Item:	CenterFromLeft/Divide1
Type:	Division by zero
Status:	Falsified - needs simulation

Test Case.

Time	**0**
Step	**1**
LaneDetections.Left.Curvature	0.55556
LaneDetections.Left.CurvatureDerivative	0
LaneDetections.Left.HeadingAngle	0
LaneDetections.Left.LateralOffset	0
LaneDetections.Left.Strength	1.1755e-38
LaneDetections.Right.Curvature	0
LaneDetections.Right.CurvatureDerivative	0
LaneDetections.Right.HeadingAngle	0
LaneDetections.Right.LateralOffset	0
LaneDetections.Right.Strength	-1.1755e-38

CenterFromRight/Divide

Summary.

Model Item:	CenterFromRight/Divide
Type:	Division by zero
Status:	Falsified

Test Case.

Time	**0**
Step	**1**
LaneDetections.Left.Curvature	0.55556
LaneDetections.Left.CurvatureDerivative	-
LaneDetections.Left.HeadingAngle	-
LaneDetections.Left.LateralOffset	-
LaneDetections.Left.Strength	0
LaneDetections.Right.Curvature	-0.55556
LaneDetections.Right.CurvatureDerivative	-
LaneDetections.Right.HeadingAngle	-
LaneDetections.Right.LateralOffset	-
LaneDetections.Right.Strength	1

CenterFromRight/Divide1

Summary.

Model Item:	CenterFromRight/Divide1
Type:	Division by zero

Status: Falsified - needs simulation

Test Case.

Time	**0**
Step	**1**
LaneDetections.Left.Curvature	0
LaneDetections.Left.CurvatureDerivative	0
LaneDetections.Left.HeadingAngle	0
LaneDetections.Left.LateralOffset	0
LaneDetections.Left.Strength	-1.1755e-38
LaneDetections.Right.Curvature	-0.55556
LaneDetections.Right.CurvatureDerivative	0
LaneDetections.Right.HeadingAngle	0
LaneDetections.Right.LateralOffset	0
LaneDetections.Right.Strength	1.1755e-38