Report Generated by Test Manager

Title: **WDGBrakingLogic Low-Level Tests**
Author:
Date: **22-Sep-2021 19:19:58**

Test Environment

Platform: PCWIN64
MATLAB: (R2022a)

Summary

Name	Outcome	Duration (Seconds)
Results: 2021-Sep-22 19:16:50	53 ✔	102.52
WDGBrakingLogic_SLDV_Based_Test	53 ✔	102.52
SLDV-Based Test	53 ✔	102.519
LLR_SLDV	53 ✔	102.519
Test Case:1	✔	3.795
Test Case:2	✔	1.887
Test Case:3	✔	1.852
Test Case:4	✔	1.887
Test Case:5	✔	1.931
Test Case:6	✔	1.758
Test Case:7	✔	1.893
Test Case:8	✔	1.73
Test Case:9	✔	1.743
Test Case:10	✔	1.861
Test Case:11	✔	1.942
Test Case:12	✔	1.841
Test Case:13	✔	1.827
Test Case:14	✔	1.736
Test Case:15	✔	1.871
Test Case:16	✔	1.852
Test Case:17	✔	1.898
Test Case:18	✔	1.853
Test Case:19	✔	1.9
Test Case:20	✔	1.768
Test Case:21	✔	1.864

Test Case:22	1.745
Test Case:23	1.863
Test Case:24	1.855
Test Case:25	1.864
Test Case:26	1.801
Test Case:27	1.865
Test Case:28	1.943
Test Case:29	1.832
Test Case:30	1.91
Test Case:31	1.95
Test Case:32	1.874
Test Case:33	1.849
Test Case:34	1.857
Test Case:35	1.952
Test Case:36	1.862
Test Case:37	1.871
Test Case:38	1.787
Test Case:39	1.857
Test Case:40	1.879
Test Case:41	1.868
Test Case:42	1.885
Test Case:43	1.887
Test Case:44	1.927
Test Case:45	1.835
Test Case:46	1.897
Test Case:47	1.909
Test Case:48	1.848

Test Case:49	✓	1.843
Test Case:50	✓	1.771
Test Case:51	✓	1.806
Test Case:52	✓	1.843
Test Case:53	✓	1.588

Results: 2021-Sep-22 19:16:50

Result Type: Result Set
Parent: None
Start Time: 22-Sep-2021 19:17:55
End Time: 22-Sep-2021 19:19:37
Outcome: Total: 53, Passed: 53

Aggregated Coverage Results

Analyzed Model	Sim Mode	Complexity	Decision	Condition	MCDC	Execution	Relational Boundary
WDGBrakingLogic	Normal	21	91%	96%	91%	100%	100%

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WDGBrakingLogic_SLDV_Based_Test

Test Result Information

Result Type: Test File Result
Parent: Results: 2021-Sep-22 19:16:50
Start Time: 22-Sep-2021 19:17:55
End Time: 22-Sep-2021 19:19:37
Outcome: Total: 53, Passed: 53
Description:

Model Version: 4.0

Model Last Modified On: 22-Sep-2021 18:13:35

Checksum when Compiled as Referenced Model: 4047763966 1651424035 440184956 1533764249

Test Suite Information

Name: WDGBrakingLogic_SLDV_Based_Test

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SLDV-Based Test

Test Result Information

Result Type:	Test Suite Result
Parent:	WDGBrakingLogic_SLDV_Based_Test
Start Time:	22-Sep-2021 19:17:55
End Time:	22-Sep-2021 19:19:37
Outcome:	Total: 53, Passed: 53

Test Suite Information

Name:	SLDV-Based Test

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LLR_SLDV

Test Result Information

Result Type:	Test Case Result
Parent:	SLDV-Based Test
Start Time:	22-Sep-2021 19:17:55
End Time:	22-Sep-2021 19:19:37
Outcome:	Passed
Description:	

Simulation test for LLR from SLDV.

Test Case Information

Name:	LLR_SLDV
Type:	Baseline Test

Test Case:1

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:17:55

End Time: 22-Sep-2021 19:17:59
Outcome: Passed

Test Case Information

Name: Test Case:1
Type: Baseline Test
Baseline Name: TestCases_1.mat
Baseline File: C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_1.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:1
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_1.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

Model: WDGBrakingLogic
Harness: WDGBrakingLogic_Harness_SLDV

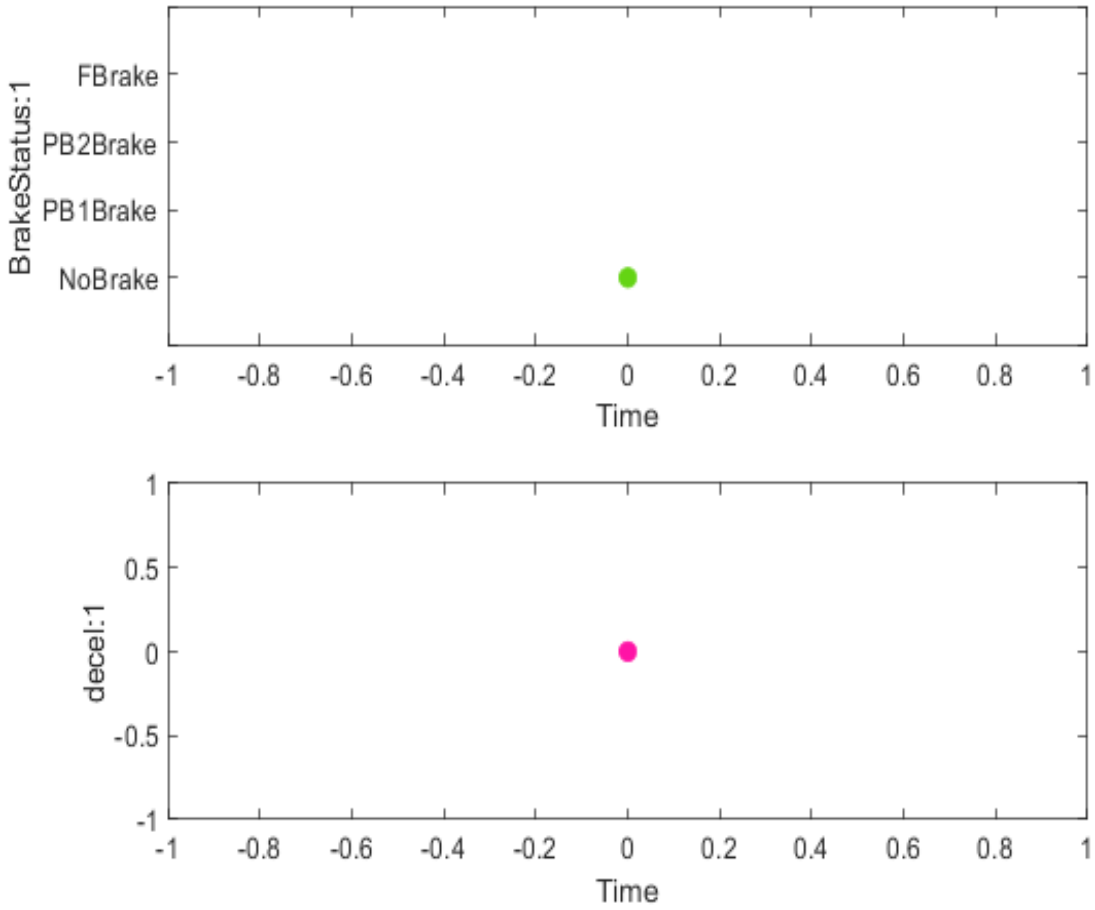
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:1
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:1
Start Time:	0
Stop Time:	0
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:17:55
Simulation Stop Time:	2021-09-22 19:17:57
Platform:	PCWIN64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union

decel:1	double	m/s^2	0.1	zoh	union



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Test Case:2

Test Result Information

Result Type: Test Iteration Result
Parent: LLR_SLDV

Start Time: 22-Sep-2021 19:17:59
End Time: 22-Sep-2021 19:18:01
Outcome: Passed

Test Case Information

Name: Test Case:2
Type: Baseline Test
Baseline Name: TestCases_2.mat
Baseline File: C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_2.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:2
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_2.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

Model: WDGBrakingLogic

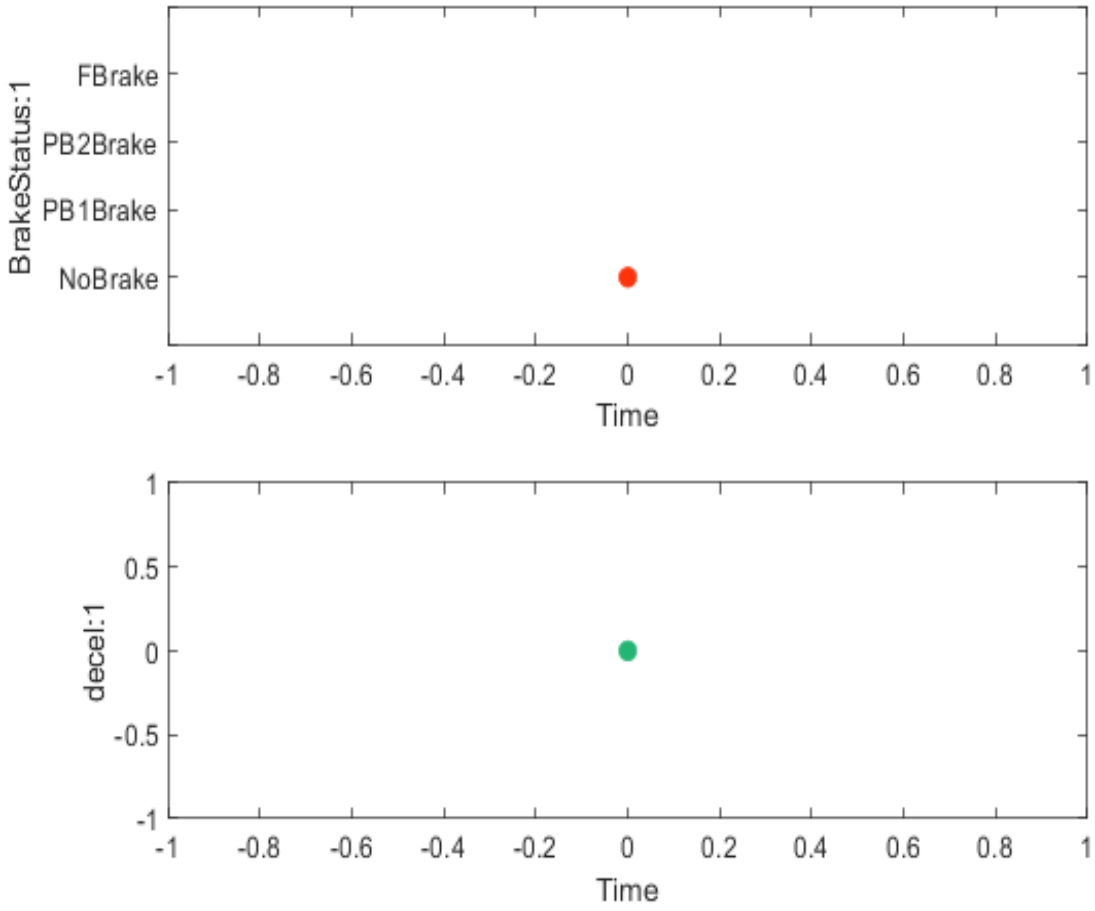
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:2
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:2
Start Time:	0
Stop Time:	0
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:17:59
Simulation Stop Time:	2021-09-22 19:17:59
Platform:	PCWIN64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync

BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union



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Test Case:3

Test Result Information

Result Type: Test Iteration Result

Parent: LLR_SLDV
Start Time: 22-Sep-2021 19:18:01
End Time: 22-Sep-2021 19:18:02
Outcome: Passed

Test Case Information

Name: Test Case:3
Type: Baseline Test
Baseline Name: TestCases_3.mat
Baseline File: C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_3.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:3
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_3.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

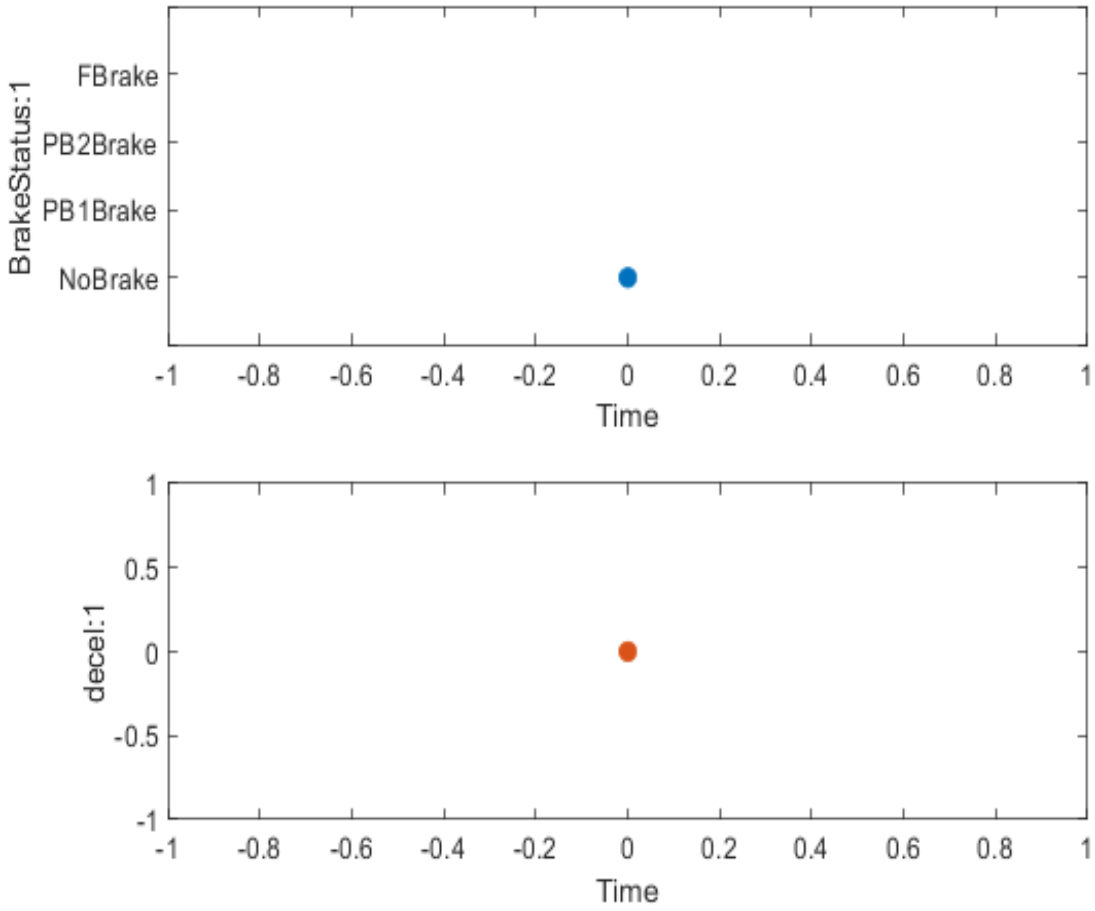
System Under Test Information

Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:3
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:3
Start Time:	0
Stop Time:	0
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:01
Simulation Stop Time:	2021-09-22 19:18:01
Platform:	PCWIN64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union



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Test Case:4

Test Result Information

Result Type: Test Iteration Result
Parent: LLR_SLDV
Start Time: 22-Sep-2021 19:18:03
End Time: 22-Sep-2021 19:18:04
Outcome: Passed

Test Case Information

Name: Test Case:4
Type: Baseline Test
Baseline Name: TestCases_4.mat
Baseline File: C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_4.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:4
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_4.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

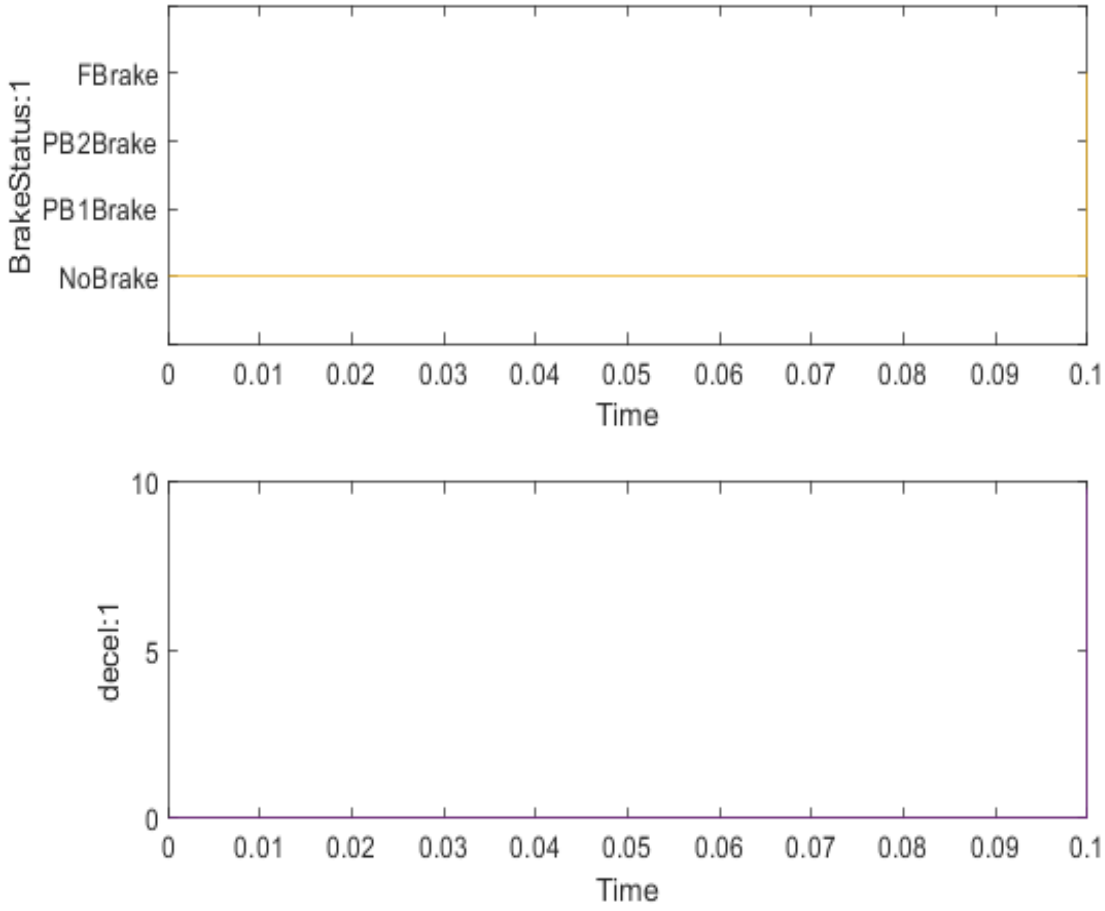
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:4
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:4
Start Time:	0
Stop Time:	0.10000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:03
Simulation Stop Time:	2021-09-22 19:18:03
Platform:	PCWIN64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
BrakeStatus:1	BrStatus		0.1	zoh	union	Link

decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union



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Test Case:5

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:04
End Time:	22-Sep-2021 19:18:06
Outcome:	Passed

Test Case Information

Name:	Test Case:5
Type:	Baseline Test
Baseline Name:	TestCases_5.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_5.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:5
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_5.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

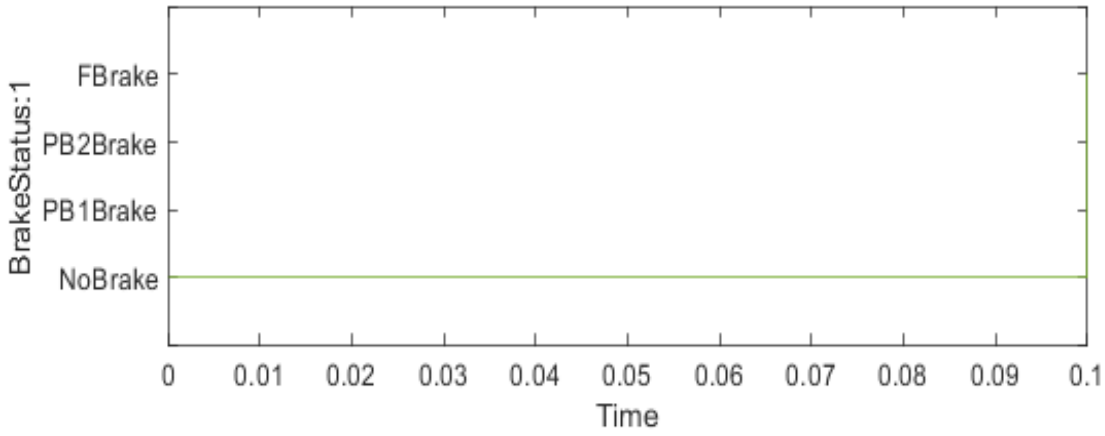
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:5
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:5
Start Time:	0
Stop Time:	0.10000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:05
Simulation Stop Time:	2021-09-22 19:18:05
Platform:	PCWIN64

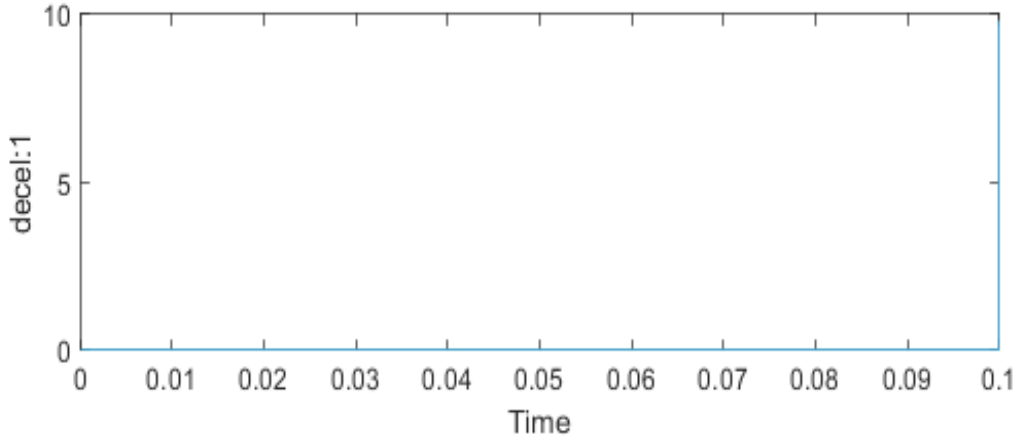
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:6

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:06
End Time:	22-Sep-2021 19:18:08
Outcome:	Passed

Test Case Information

Name:	Test Case:6
Type:	Baseline Test
Baseline Name:	TestCases_6.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_6.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:6
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_6.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

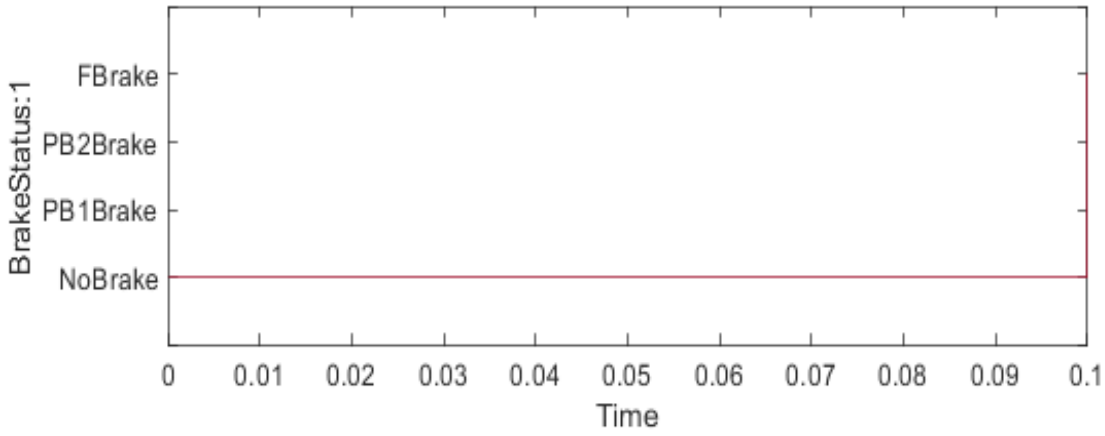
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:6
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:6
Start Time:	0
Stop Time:	0.10000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:07
Simulation Stop Time:	2021-09-22 19:18:07
Platform:	PCWIN64

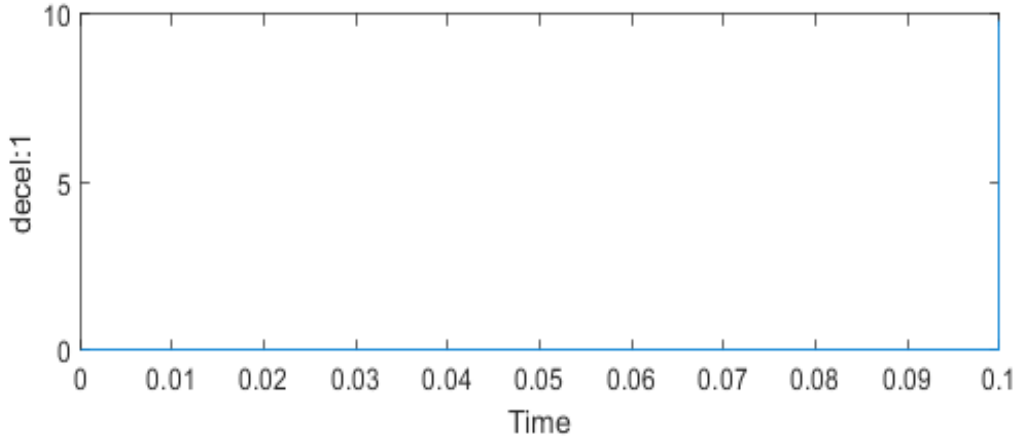
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:7

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:08
End Time:	22-Sep-2021 19:18:10
Outcome:	Passed

Test Case Information

Name:	Test Case:7
Type:	Baseline Test
Baseline Name:	TestCases_7.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_7.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:7
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_7.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

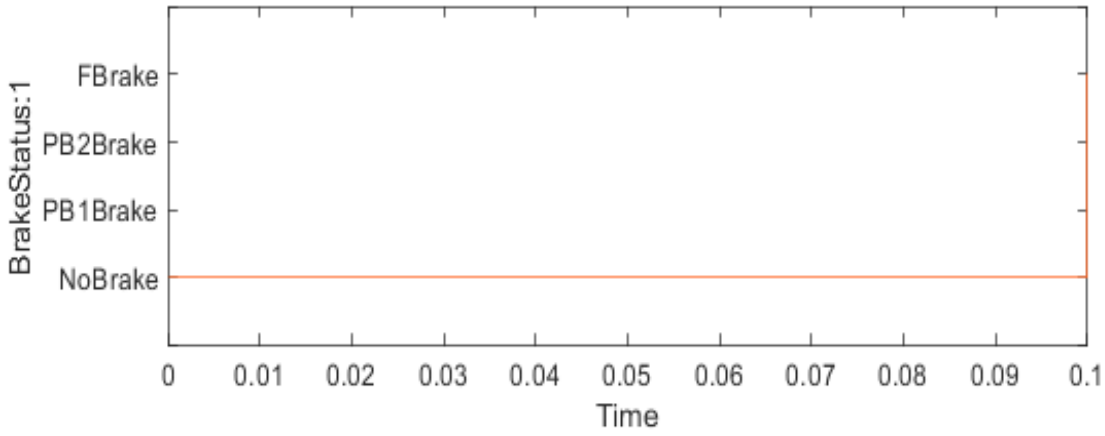
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:7
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:7
Start Time:	0
Stop Time:	0.10000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:08
Simulation Stop Time:	2021-09-22 19:18:09
Platform:	PCWIN64

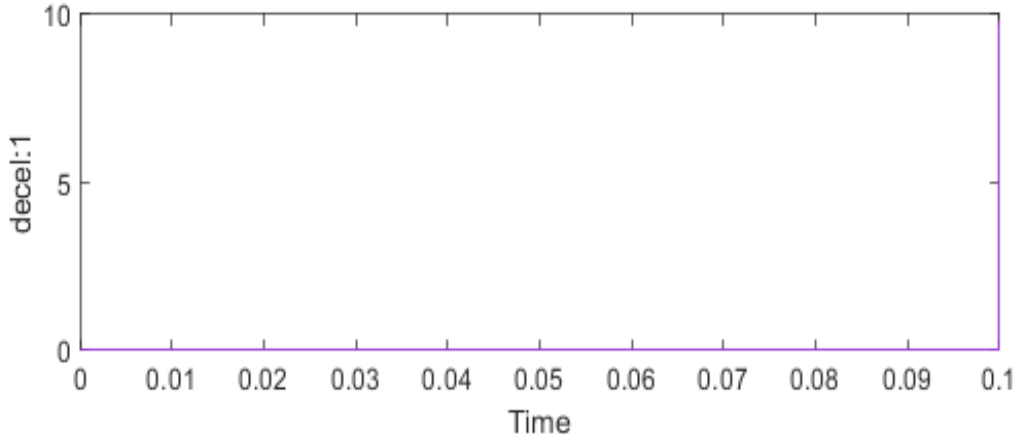
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:8

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:10
End Time:	22-Sep-2021 19:18:12
Outcome:	Passed

Test Case Information

Name:	Test Case:8
Type:	Baseline Test
Baseline Name:	TestCases_8.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_8.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:8
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_8.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

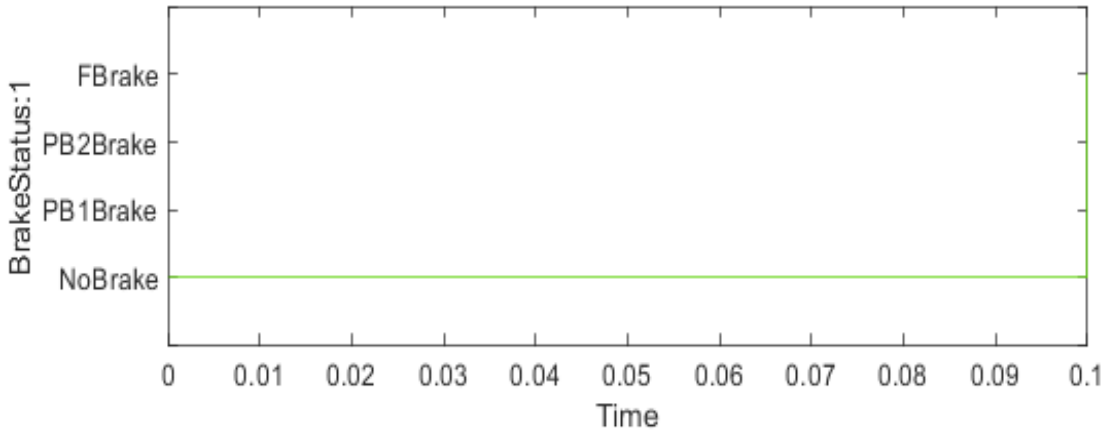
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:8
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:8
Start Time:	0
Stop Time:	0.10000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:10
Simulation Stop Time:	2021-09-22 19:18:10
Platform:	PCWIN64

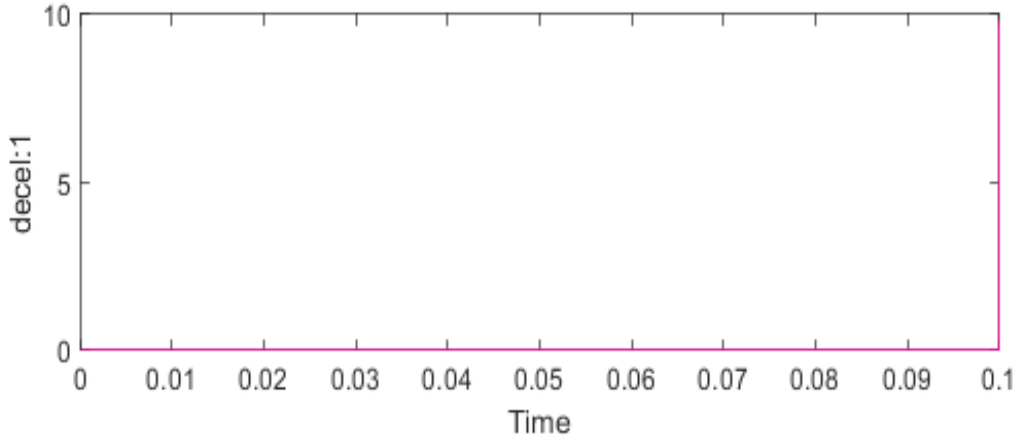
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:9

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:12
End Time:	22-Sep-2021 19:18:14
Outcome:	Passed

Test Case Information

Name:	Test Case:9
Type:	Baseline Test
Baseline Name:	TestCases_9.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_9.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:9
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_9.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

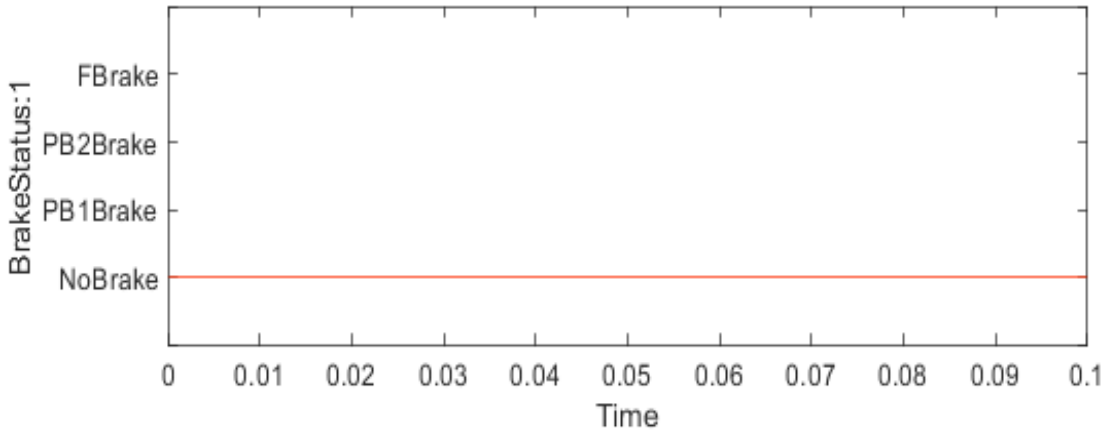
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:9
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:9
Start Time:	0
Stop Time:	0.10000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:12
Simulation Stop Time:	2021-09-22 19:18:12
Platform:	PCWIN64

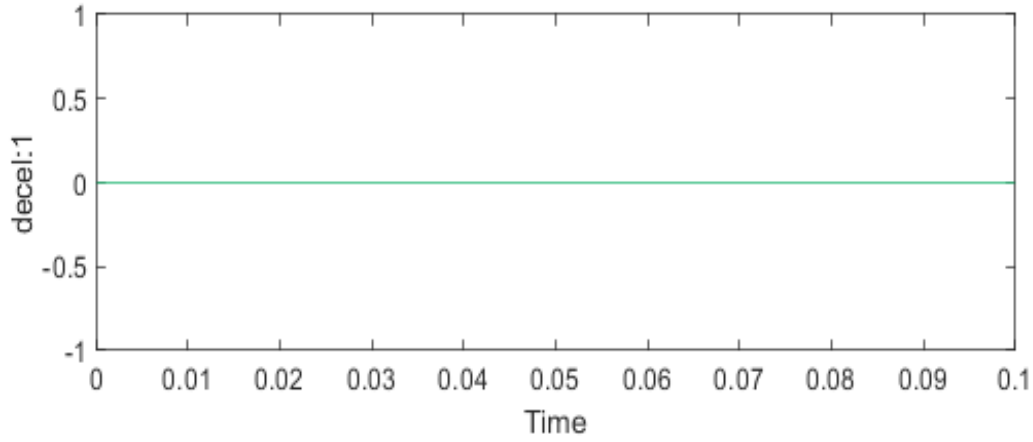
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:10

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:14
End Time:	22-Sep-2021 19:18:16
Outcome:	Passed

Test Case Information

Name:	Test Case:10
Type:	Baseline Test
Baseline Name:	TestCases_10.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_10.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:10
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_10.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

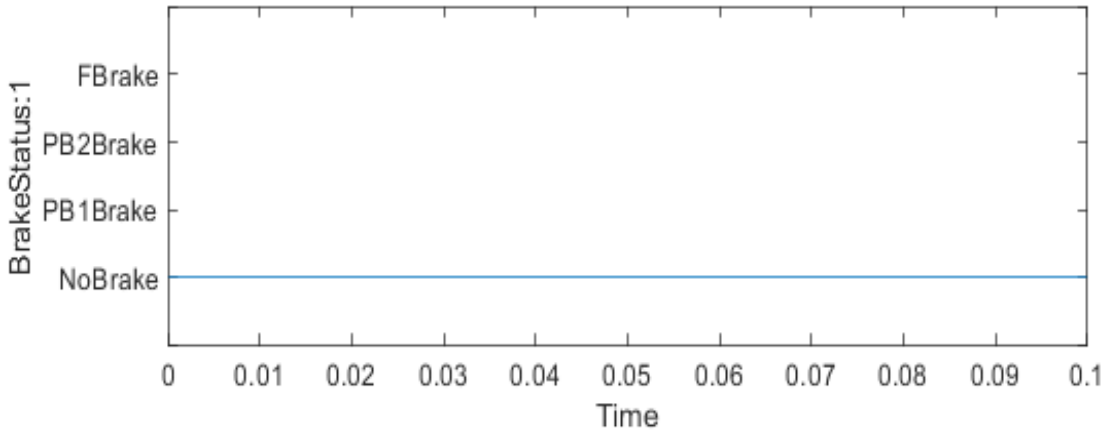
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:10
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:10
Start Time:	0
Stop Time:	0.10000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:14
Simulation Stop Time:	2021-09-22 19:18:14
Platform:	PCWIN64

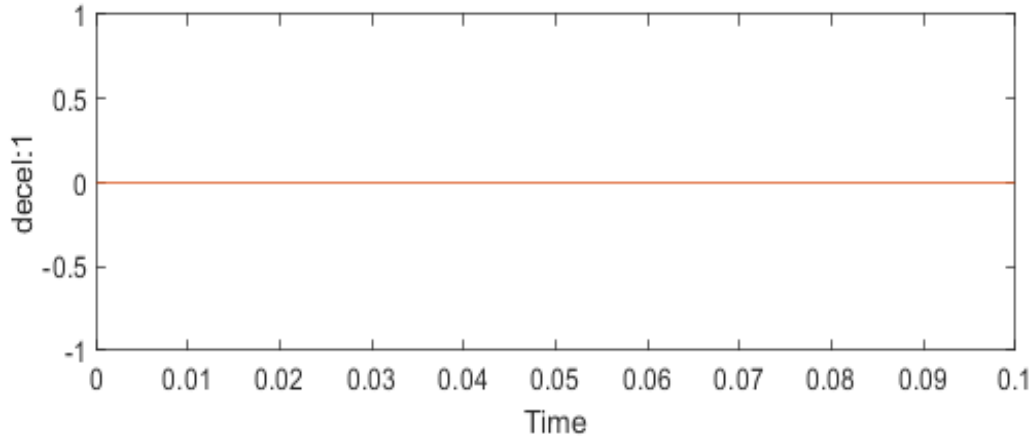
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:11

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:16
End Time:	22-Sep-2021 19:18:18
Outcome:	Passed

Test Case Information

Name:	Test Case:11
Type:	Baseline Test
Baseline Name:	TestCases_11.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_11.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:11
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_11.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

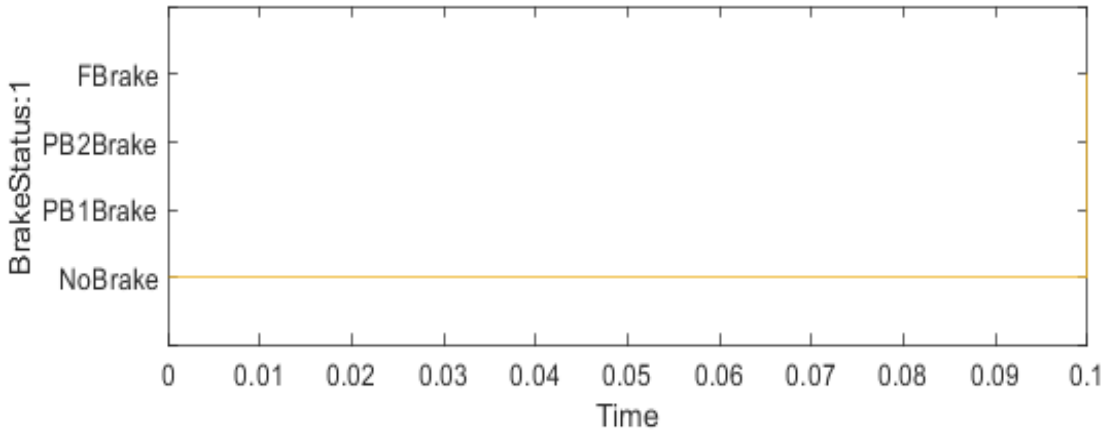
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:11
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:11
Start Time:	0
Stop Time:	0.10000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:16
Simulation Stop Time:	2021-09-22 19:18:16
Platform:	PCWIN64

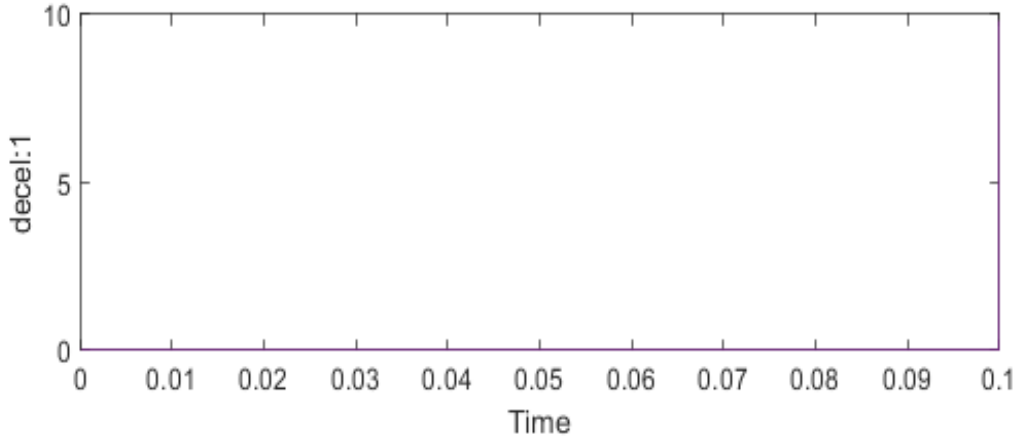
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:12

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:18
End Time:	22-Sep-2021 19:18:19
Outcome:	Passed

Test Case Information

Name:	Test Case:12
Type:	Baseline Test
Baseline Name:	TestCases_12.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_12.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:12
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_12.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

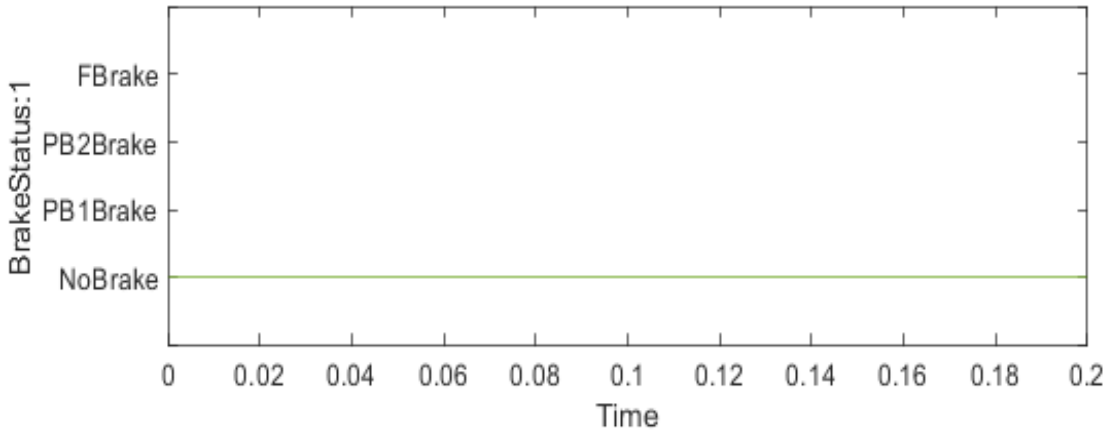
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:12
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:12
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:18
Simulation Stop Time:	2021-09-22 19:18:18
Platform:	PCWIN64

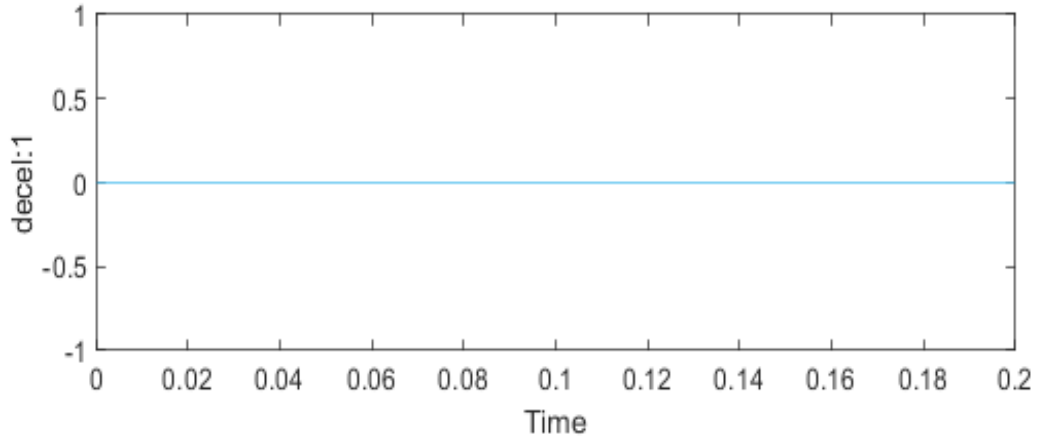
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:13

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:20
End Time:	22-Sep-2021 19:18:21
Outcome:	Passed

Test Case Information

Name:	Test Case:13
Type:	Baseline Test
Baseline Name:	TestCases_13.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_13.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:13
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_13.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

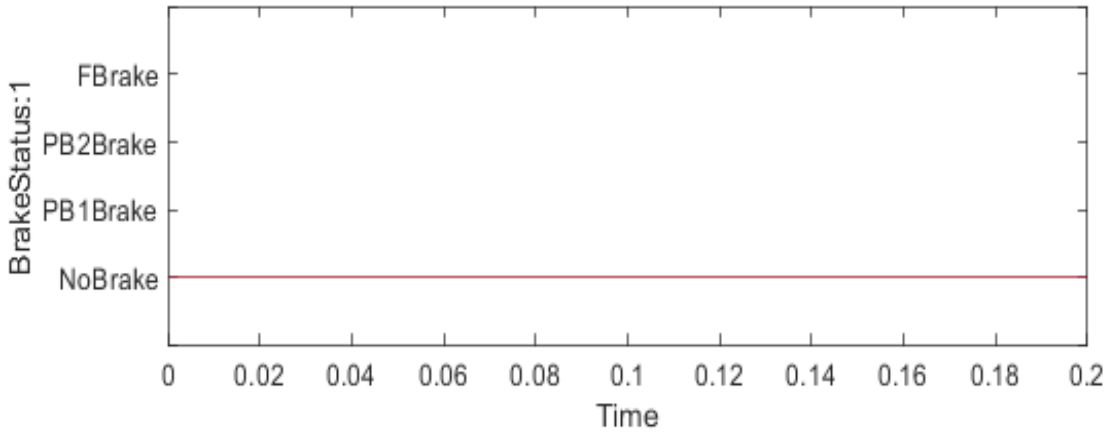
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:13
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:13
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:20
Simulation Stop Time:	2021-09-22 19:18:20
Platform:	PCWIN64

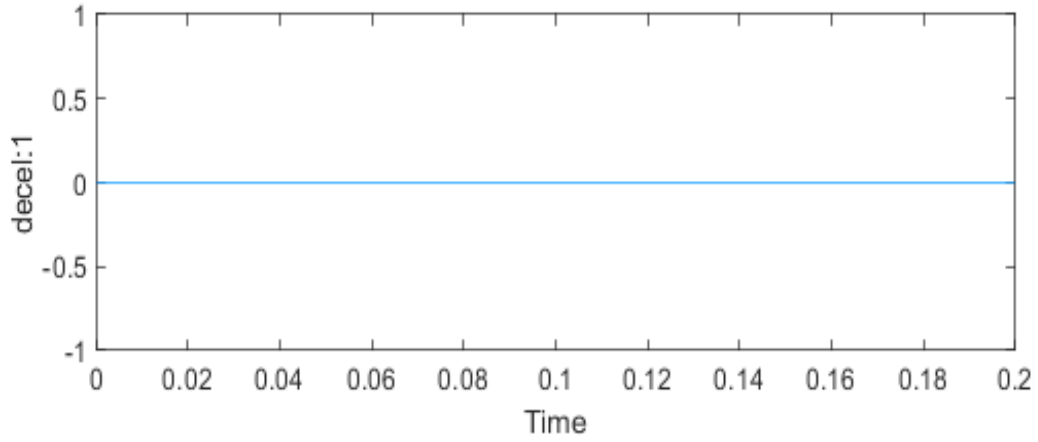
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:14

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:21
End Time:	22-Sep-2021 19:18:23
Outcome:	Passed

Test Case Information

Name:	Test Case:14
Type:	Baseline Test
Baseline Name:	TestCases_14.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_14.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:14
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_14.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

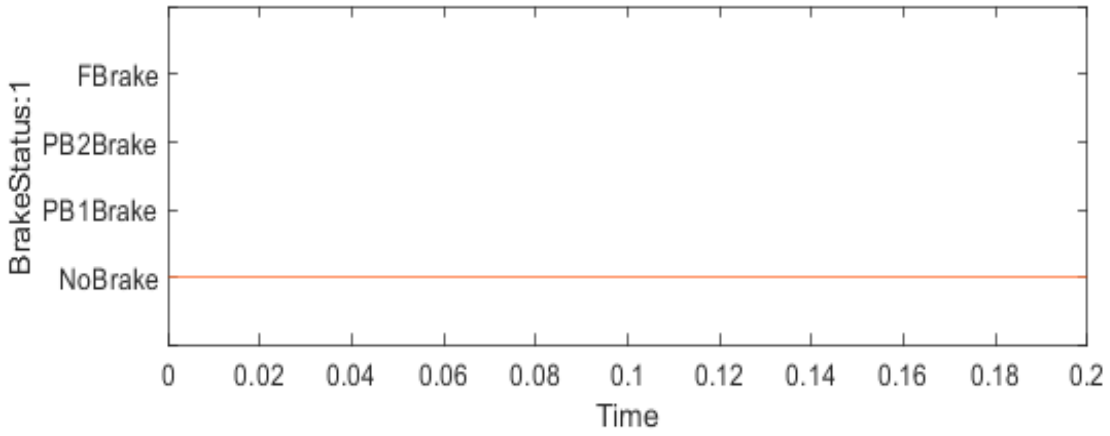
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:14
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:14
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:22
Simulation Stop Time:	2021-09-22 19:18:22
Platform:	PCWIN64

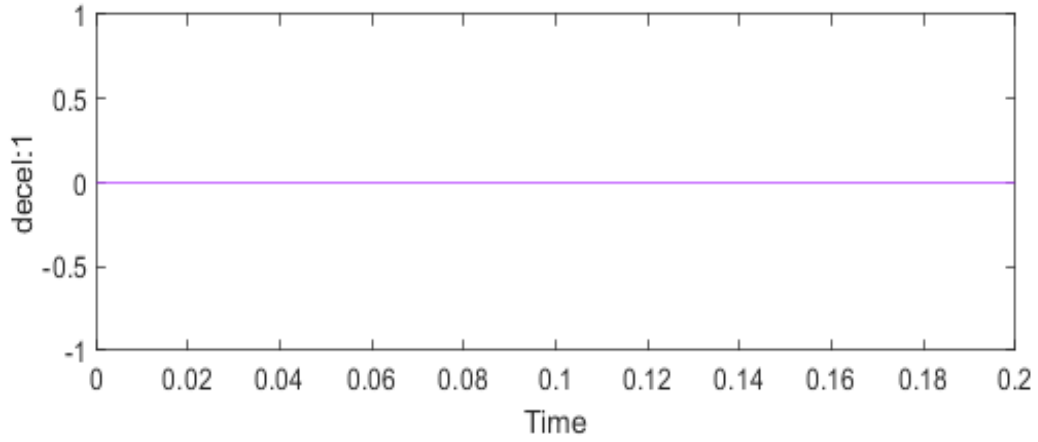
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:15

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:23
End Time:	22-Sep-2021 19:18:25
Outcome:	Passed

Test Case Information

Name:	Test Case:15
Type:	Baseline Test
Baseline Name:	TestCases_15.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_15.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:15
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_15.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

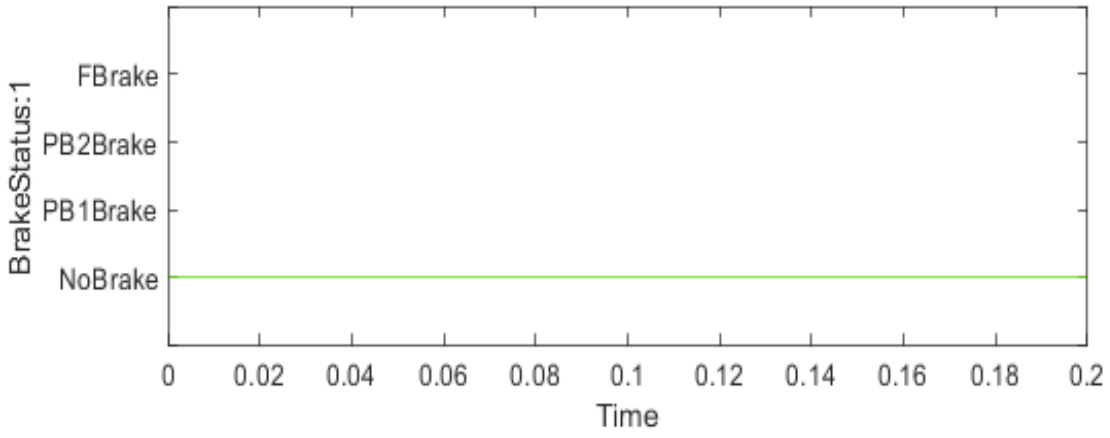
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:15
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:15
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:23
Simulation Stop Time:	2021-09-22 19:18:24
Platform:	PCWIN64

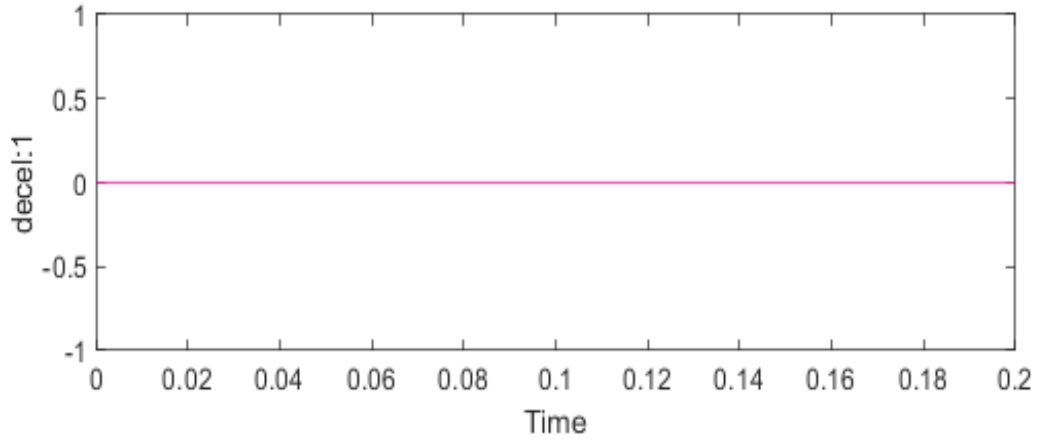
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:16

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:25
End Time:	22-Sep-2021 19:18:27
Outcome:	Passed

Test Case Information

Name:	Test Case:16
Type:	Baseline Test
Baseline Name:	TestCases_16.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_16.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:16
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_16.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

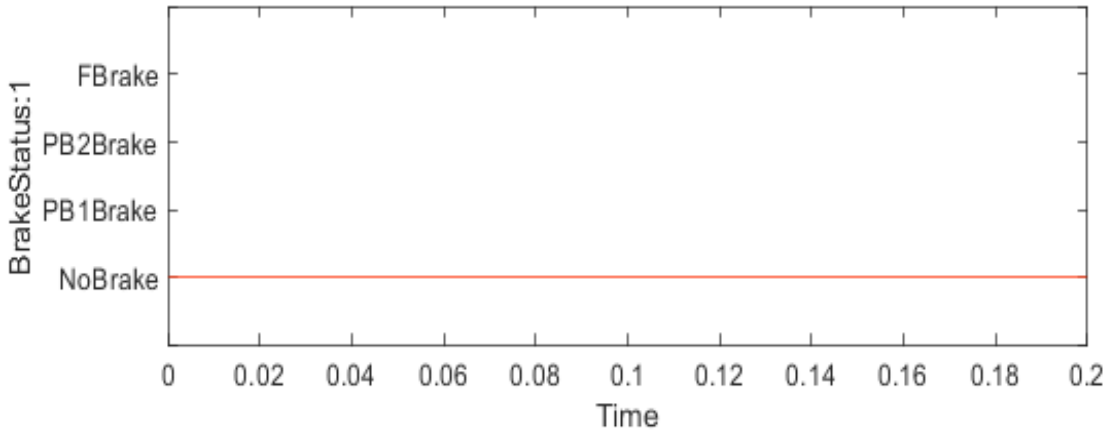
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:16
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:16
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:25
Simulation Stop Time:	2021-09-22 19:18:25
Platform:	PCWIN64

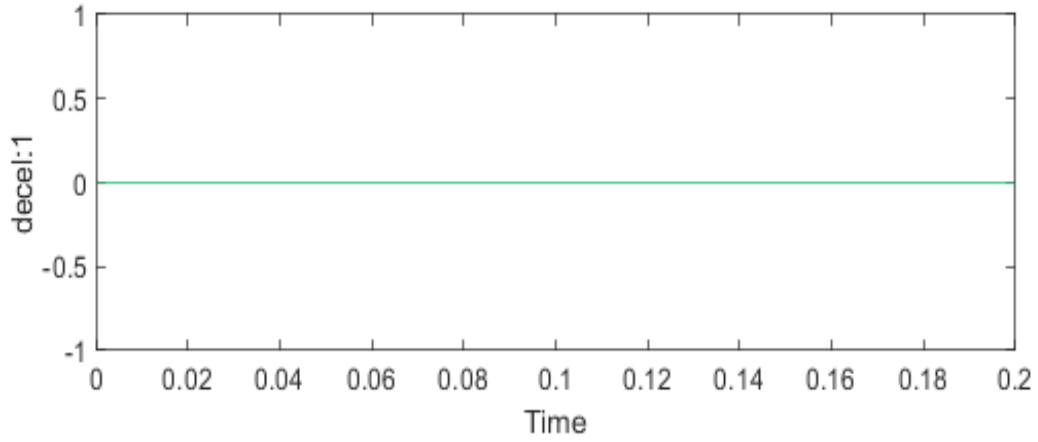
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:17

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:27
End Time:	22-Sep-2021 19:18:29
Outcome:	Passed

Test Case Information

Name:	Test Case:17
Type:	Baseline Test
Baseline Name:	TestCases_17.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_17.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:17
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_17.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

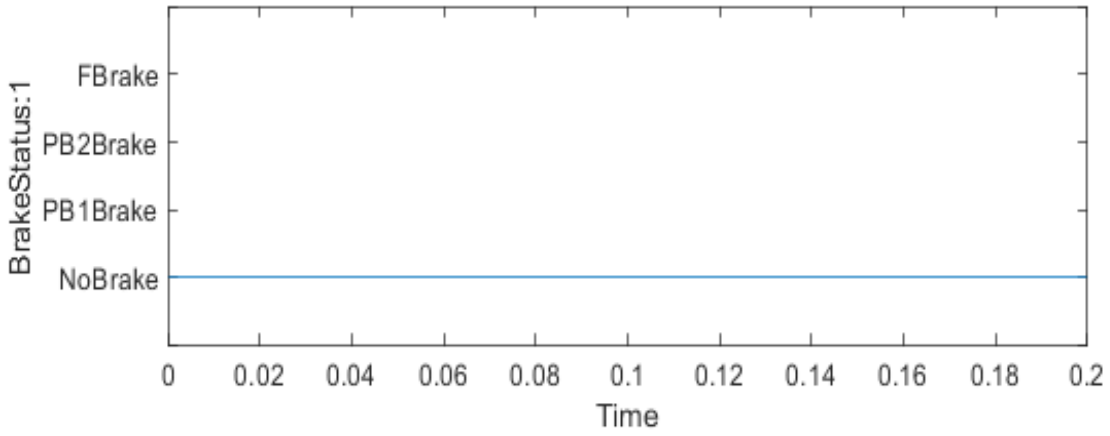
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:17
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:17
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:27
Simulation Stop Time:	2021-09-22 19:18:27
Platform:	PCWIN64

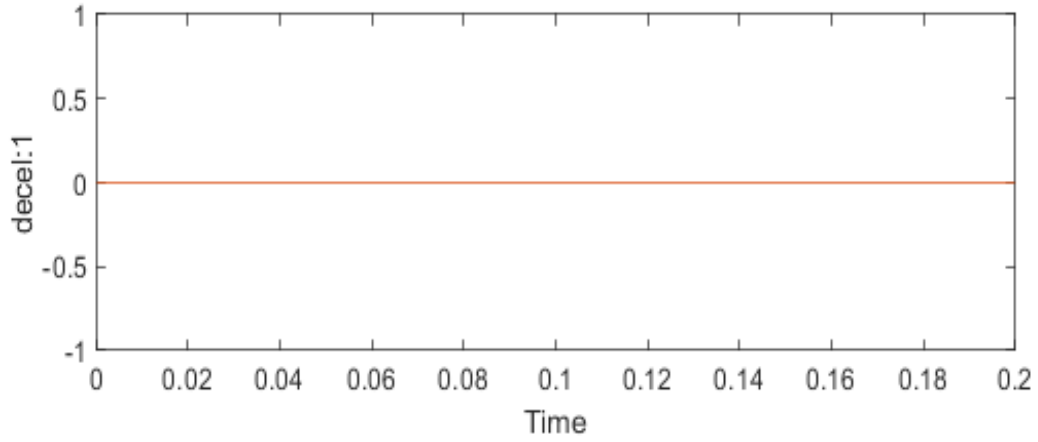
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:18

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:29
End Time:	22-Sep-2021 19:18:31
Outcome:	Passed

Test Case Information

Name:	Test Case:18
Type:	Baseline Test
Baseline Name:	TestCases_18.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_18.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:18
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_18.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

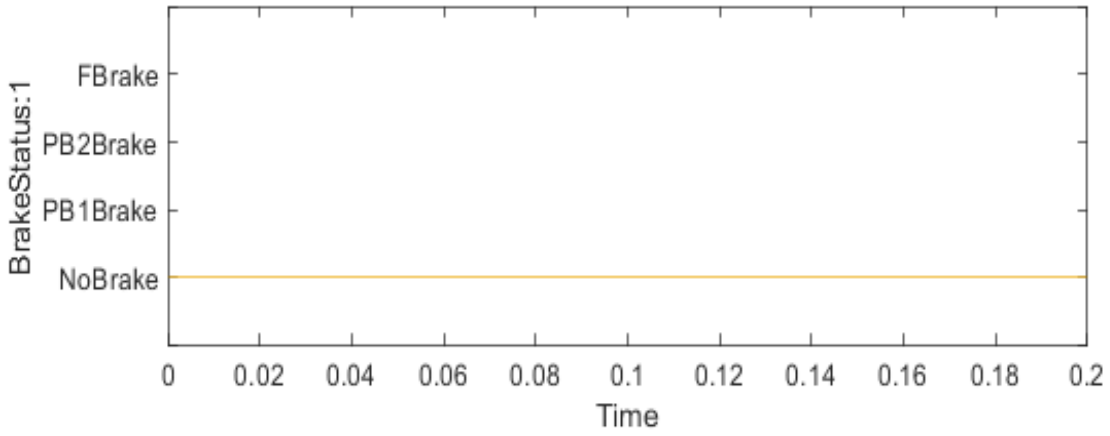
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:18
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:18
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:29
Simulation Stop Time:	2021-09-22 19:18:29
Platform:	PCWIN64

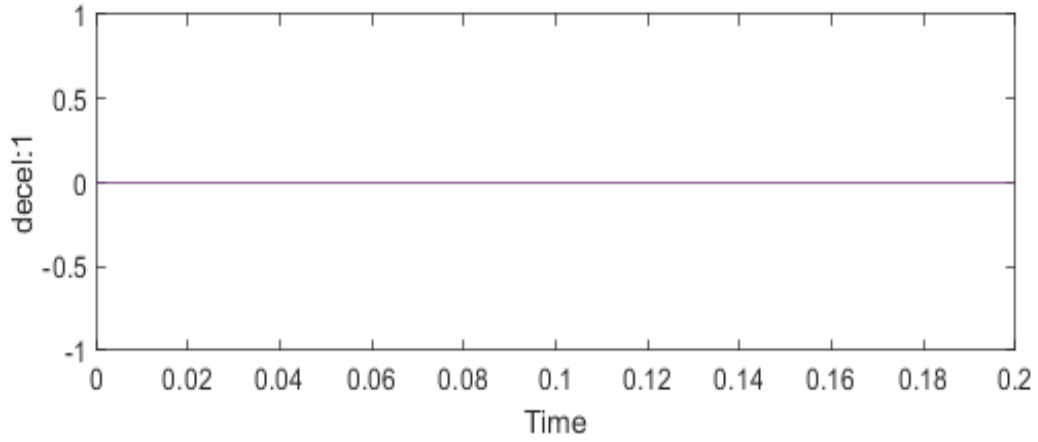
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:19

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:31
End Time:	22-Sep-2021 19:18:33
Outcome:	Passed

Test Case Information

Name:	Test Case:19
Type:	Baseline Test
Baseline Name:	TestCases_19.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_19.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:19
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_19.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

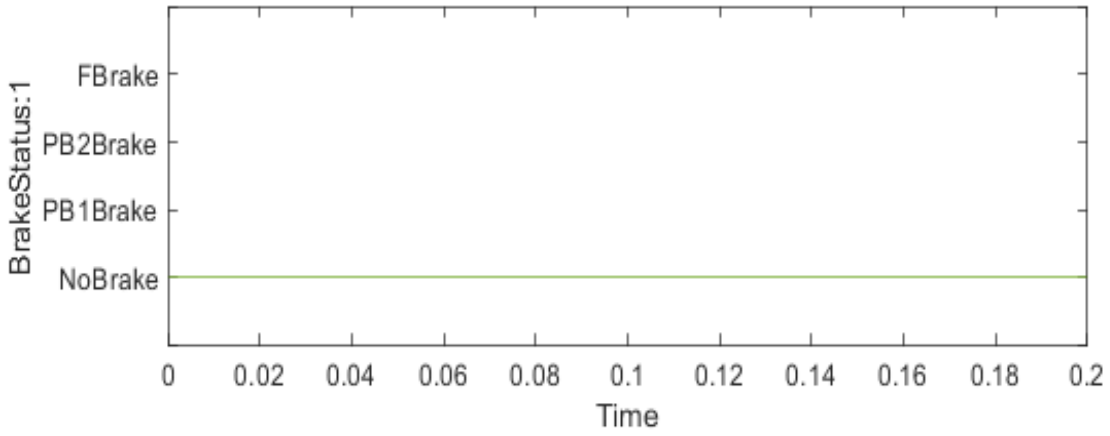
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:19
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:19
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:31
Simulation Stop Time:	2021-09-22 19:18:31
Platform:	PCWIN64

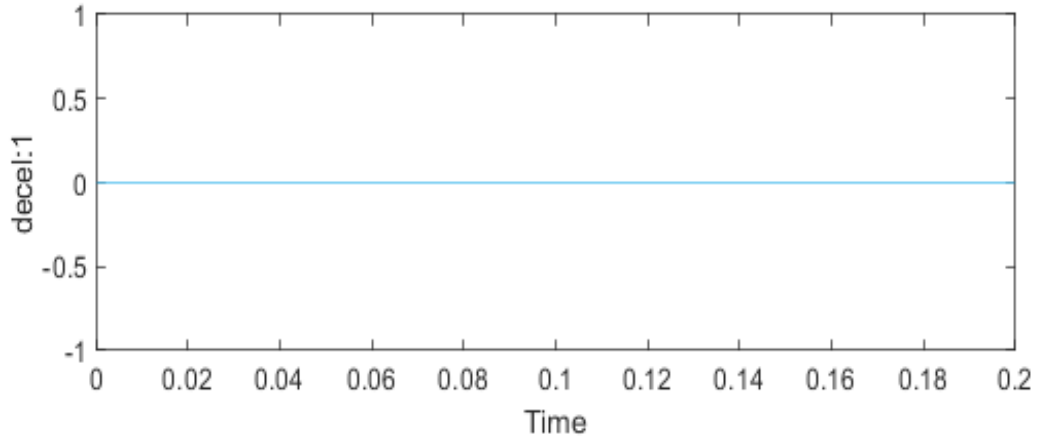
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:20

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:33
End Time:	22-Sep-2021 19:18:35
Outcome:	Passed

Test Case Information

Name:	Test Case:20
Type:	Baseline Test
Baseline Name:	TestCases_20.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_20.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:20
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_20.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

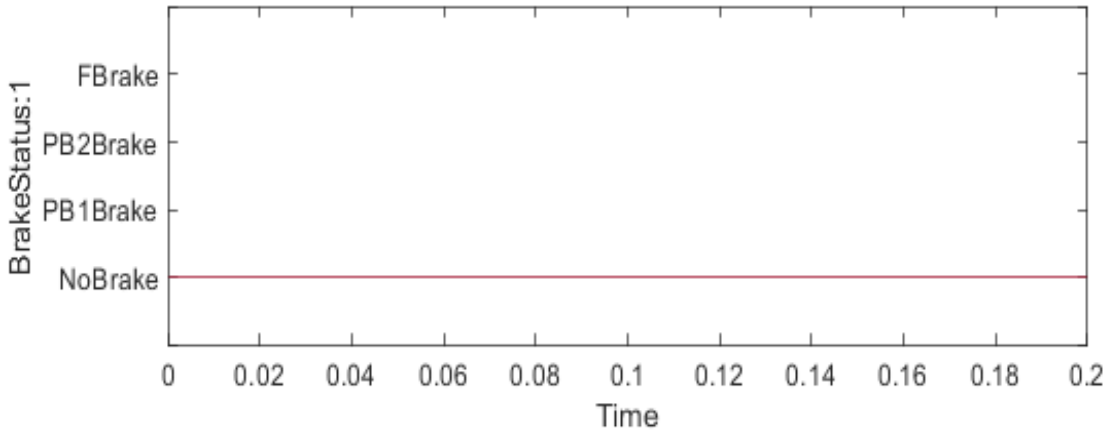
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:20
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:20
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:33
Simulation Stop Time:	2021-09-22 19:18:33
Platform:	PCWIN64

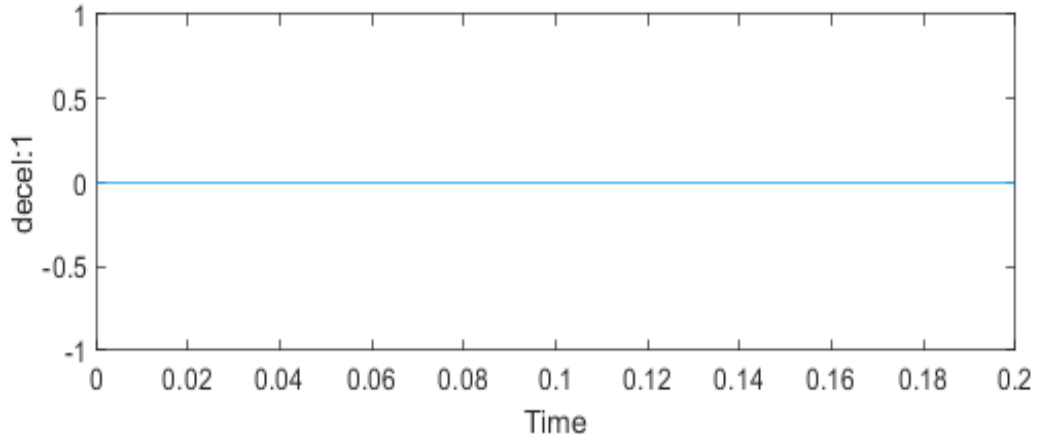
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:21

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:35
End Time:	22-Sep-2021 19:18:37
Outcome:	Passed

Test Case Information

Name:	Test Case:21
Type:	Baseline Test
Baseline Name:	TestCases_21.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_21.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:21
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_21.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

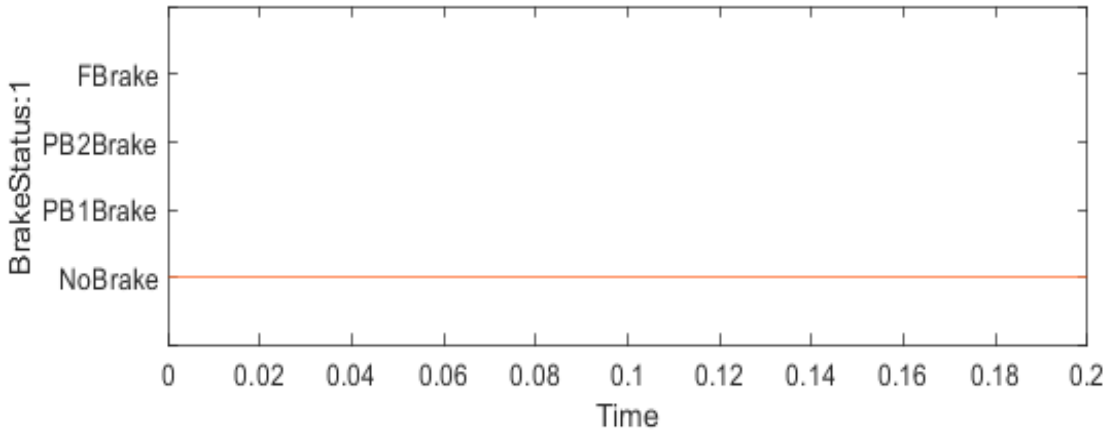
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:21
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:21
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:35
Simulation Stop Time:	2021-09-22 19:18:35
Platform:	PCWIN64

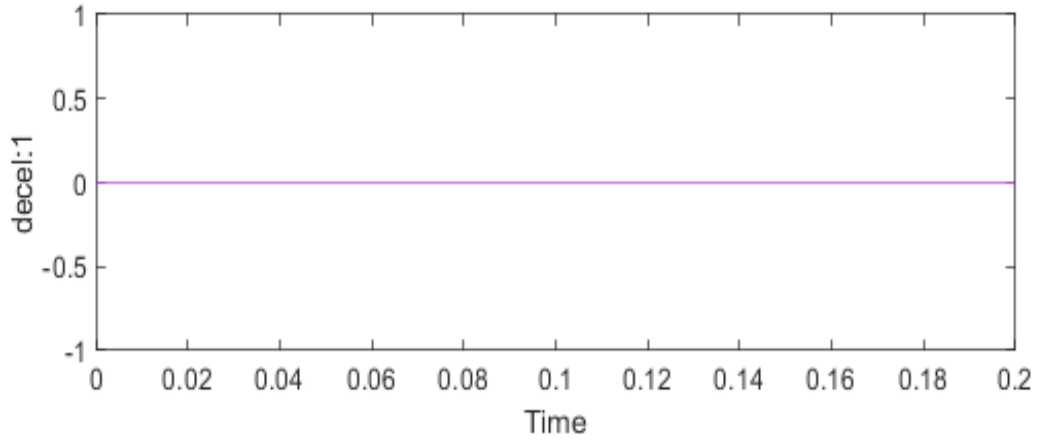
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:22

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:37
End Time:	22-Sep-2021 19:18:38
Outcome:	Passed

Test Case Information

Name:	Test Case:22
Type:	Baseline Test
Baseline Name:	TestCases_22.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_22.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:22
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_22.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

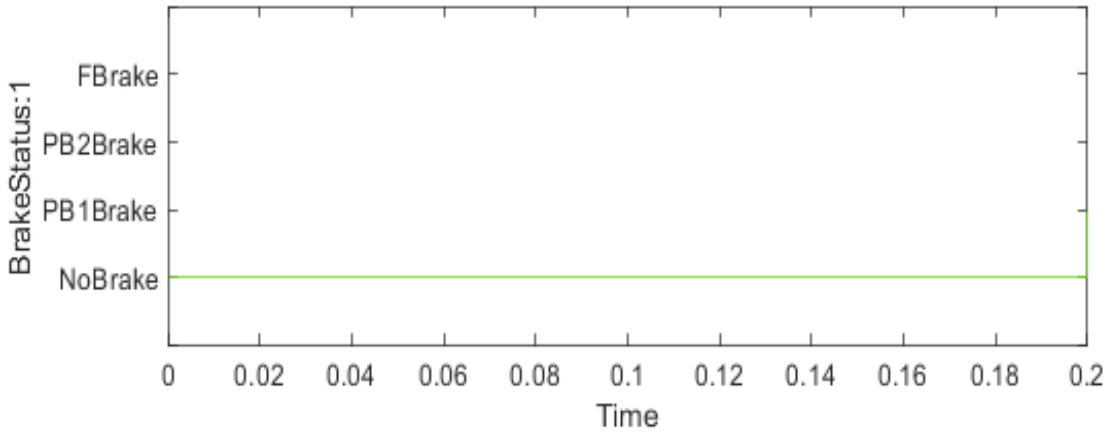
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:22
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:22
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:37
Simulation Stop Time:	2021-09-22 19:18:37
Platform:	PCWIN64

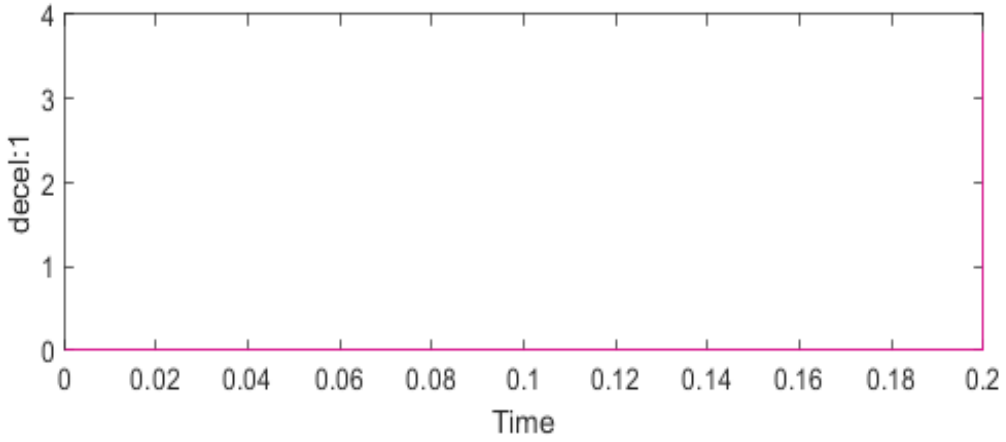
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:23

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:38
End Time:	22-Sep-2021 19:18:40
Outcome:	Passed

Test Case Information

Name:	Test Case:23
Type:	Baseline Test
Baseline Name:	TestCases_23.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_23.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:23
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_23.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

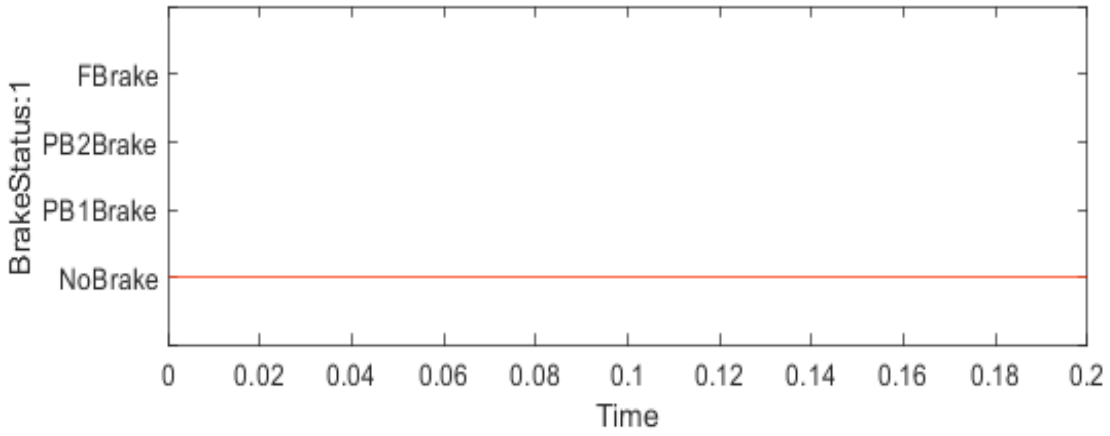
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:23
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:23
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:38
Simulation Stop Time:	2021-09-22 19:18:39
Platform:	PCWIN64

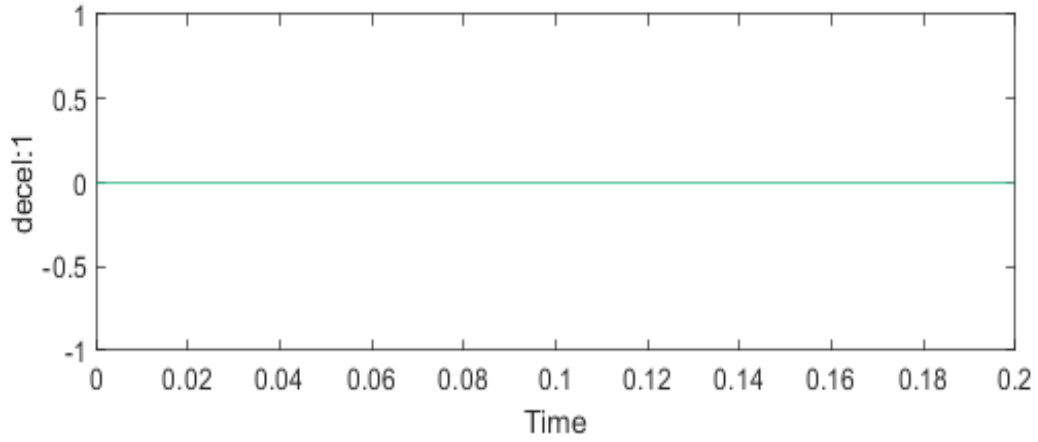
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:24

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:40
End Time:	22-Sep-2021 19:18:42
Outcome:	Passed

Test Case Information

Name:	Test Case:24
Type:	Baseline Test
Baseline Name:	TestCases_24.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_24.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:24
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_24.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

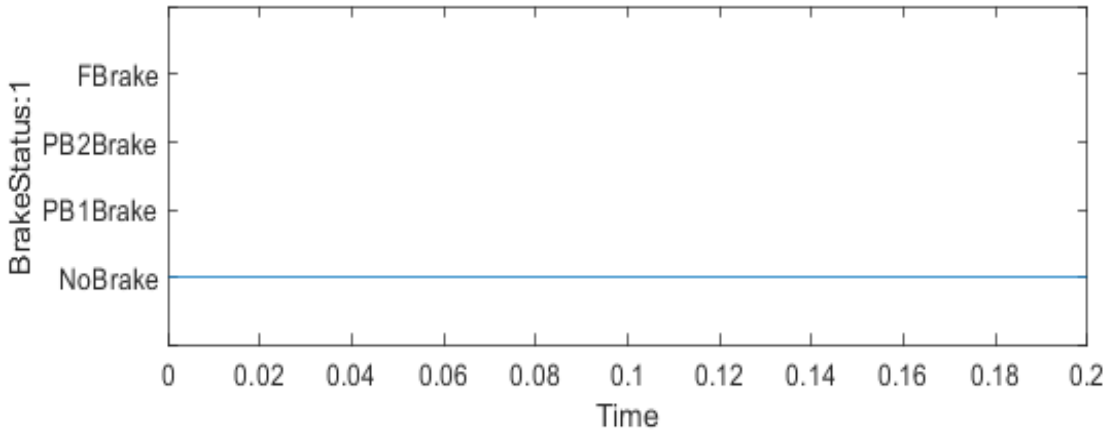
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:24
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:24
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:40
Simulation Stop Time:	2021-09-22 19:18:41
Platform:	PCWIN64

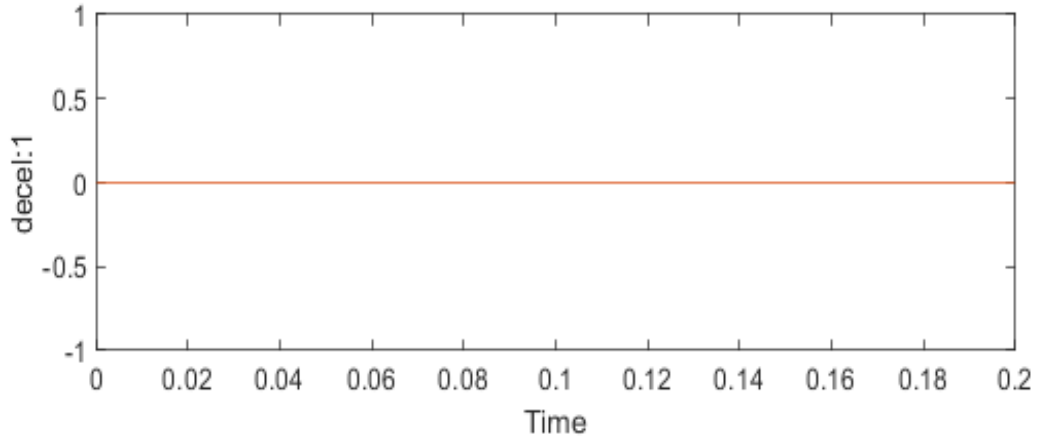
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:25

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:42
End Time:	22-Sep-2021 19:18:44
Outcome:	Passed

Test Case Information

Name:	Test Case:25
Type:	Baseline Test
Baseline Name:	TestCases_25.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_25.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:25
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_25.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

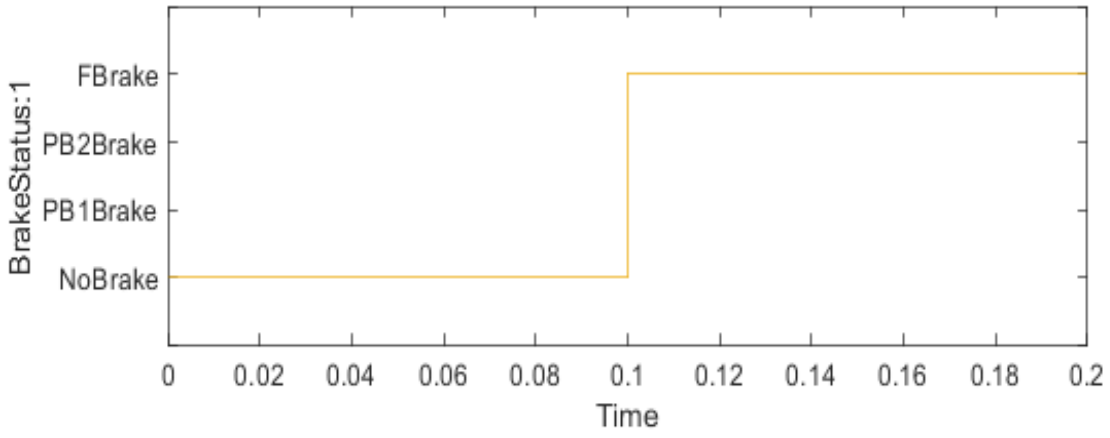
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:25
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:25
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:42
Simulation Stop Time:	2021-09-22 19:18:42
Platform:	PCWIN64

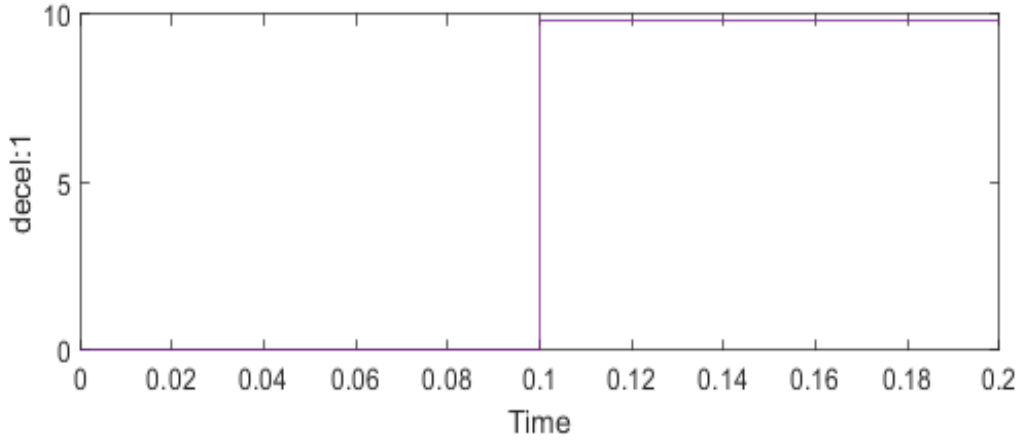
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:26

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:44
End Time:	22-Sep-2021 19:18:46
Outcome:	Passed

Test Case Information

Name:	Test Case:26
Type:	Baseline Test
Baseline Name:	TestCases_26.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_26.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:26
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_26.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

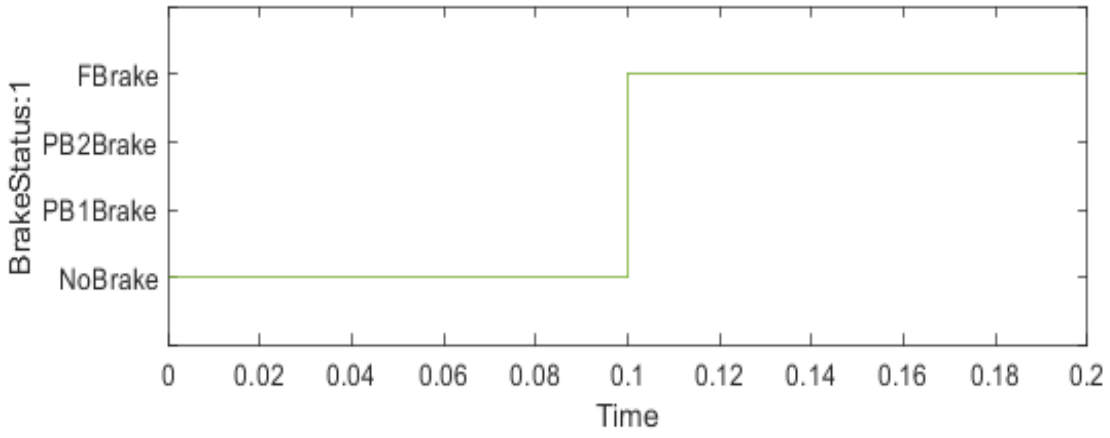
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:26
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:26
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:44
Simulation Stop Time:	2021-09-22 19:18:44
Platform:	PCWIN64

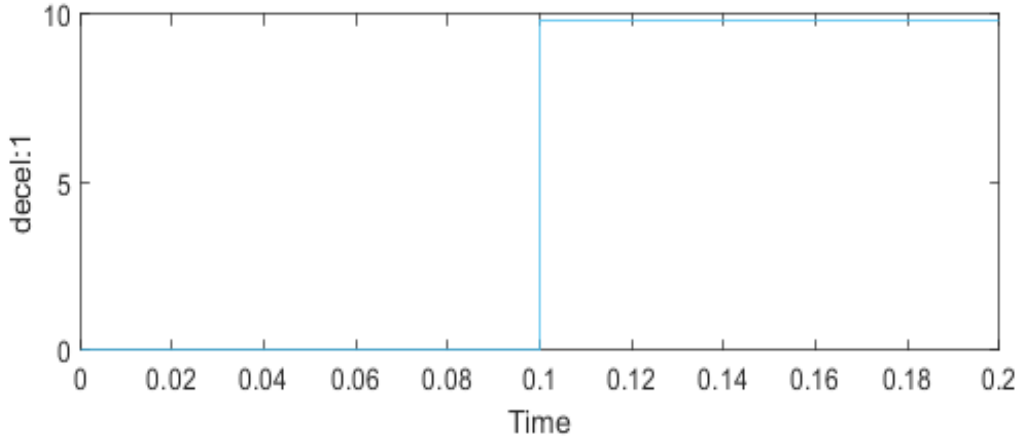
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:27

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:46
End Time:	22-Sep-2021 19:18:48
Outcome:	Passed

Test Case Information

Name:	Test Case:27
Type:	Baseline Test
Baseline Name:	TestCases_27.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_27.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:27
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_27.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

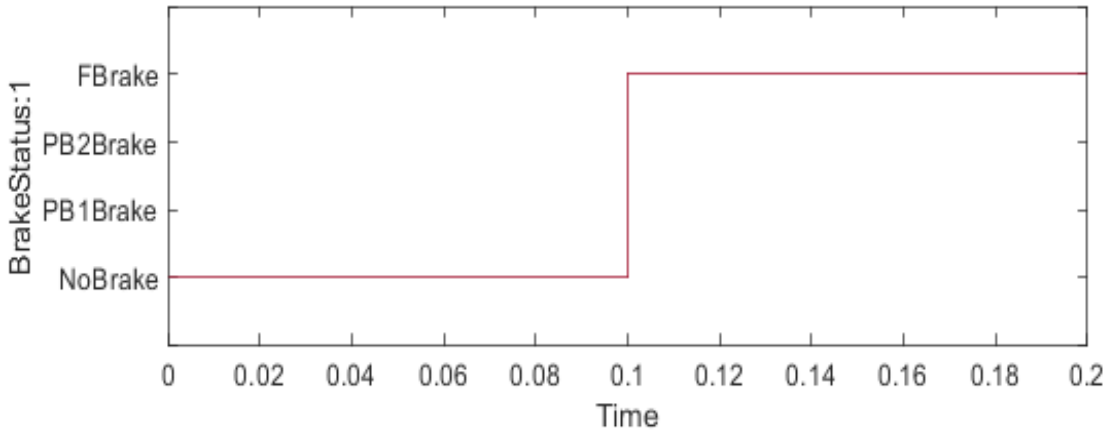
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:27
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:27
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:46
Simulation Stop Time:	2021-09-22 19:18:46
Platform:	PCWIN64

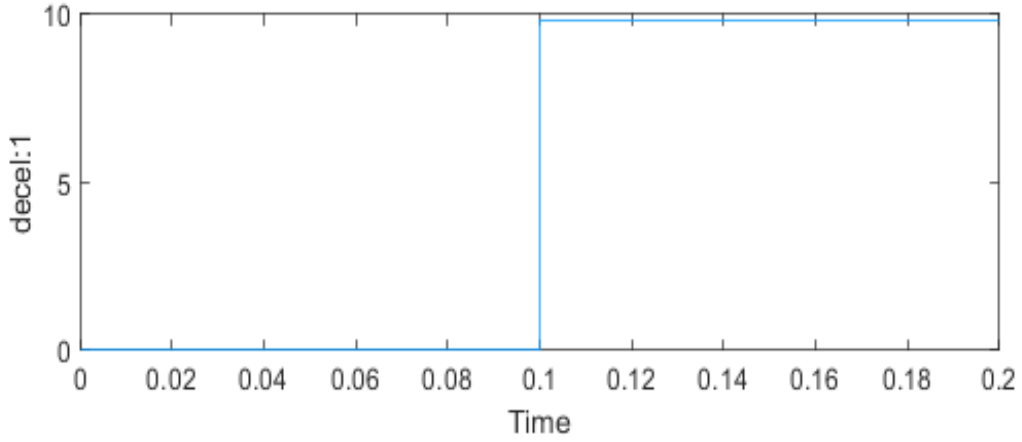
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:28

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:48
End Time:	22-Sep-2021 19:18:50
Outcome:	Passed

Test Case Information

Name:	Test Case:28
Type:	Baseline Test
Baseline Name:	TestCases_28.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_28.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:28
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_28.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

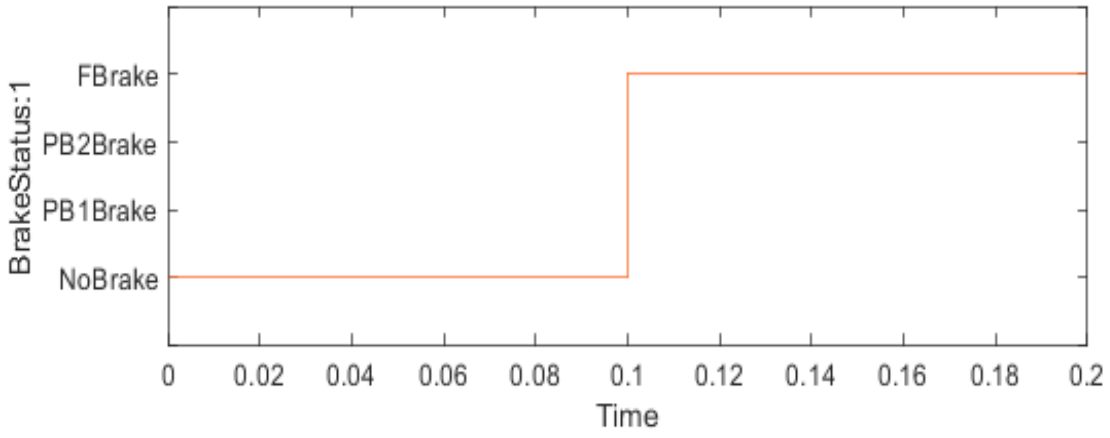
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:28
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:28
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:48
Simulation Stop Time:	2021-09-22 19:18:48
Platform:	PCWIN64

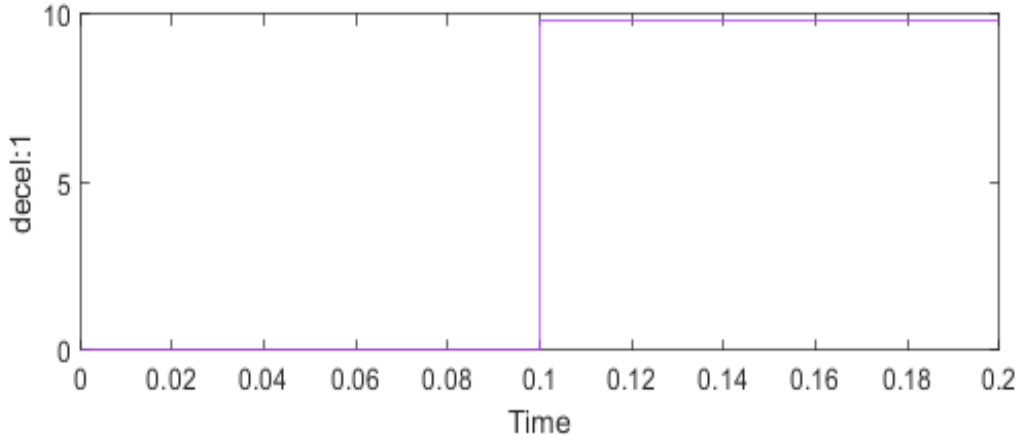
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:29

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:50
End Time:	22-Sep-2021 19:18:52
Outcome:	Passed

Test Case Information

Name:	Test Case:29
Type:	Baseline Test
Baseline Name:	TestCases_29.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_29.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:29
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_29.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

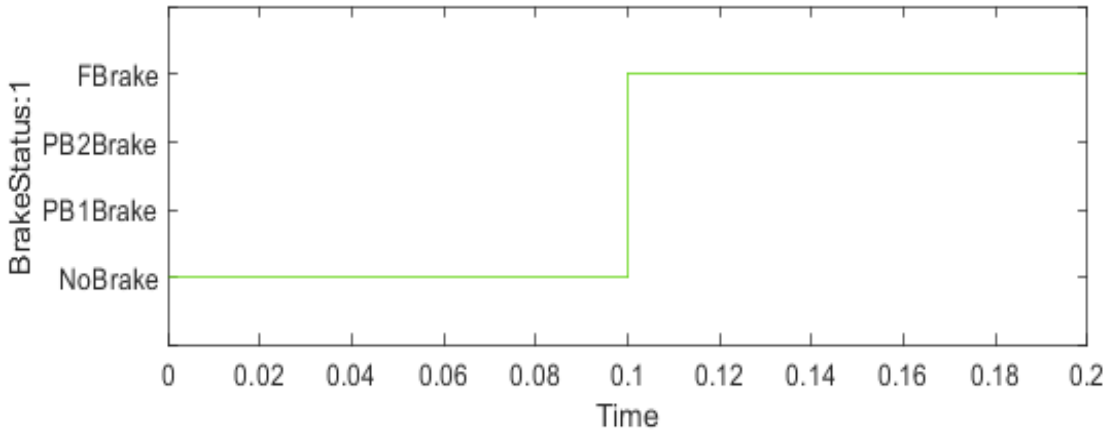
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:29
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:29
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:50
Simulation Stop Time:	2021-09-22 19:18:50
Platform:	PCWIN64

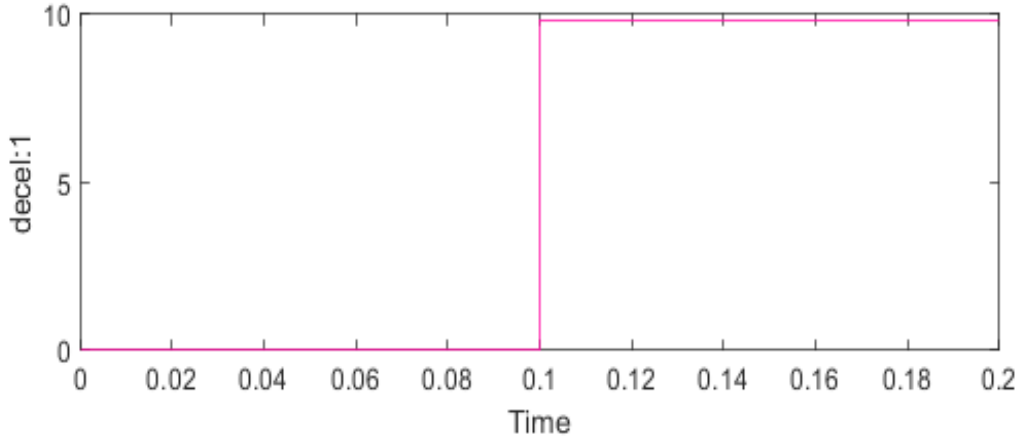
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:30

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:52
End Time:	22-Sep-2021 19:18:54
Outcome:	Passed

Test Case Information

Name:	Test Case:30
Type:	Baseline Test
Baseline Name:	TestCases_30.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_30.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:30
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_30.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

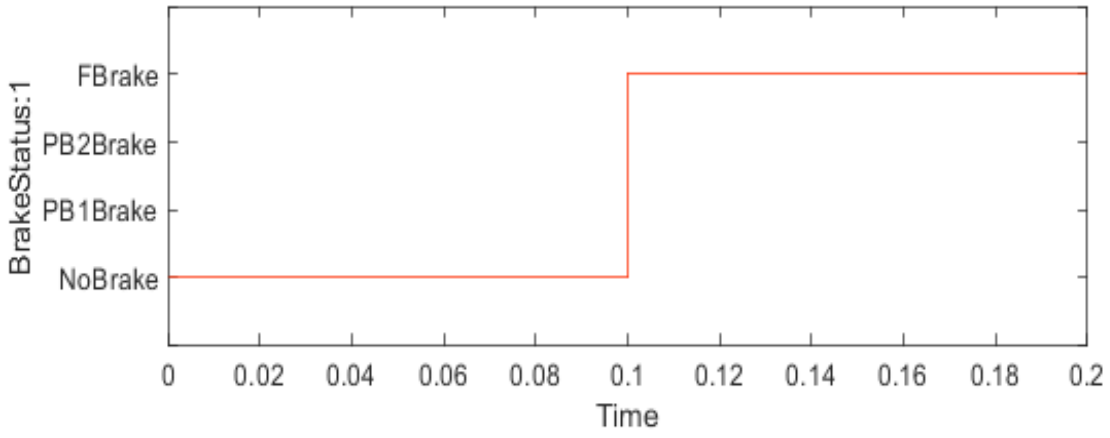
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:30
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:30
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:52
Simulation Stop Time:	2021-09-22 19:18:52
Platform:	PCWIN64

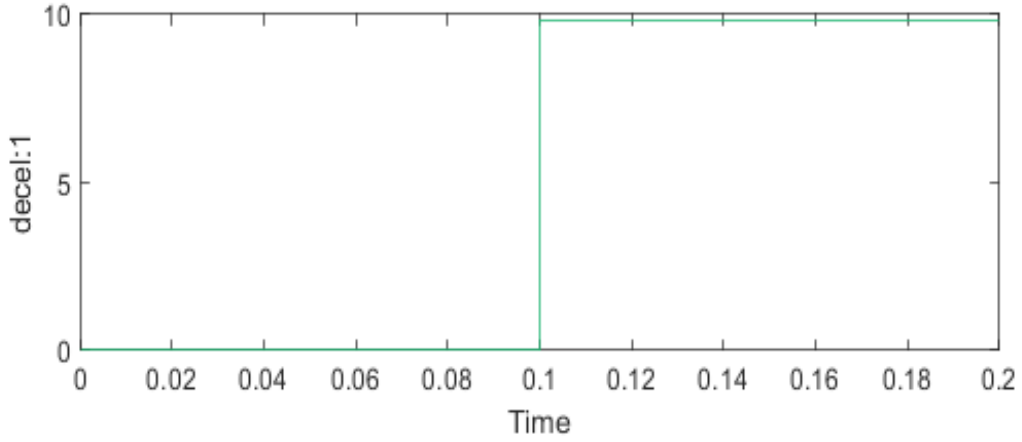
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:31

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:54
End Time:	22-Sep-2021 19:18:56
Outcome:	Passed

Test Case Information

Name:	Test Case:31
Type:	Baseline Test
Baseline Name:	TestCases_31.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_31.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:31
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_31.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

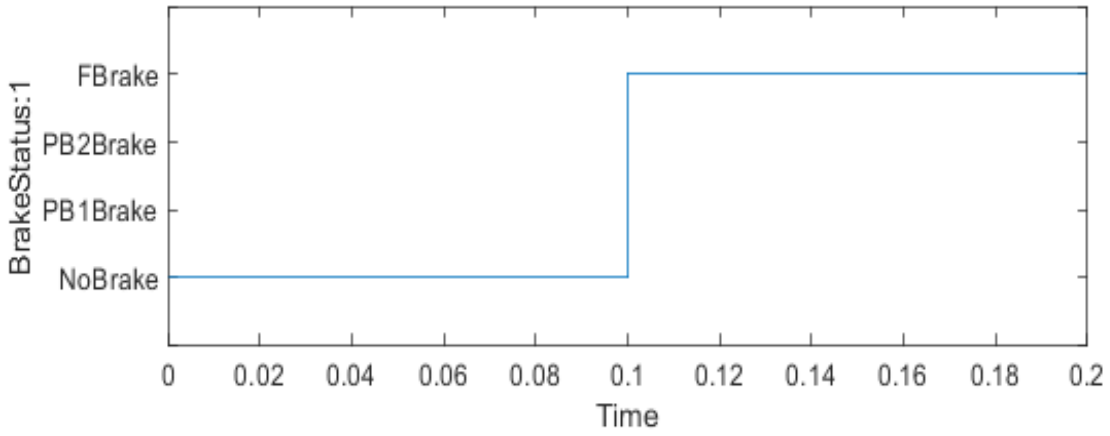
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:31
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:31
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:54
Simulation Stop Time:	2021-09-22 19:18:54
Platform:	PCWIN64

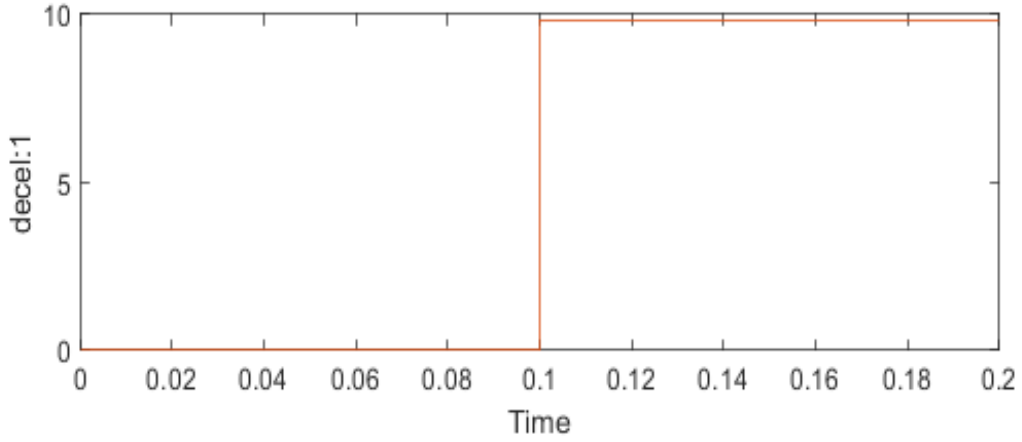
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:32

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:56
End Time:	22-Sep-2021 19:18:58
Outcome:	Passed

Test Case Information

Name:	Test Case:32
Type:	Baseline Test
Baseline Name:	TestCases_32.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_32.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:32
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_32.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

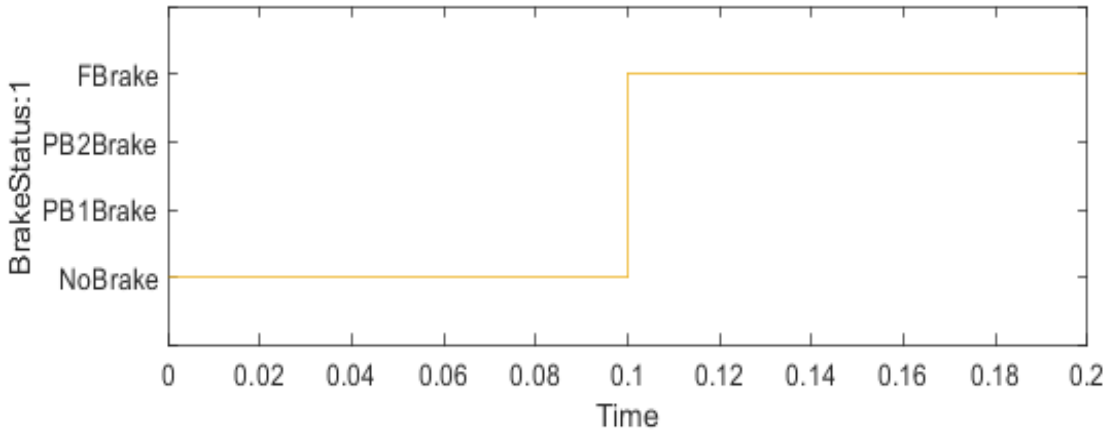
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:32
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:32
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:56
Simulation Stop Time:	2021-09-22 19:18:56
Platform:	PCWIN64

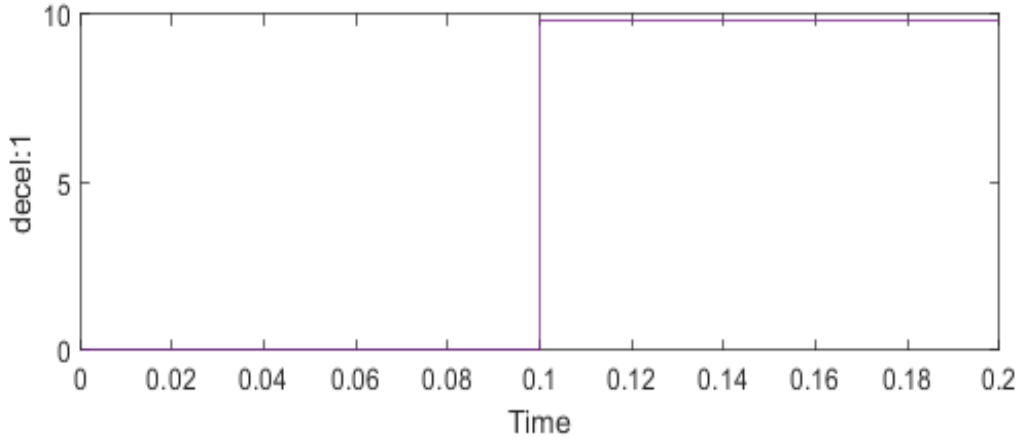
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:33

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:18:58
End Time:	22-Sep-2021 19:18:59
Outcome:	Passed

Test Case Information

Name:	Test Case:33
Type:	Baseline Test
Baseline Name:	TestCases_33.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_33.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:33
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_33.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

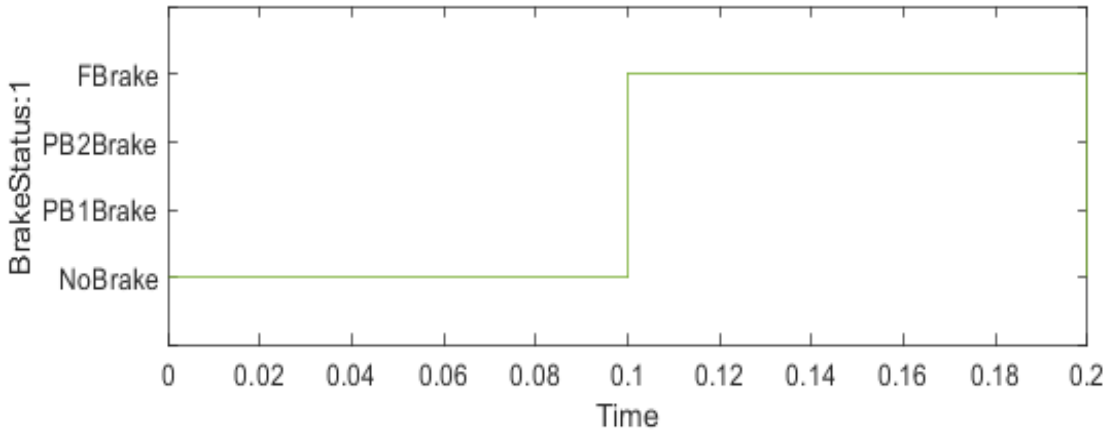
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:33
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:33
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:18:58
Simulation Stop Time:	2021-09-22 19:18:58
Platform:	PCWIN64

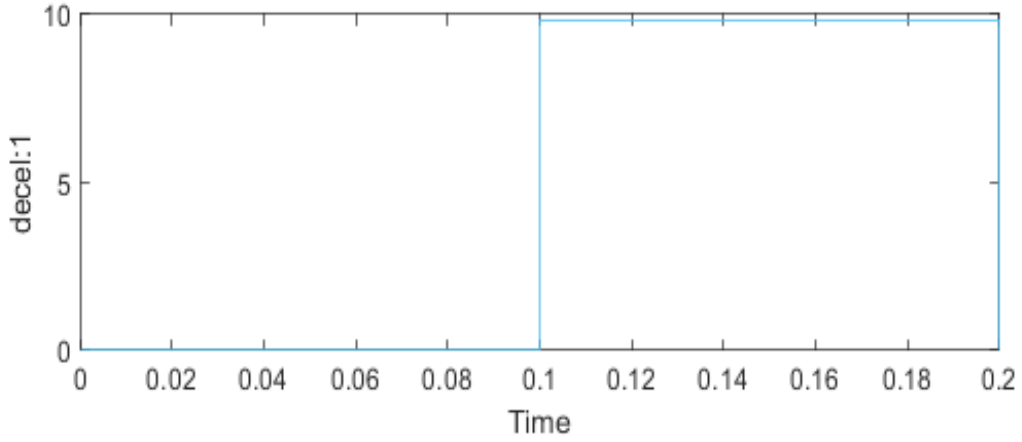
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:34

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:00
End Time:	22-Sep-2021 19:19:01
Outcome:	Passed

Test Case Information

Name:	Test Case:34
Type:	Baseline Test
Baseline Name:	TestCases_34.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_34.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:34
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_34.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

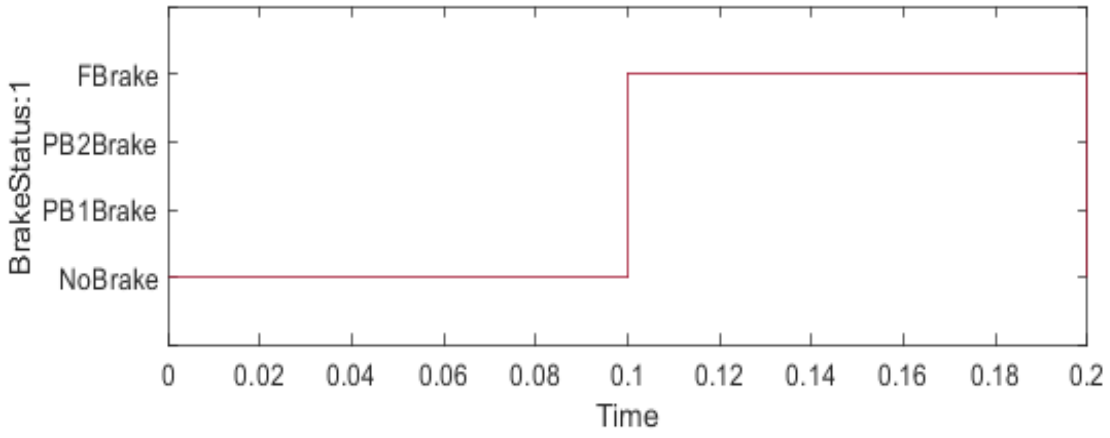
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:34
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:34
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:00
Simulation Stop Time:	2021-09-22 19:19:00
Platform:	PCWIN64

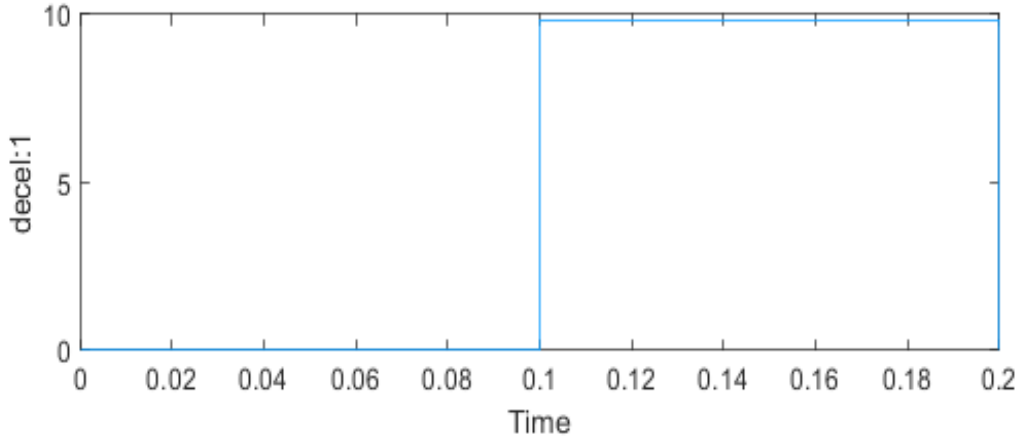
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:35

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:01
End Time:	22-Sep-2021 19:19:03
Outcome:	Passed

Test Case Information

Name:	Test Case:35
Type:	Baseline Test
Baseline Name:	TestCases_35.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_35.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:35
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_35.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

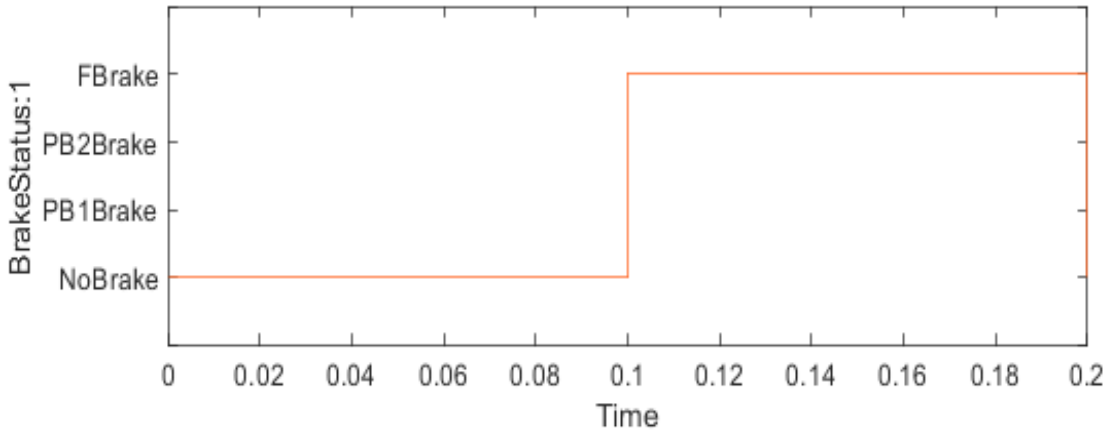
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:35
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:35
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:02
Simulation Stop Time:	2021-09-22 19:19:02
Platform:	PCWIN64

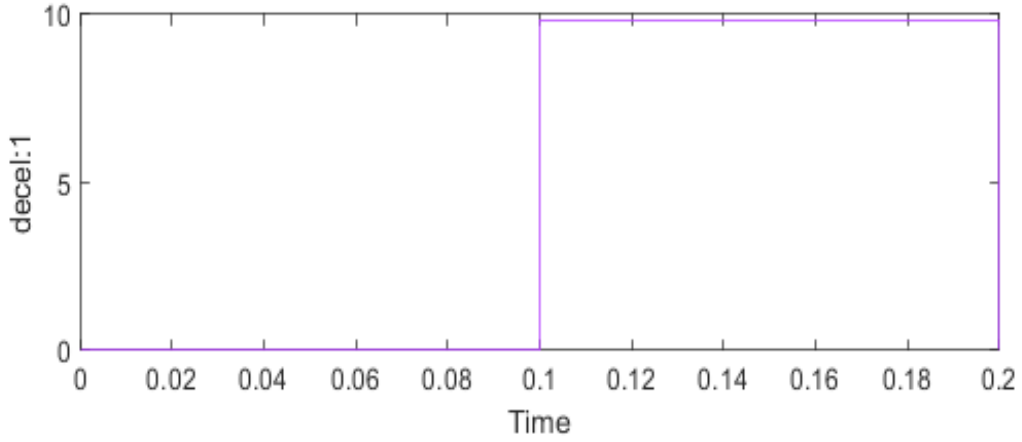
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:36

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:03
End Time:	22-Sep-2021 19:19:05
Outcome:	Passed

Test Case Information

Name:	Test Case:36
Type:	Baseline Test
Baseline Name:	TestCases_36.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_36.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:36
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_36.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

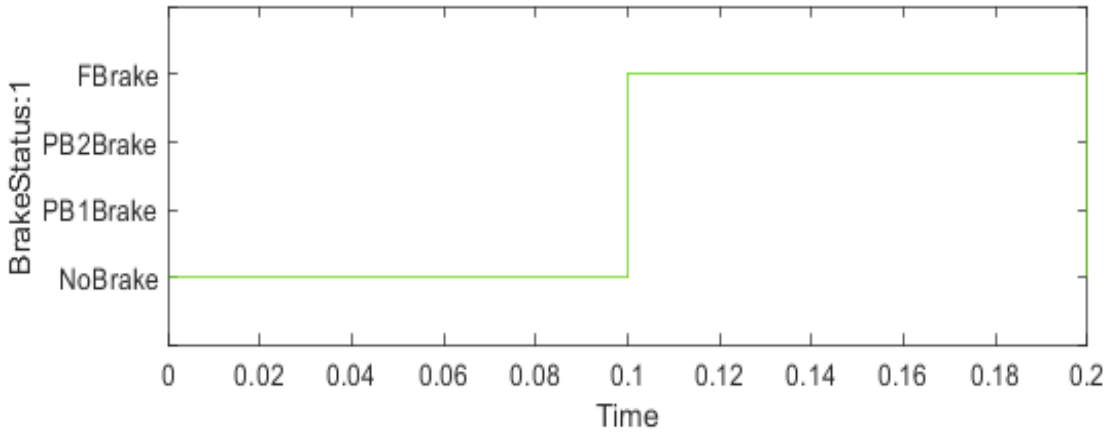
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:36
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:36
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:04
Simulation Stop Time:	2021-09-22 19:19:04
Platform:	PCWIN64

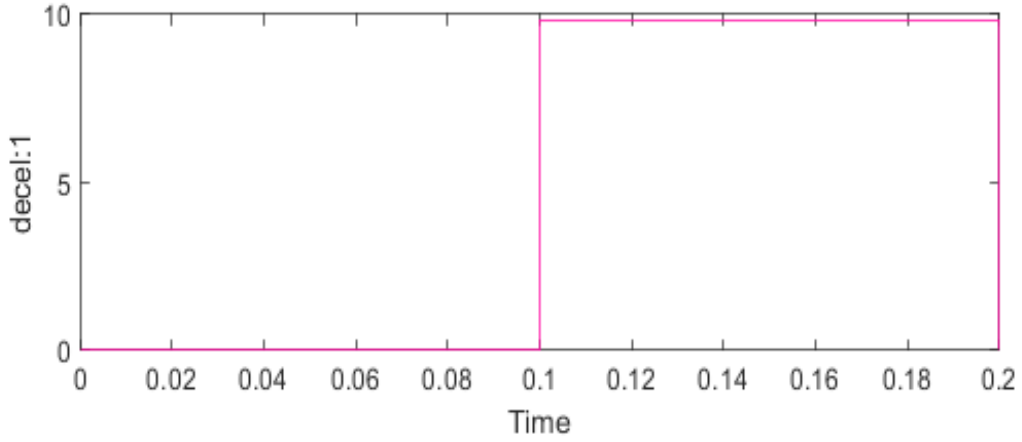
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:37

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:05
End Time:	22-Sep-2021 19:19:07
Outcome:	Passed

Test Case Information

Name:	Test Case:37
Type:	Baseline Test
Baseline Name:	TestCases_37.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_37.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:37
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_37.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

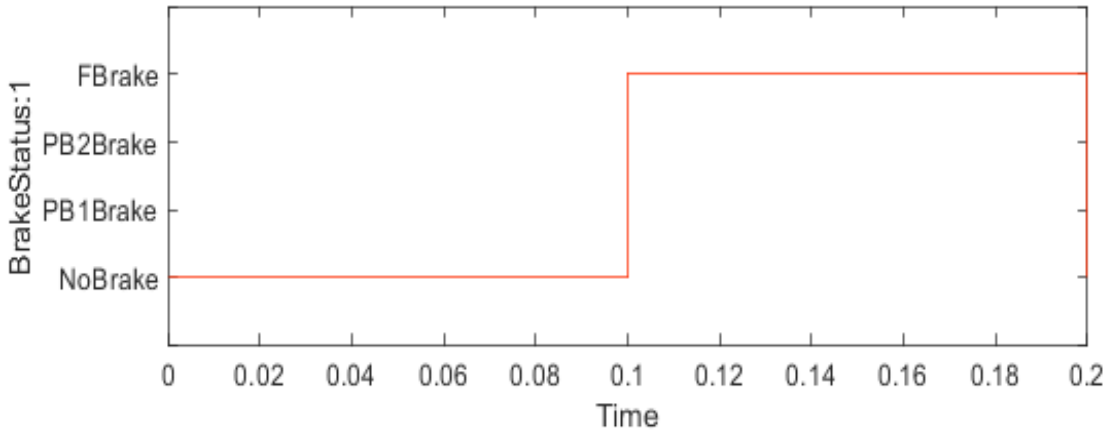
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:37
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:37
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:05
Simulation Stop Time:	2021-09-22 19:19:06
Platform:	PCWIN64

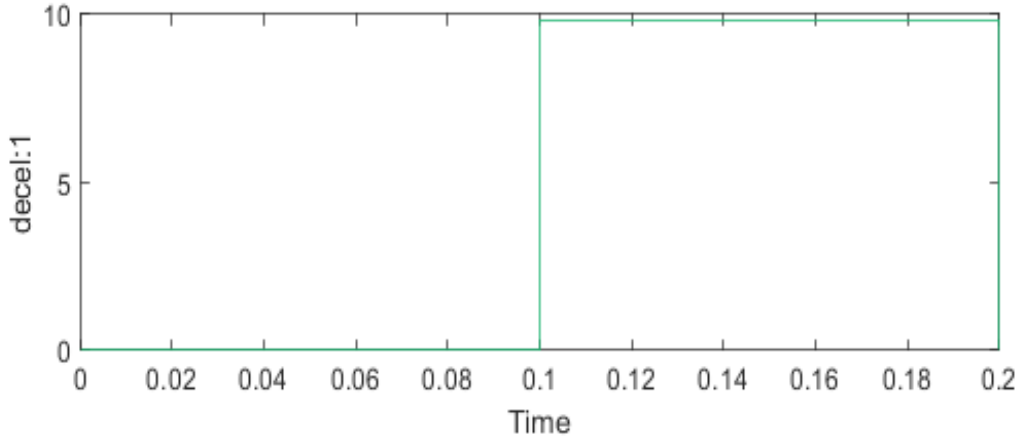
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:38

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:07
End Time:	22-Sep-2021 19:19:09
Outcome:	Passed

Test Case Information

Name:	Test Case:38
Type:	Baseline Test
Baseline Name:	TestCases_38.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_38.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:38
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_38.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

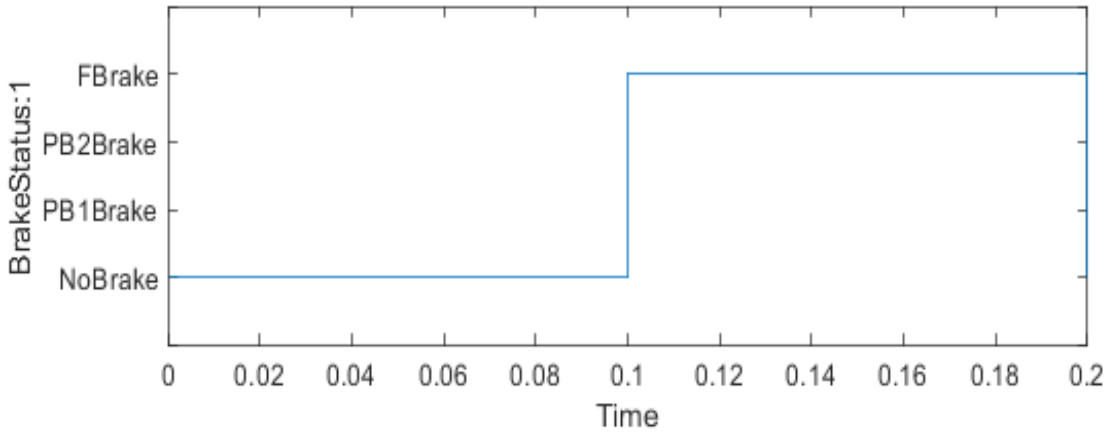
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:38
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:38
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:07
Simulation Stop Time:	2021-09-22 19:19:08
Platform:	PCWIN64

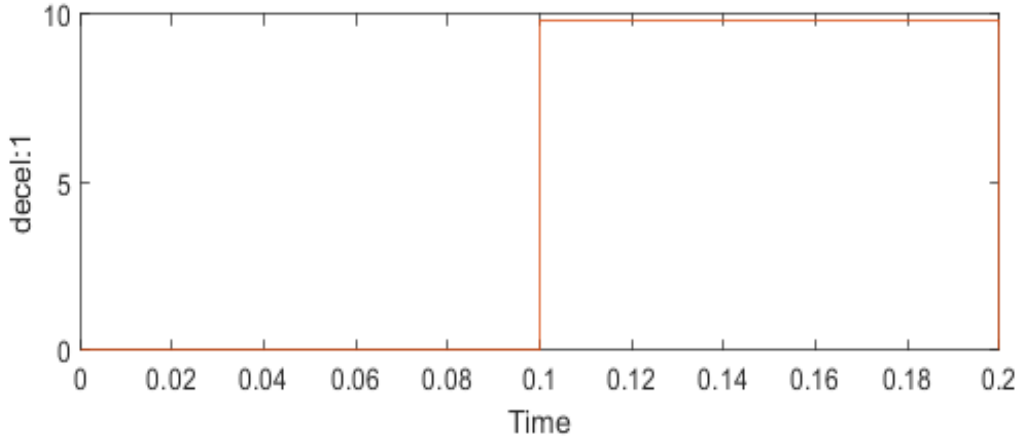
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:39

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:09
End Time:	22-Sep-2021 19:19:11
Outcome:	Passed

Test Case Information

Name:	Test Case:39
Type:	Baseline Test
Baseline Name:	TestCases_39.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_39.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:39
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_39.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

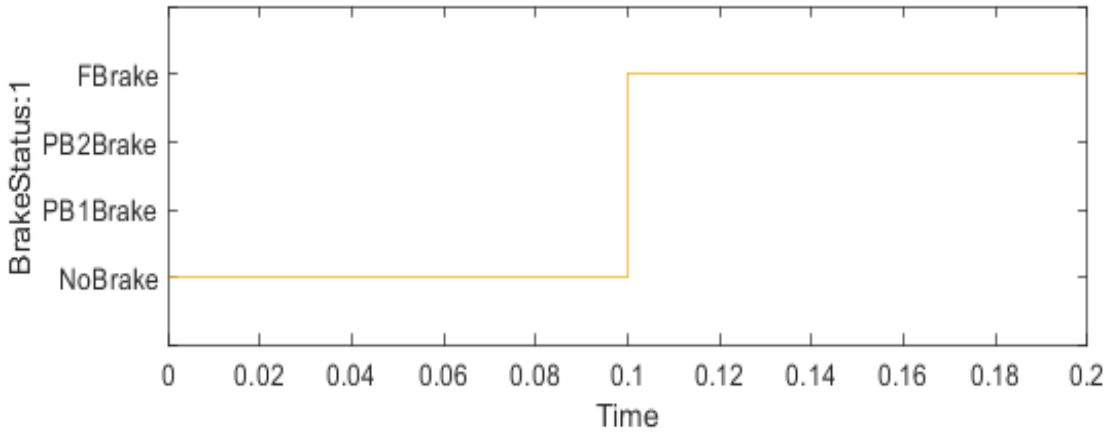
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:39
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:39
Start Time:	0
Stop Time:	0.20000000000000001
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:09
Simulation Stop Time:	2021-09-22 19:19:09
Platform:	PCWIN64

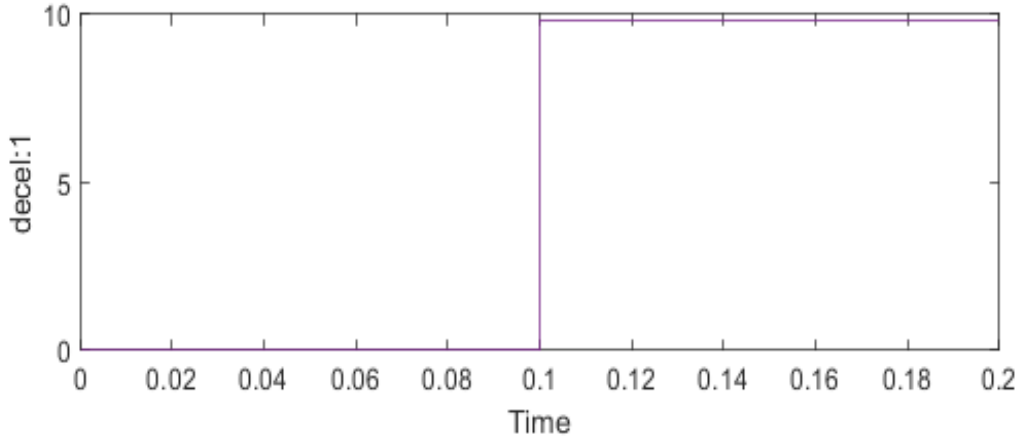
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:40

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:11
End Time:	22-Sep-2021 19:19:13
Outcome:	Passed

Test Case Information

Name:	Test Case:40
Type:	Baseline Test
Baseline Name:	TestCases_40.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_40.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:40
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_40.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

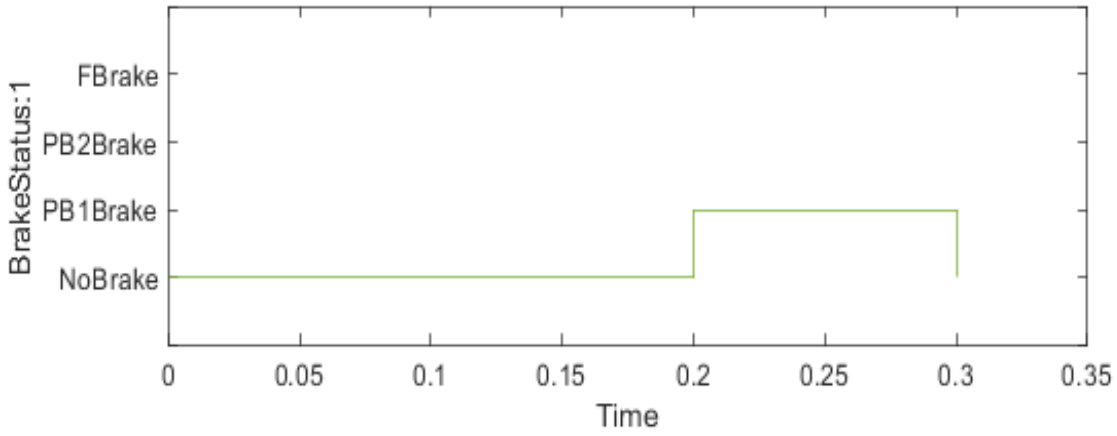
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:40
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:40
Start Time:	0
Stop Time:	0.30000000000000004
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:11
Simulation Stop Time:	2021-09-22 19:19:11
Platform:	PCWIN64

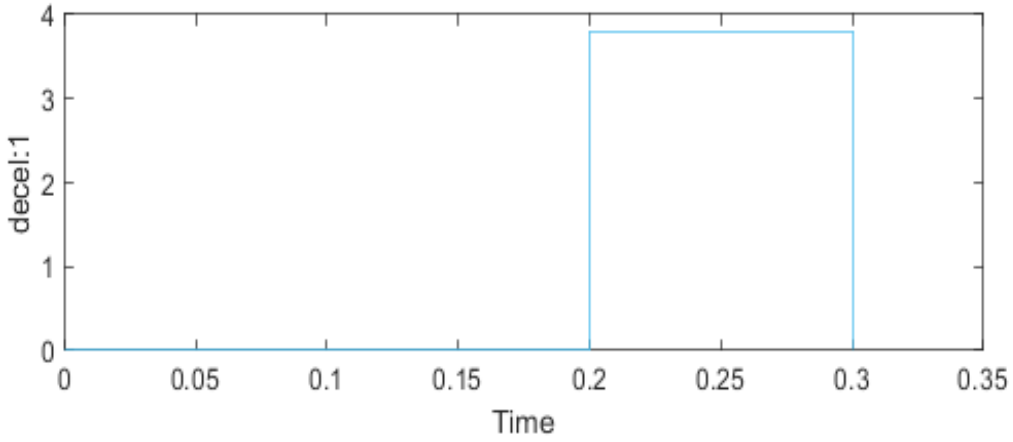
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:41

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:13
End Time:	22-Sep-2021 19:19:15
Outcome:	Passed

Test Case Information

Name:	Test Case:41
Type:	Baseline Test
Baseline Name:	TestCases_41.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_41.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:41
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_41.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

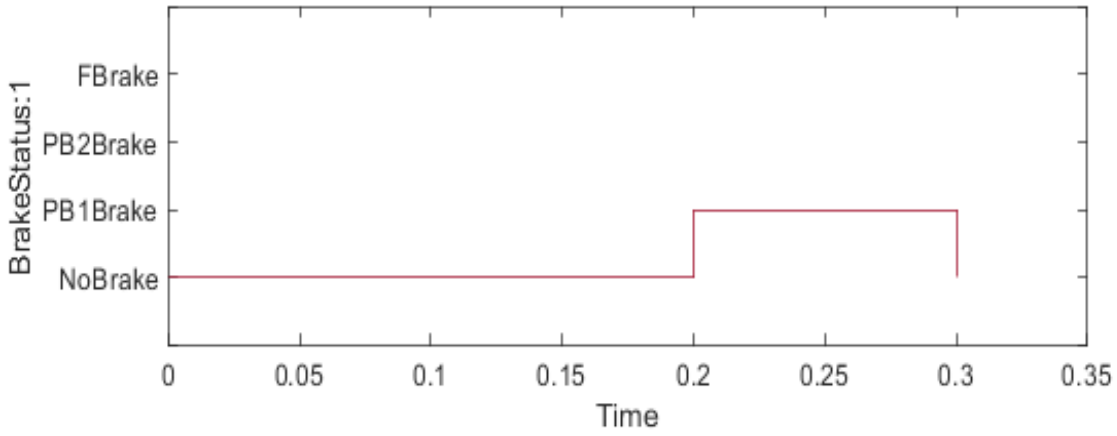
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:41
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:41
Start Time:	0
Stop Time:	0.30000000000000004
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:13
Simulation Stop Time:	2021-09-22 19:19:13
Platform:	PCWIN64

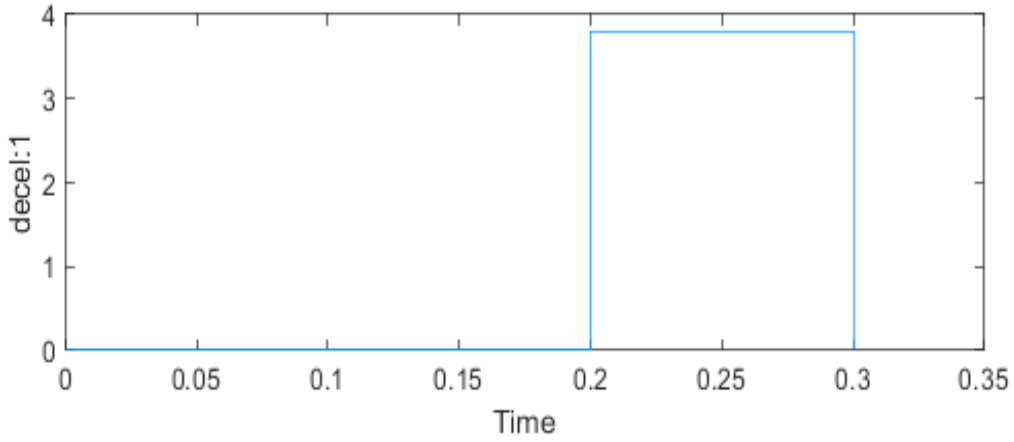
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:42

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:15
End Time:	22-Sep-2021 19:19:17
Outcome:	Passed

Test Case Information

Name:	Test Case:42
Type:	Baseline Test
Baseline Name:	TestCases_42.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_42.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:42
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_42.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

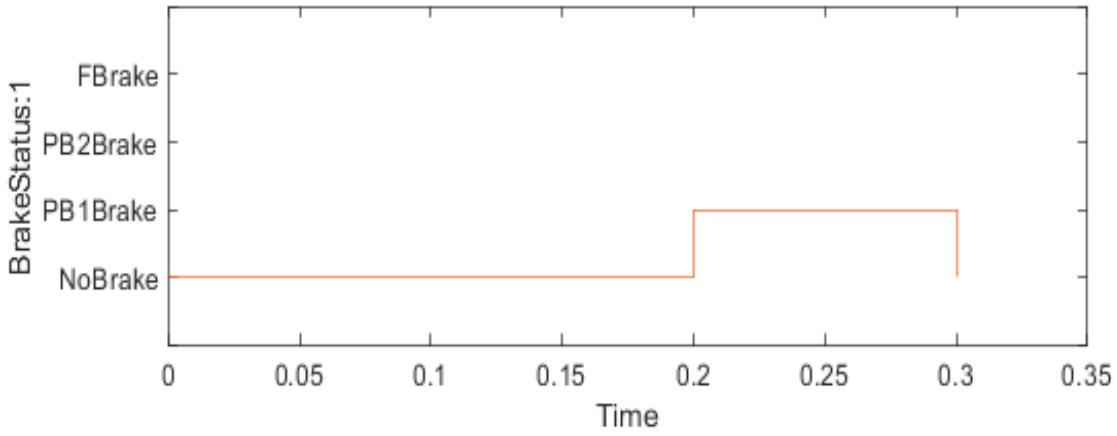
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:42
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:42
Start Time:	0
Stop Time:	0.30000000000000004
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:15
Simulation Stop Time:	2021-09-22 19:19:15
Platform:	PCWIN64

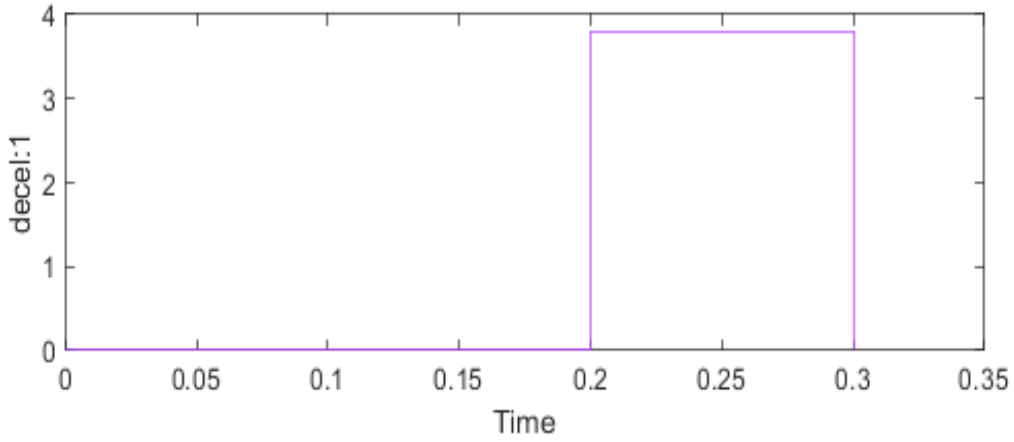
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:43

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:17
End Time:	22-Sep-2021 19:19:19
Outcome:	Passed

Test Case Information

Name:	Test Case:43
Type:	Baseline Test
Baseline Name:	TestCases_43.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_43.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:43
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_43.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

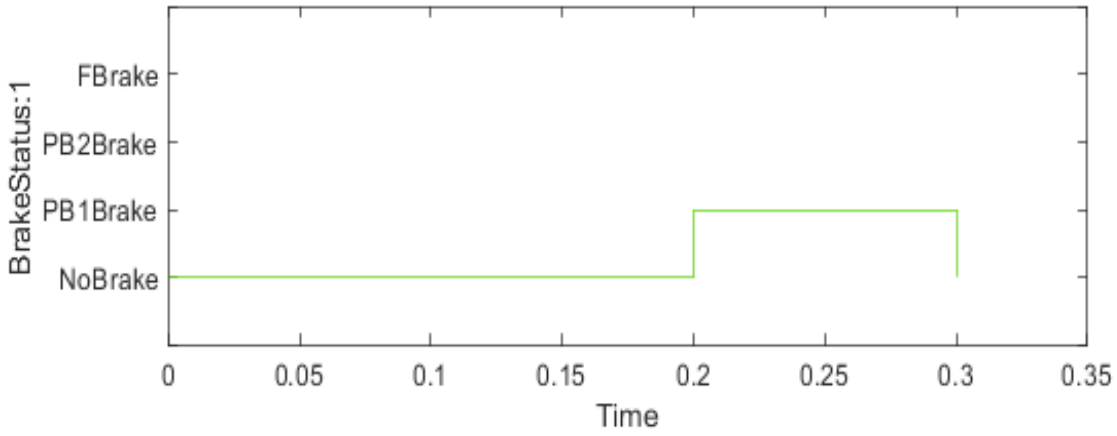
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:43
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:43
Start Time:	0
Stop Time:	0.30000000000000004
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:17
Simulation Stop Time:	2021-09-22 19:19:17
Platform:	PCWIN64

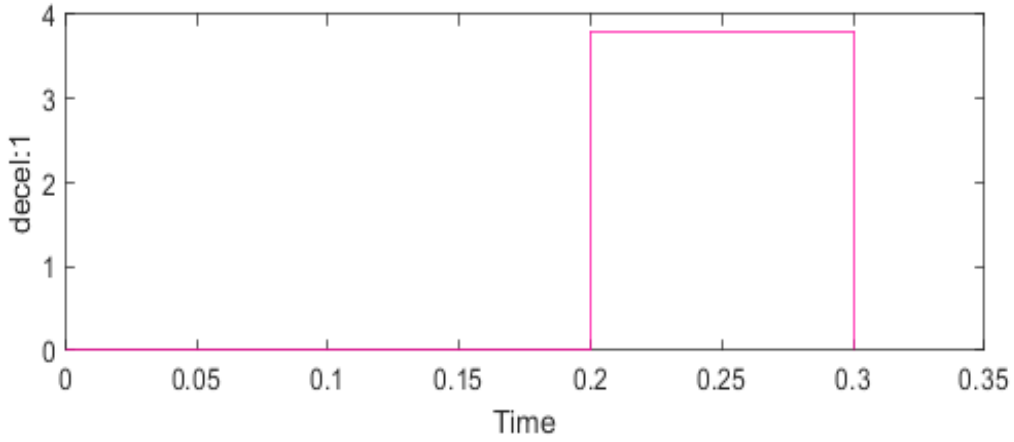
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:44

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:19
End Time:	22-Sep-2021 19:19:21
Outcome:	Passed

Test Case Information

Name:	Test Case:44
Type:	Baseline Test
Baseline Name:	TestCases_44.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_44.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:44
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_44.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

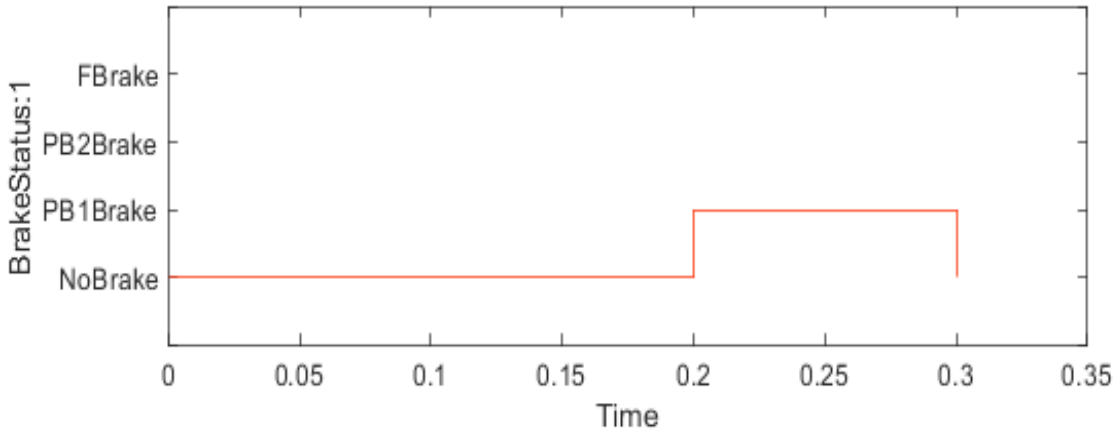
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:44
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:44
Start Time:	0
Stop Time:	0.30000000000000004
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:19
Simulation Stop Time:	2021-09-22 19:19:19
Platform:	PCWIN64

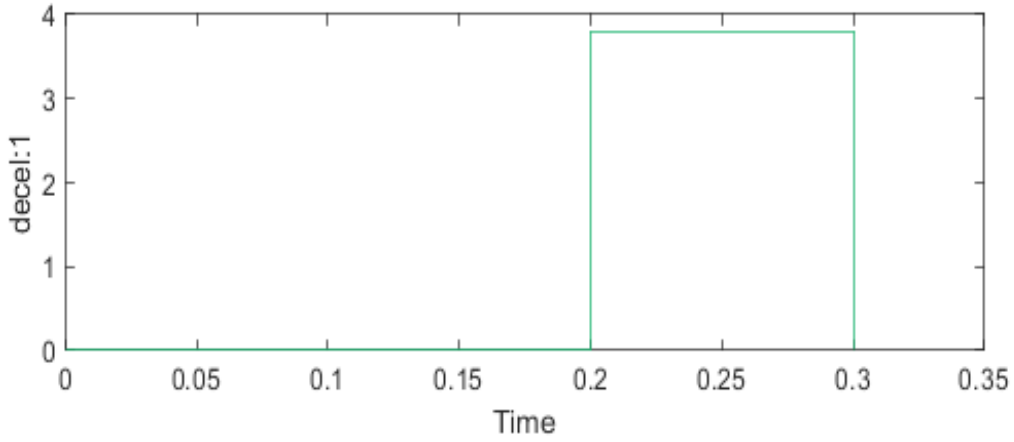
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:45

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:21
End Time:	22-Sep-2021 19:19:23
Outcome:	Passed

Test Case Information

Name:	Test Case:45
Type:	Baseline Test
Baseline Name:	TestCases_45.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_45.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:45
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_45.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

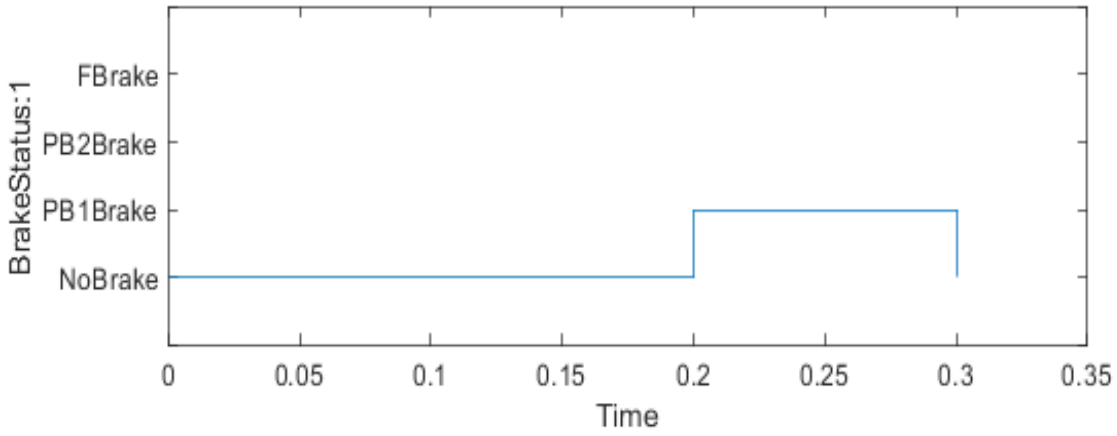
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:45
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:45
Start Time:	0
Stop Time:	0.30000000000000004
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:21
Simulation Stop Time:	2021-09-22 19:19:21
Platform:	PCWIN64

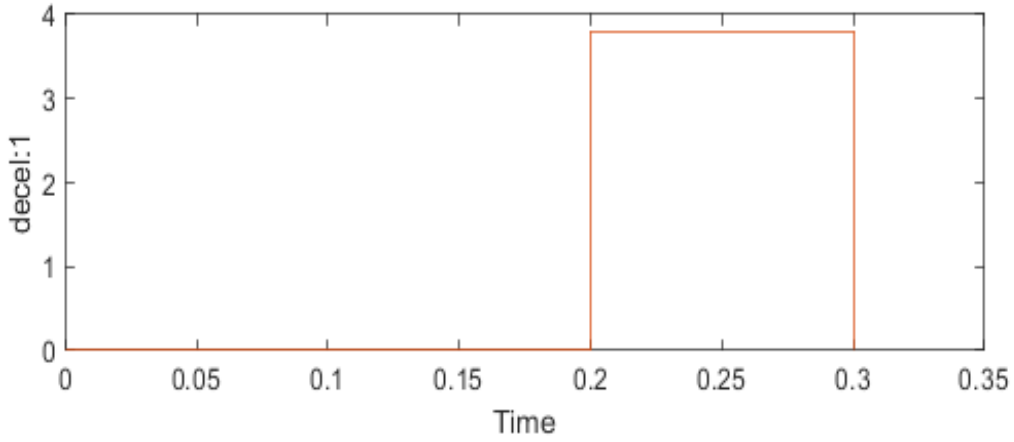
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:46

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:23
End Time:	22-Sep-2021 19:19:24
Outcome:	Passed

Test Case Information

Name:	Test Case:46
Type:	Baseline Test
Baseline Name:	TestCases_46.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_46.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:46
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_46.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

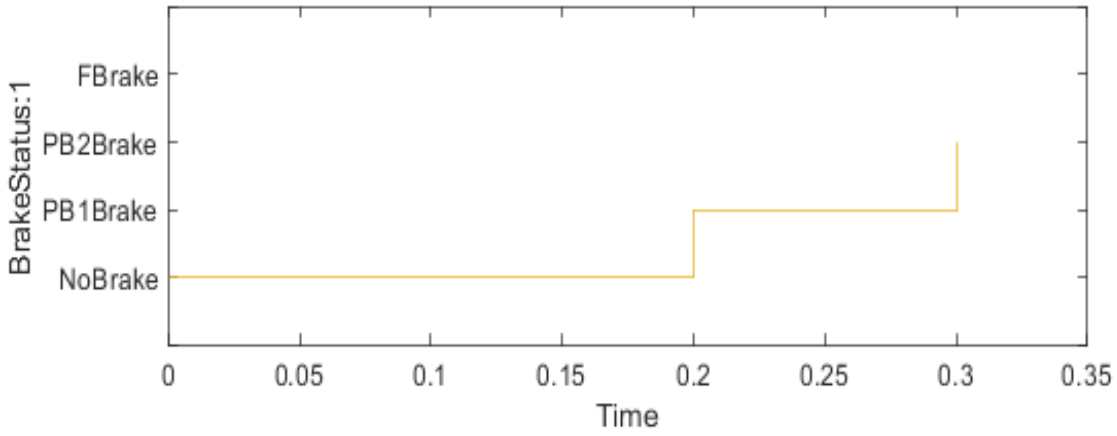
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:46
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:46
Start Time:	0
Stop Time:	0.30000000000000004
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:23
Simulation Stop Time:	2021-09-22 19:19:23
Platform:	PCWIN64

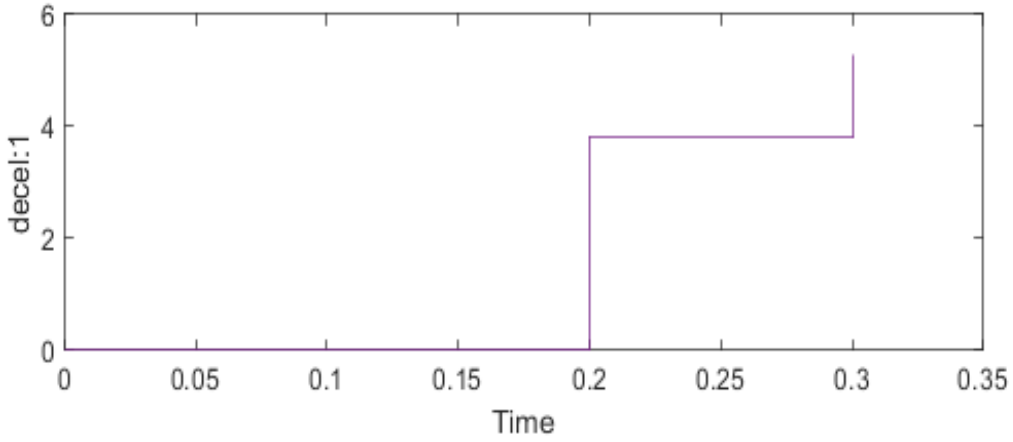
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:47

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:24
End Time:	22-Sep-2021 19:19:26
Outcome:	Passed

Test Case Information

Name:	Test Case:47
Type:	Baseline Test
Baseline Name:	TestCases_47.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_47.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:47
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_47.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

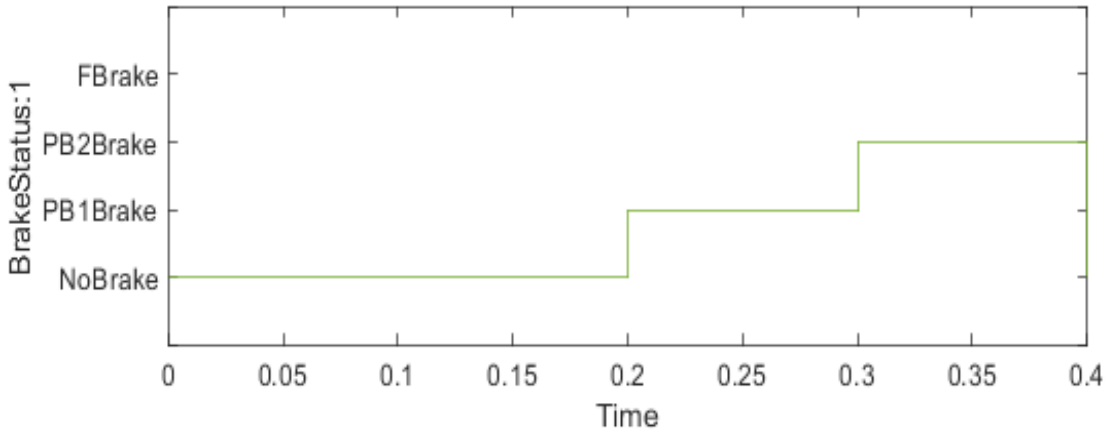
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:47
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:47
Start Time:	0
Stop Time:	0.40000000000000002
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:25
Simulation Stop Time:	2021-09-22 19:19:25
Platform:	PCWIN64

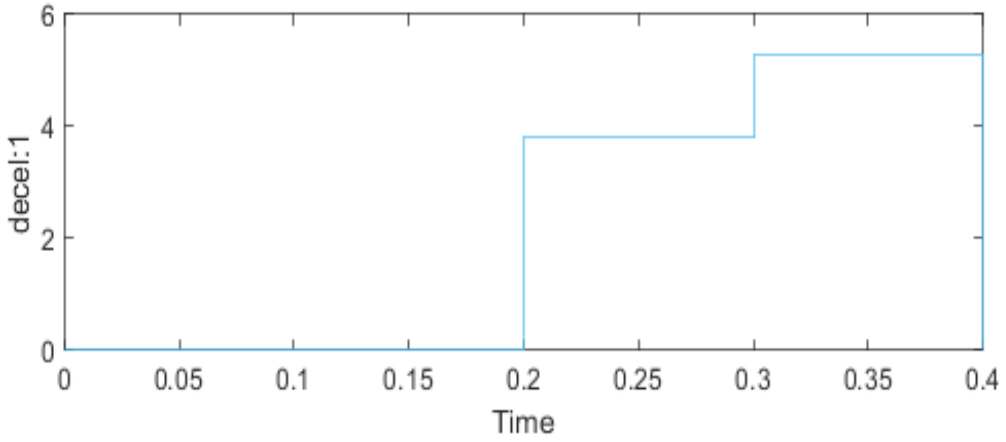
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:48

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:26
End Time:	22-Sep-2021 19:19:28
Outcome:	Passed

Test Case Information

Name:	Test Case:48
Type:	Baseline Test
Baseline Name:	TestCases_48.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_48.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:48
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_48.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

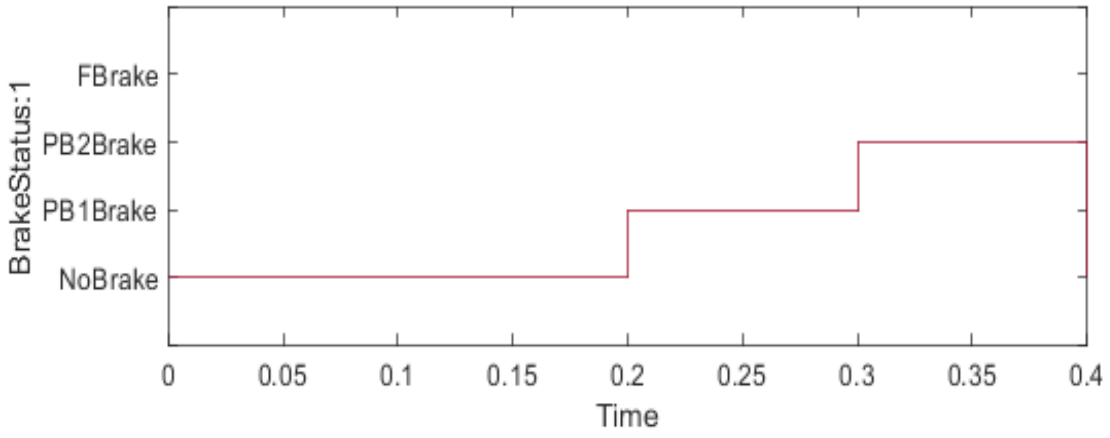
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:48
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:48
Start Time:	0
Stop Time:	0.40000000000000002
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:27
Simulation Stop Time:	2021-09-22 19:19:27
Platform:	PCWIN64

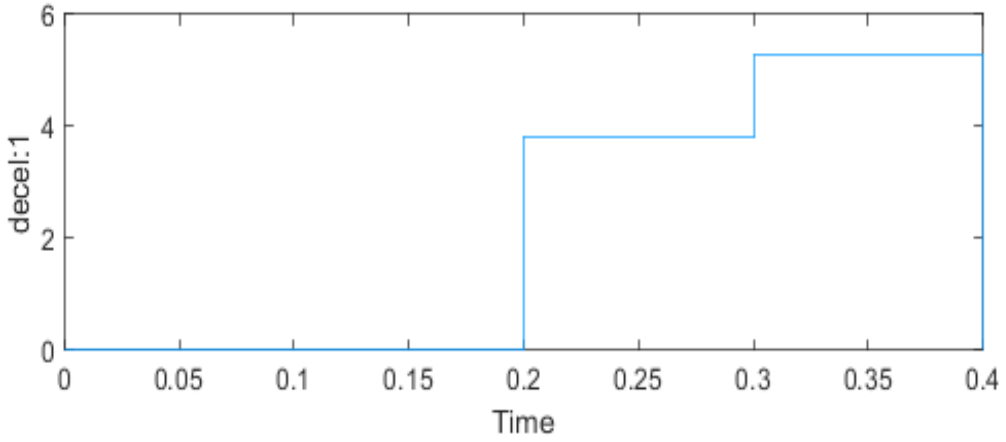
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:49

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:28
End Time:	22-Sep-2021 19:19:30
Outcome:	Passed

Test Case Information

Name:	Test Case:49
Type:	Baseline Test
Baseline Name:	TestCases_49.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_49.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:49
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_49.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

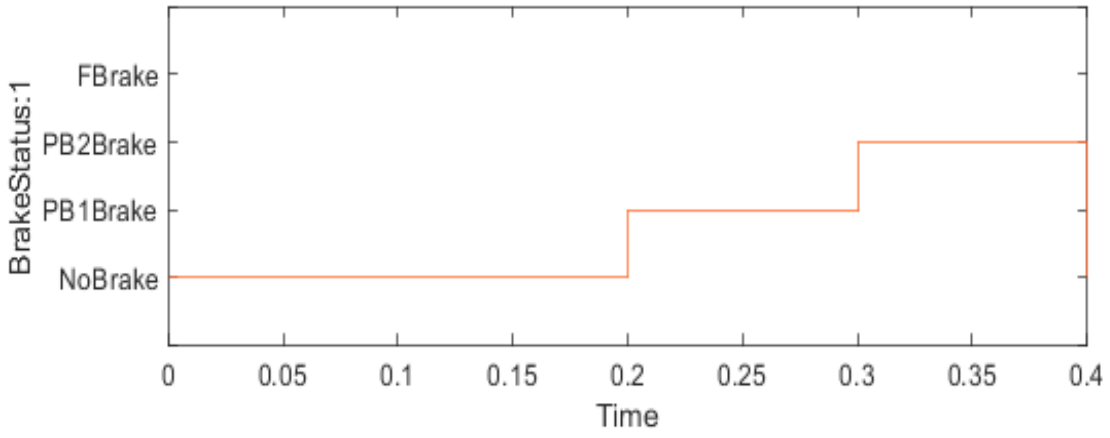
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:49
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:49
Start Time:	0
Stop Time:	0.40000000000000002
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:28
Simulation Stop Time:	2021-09-22 19:19:29
Platform:	PCWIN64

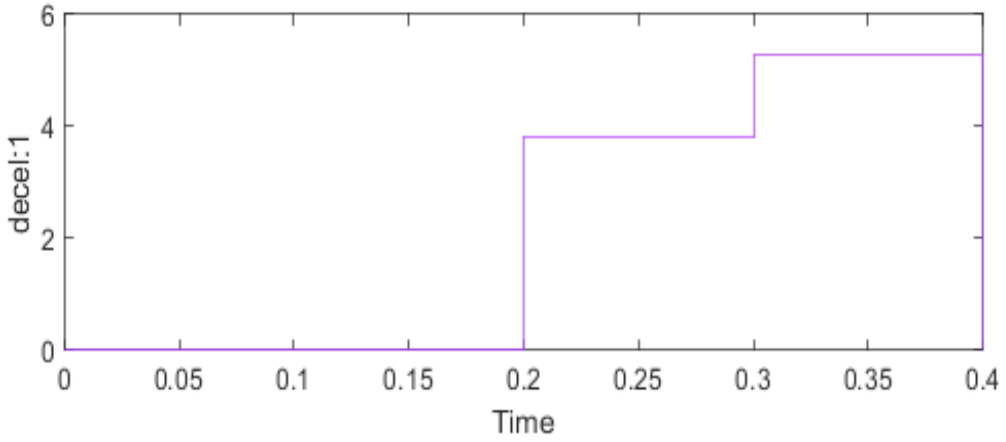
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:50

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:30
End Time:	22-Sep-2021 19:19:32
Outcome:	Passed

Test Case Information

Name:	Test Case:50
Type:	Baseline Test
Baseline Name:	TestCases_50.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_50.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:50
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_50.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

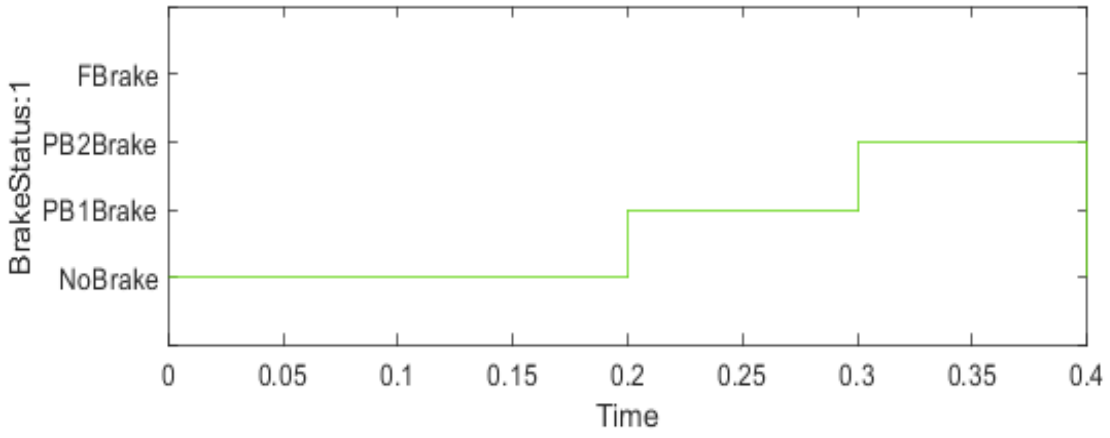
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:50
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:50
Start Time:	0
Stop Time:	0.40000000000000002
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:30
Simulation Stop Time:	2021-09-22 19:19:31
Platform:	PCWIN64

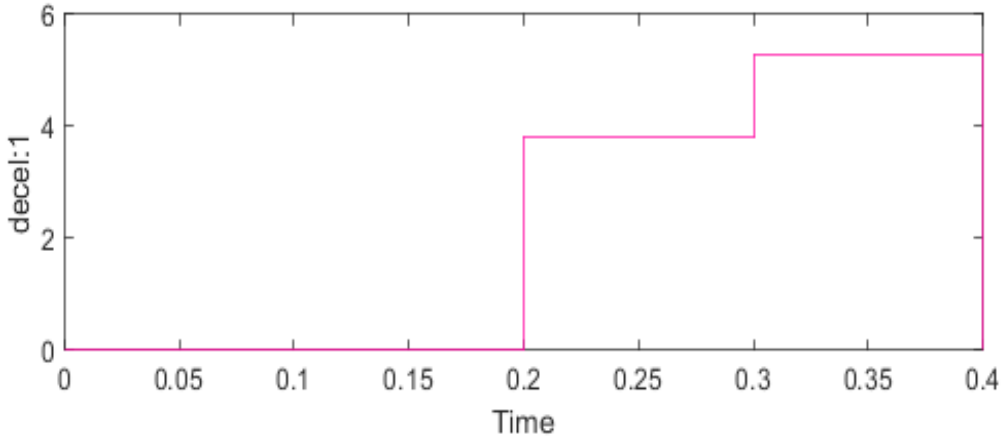
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:51

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:32
End Time:	22-Sep-2021 19:19:34
Outcome:	Passed

Test Case Information

Name:	Test Case:51
Type:	Baseline Test
Baseline Name:	TestCases_51.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_51.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:51
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_51.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

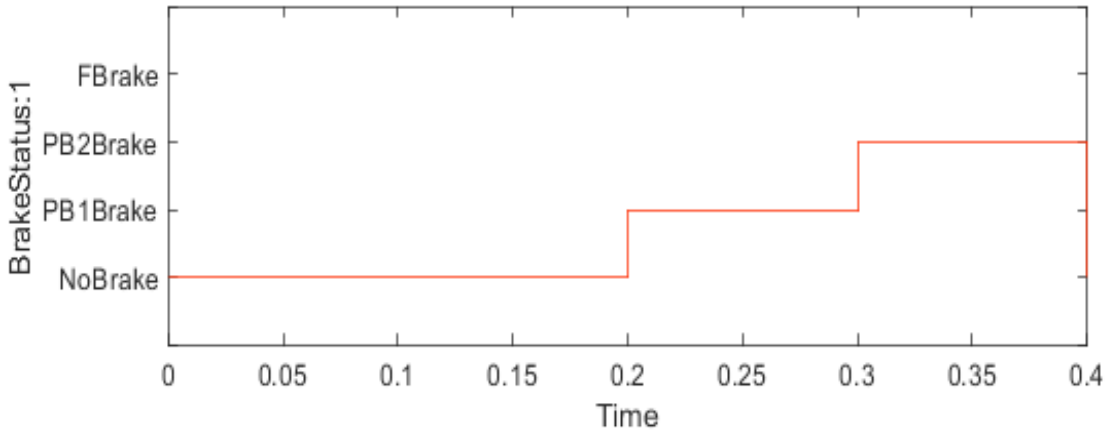
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:51
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:51
Start Time:	0
Stop Time:	0.40000000000000002
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:32
Simulation Stop Time:	2021-09-22 19:19:32
Platform:	PCWIN64

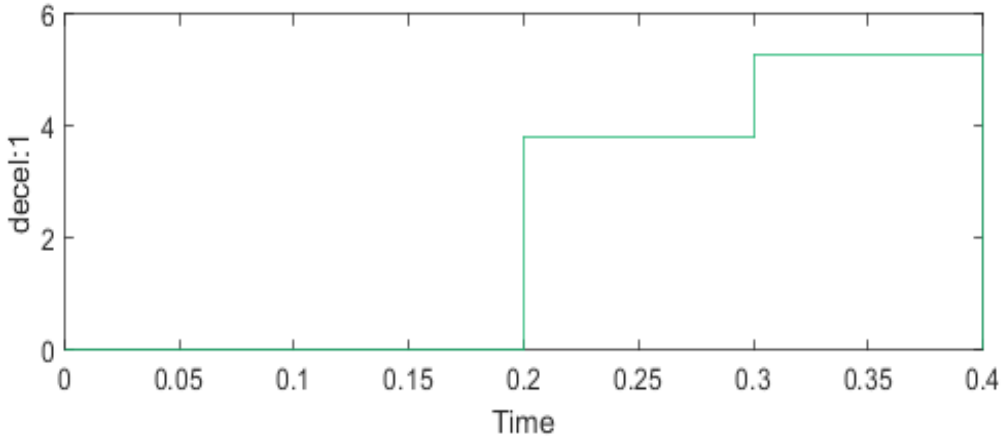
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:52

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:34
End Time:	22-Sep-2021 19:19:36
Outcome:	Passed

Test Case Information

Name:	Test Case:52
Type:	Baseline Test
Baseline Name:	TestCases_52.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_52.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:52
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_52.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

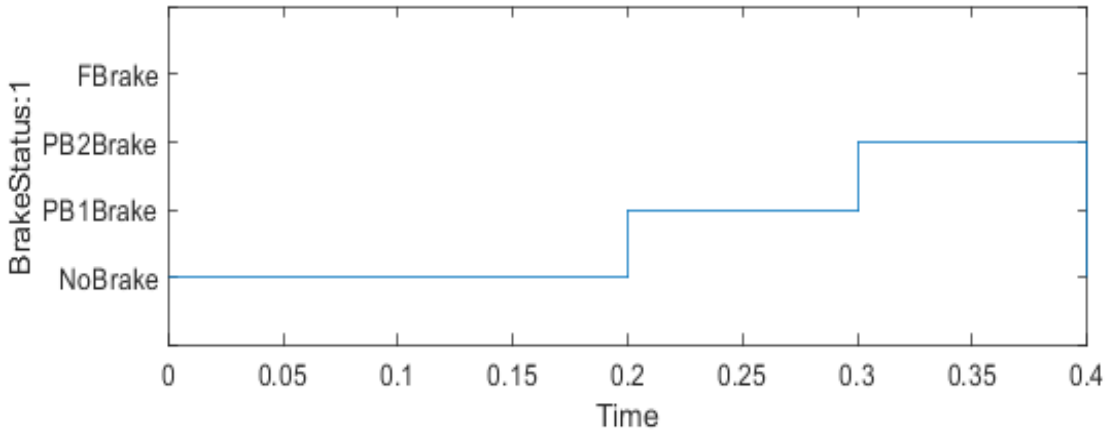
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:52
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:52
Start Time:	0
Stop Time:	0.40000000000000002
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:34
Simulation Stop Time:	2021-09-22 19:19:34
Platform:	PCWIN64

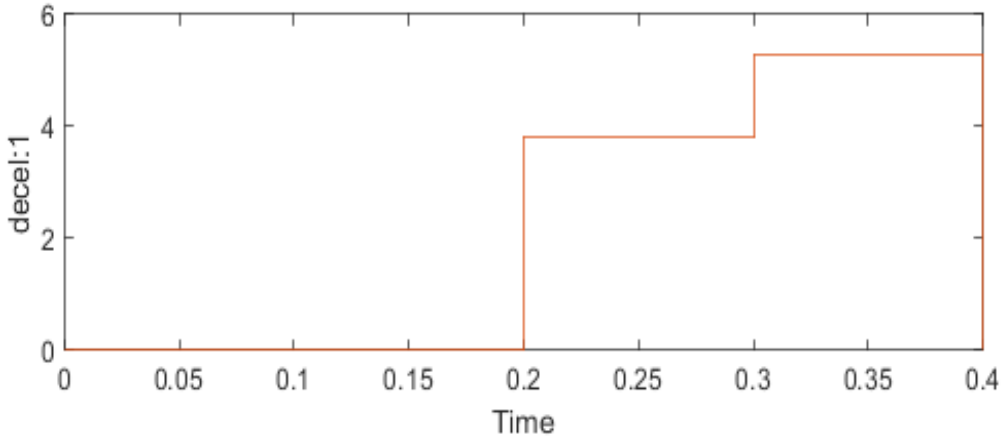
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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Test Case:53

Test Result Information

Result Type:	Test Iteration Result
Parent:	LLR_SLDV
Start Time:	22-Sep-2021 19:19:36
End Time:	22-Sep-2021 19:19:37
Outcome:	Passed

Test Case Information

Name:	Test Case:53
Type:	Baseline Test
Baseline Name:	TestCases_53.mat
Baseline File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_53.mat

Iteration Settings

Test Overrides

Parameter Name	Value
ExternalInput	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:53
Baseline	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\sl_test_baselines\TestCases_53.mat

Baseline Comparison

Name	Abs Tol	Rel Tol	Lead Tol	Lag Tol	Max Diff	Data Type 1	Units 1	Sample Time 1	Data Type 2	Units 2	Sample Time 2	Interp	Sync
BrakeStatus:1	1e-06	0.001	0	0	0	BrStatus			BrStatus		0.1	zoh	union
decel:1	1e-06	0.001	0	0	0	double			double	m/s^2	0.1	zoh	union

Simulation

System Under Test Information

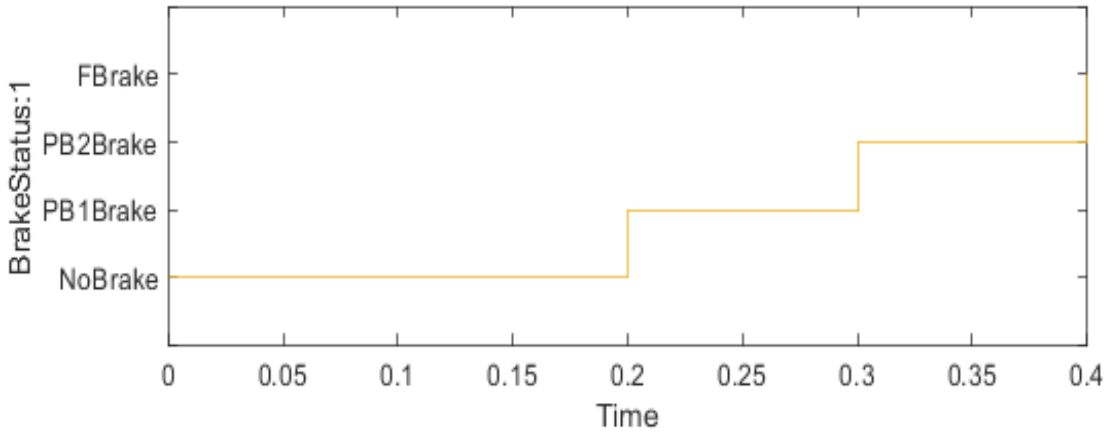
Model:	WDGBrakingLogic
Harness:	WDGBrakingLogic_Harness_SLDV
Harness Owner:	WDGBrakingLogic
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	ModelReferencing
External Input Name:	Test Case:53
External Input File:	C:\Users\mabualqu\hlf2\ISO_06_09_SwUVer\WPs\ISO_6_9_5_1_SwVerSpec\WDGBrakingLogic\WDGBrakingLogic_sldvdata.mat : Test Case:53
Start Time:	0
Stop Time:	0.40000000000000002
Checksum:	3973246956 3352263426 3523086152 321462018
Simulink Version:	10.4
Model Version:	4.3
Model Author:	mabualqu
Date:	Wed Sep 22 19:16:24 2021
User ID:	mabualqu
Model Path:	C:\Users\mabualqu\hlf2\ISO_06_08_SwU\WPs\ISO_6_8_5_1_SwUnDesSpec\WDGBrakingLogic\WDGBrakingLogic_Harness_SLDV.slx
Machine Name:	BAT917931WIN64
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2021-09-22 19:19:36
Simulation Stop Time:	2021-09-22 19:19:36
Platform:	PCWIN64

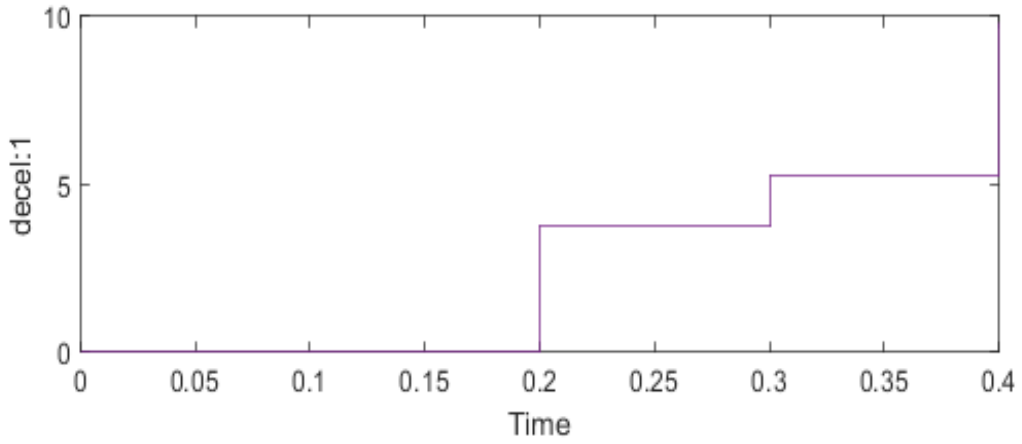
Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot

BrakeStatus:1	BrStatus		0.1	zoh	union	Link
decel:1	double	m/s^2	0.1	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
BrakeStatus:1	BrStatus		0.1	zoh	union
decel:1	double	m/s^2	0.1	zoh	union





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