

C.O & A

The systematical arrangement of physical entity is known as Architecture.

When these physical entity work together to give a desire output then it is known as organisation.

e.g.) Class room is architecture.

→ In the classroom teachers & students are organisation.

or DRAM & ROM

RAM

- Temporary storage
- Store data in MB's
- Volatile
- Used in normal operation
- Writing data is faster

ROM

- permanent storage
- Store data in MB's
- Non-Volatile
- Used for startup process of computer.
- Writing data is slower
- One-time programmable ROM (OTP)

Memory

Storage - Having the specific address.

Data stores in memory. Memories are used to store data. We cannot bring some thing for that we want to use, so we store data. So, at the time we get that particular thing.

Systematic & perfect address are stored in memory.

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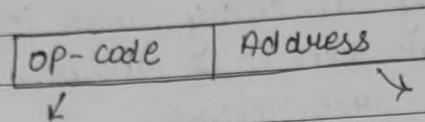
MATH
fragmentation - arrangement of storage it shows the memory.

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O.P. code - operational code

Instruction



Kya kouna hai

kis per kouna hai

To pass the details from memory to CPU is known as fetching.

RAM i.e. for fast memory we call the details. So, we get our data fast.

Places are not stored in the memory.

For the first time the memory are arranged in a systematic manner or way.

It depends on data that how the memory chunks

Type of memory

OPTICAL
Memory

e.g.
CD, DVD,
Blue Ray
disk

MAGNETIC
Memory

e.g.
HDD,
Floppy
disk

SEMICONDUCTOR
memory

e.g.
RAM ROM

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1) Optical Memory (Connected to light) → (light)

The sensation due to light is known as optical material that is found in DVD (Binary Part)
Head & write

The DVD is read by DVD player through laser.

First it search the initial point Layer touch makes marks two maps one is deep i.e. zero & other is small i.e. one

We use optical memory because it is cheap in cost.

It is cheap in cost among all the three memory

Speed is low in optical memory among all 3 memory.

Take lots of space extra power space.

On searching in (1) it does not read.

2) Magnetic Memory

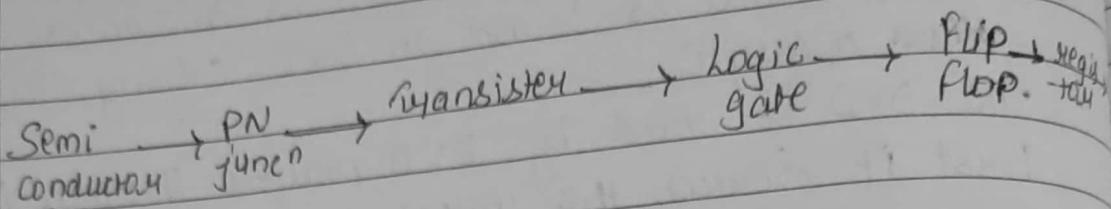
Count the magnetic field line.

Advantage

1. Faster than optical memory.
2. Durability is faster than optical memory.
3. Expensive.
4. No such phenomena.
5. Cannot take in high magnetic field like transformer A.C., otherwise it will get destroy or give an error.

Collection of registers is known as memory.

3) Semiconductor memory



It is faster memory among the three

* Memory Organisation

memory is a collection of registers
it keeps memory near itself. In memory either it stores or utilizes the memory. Storage means to assign the address of the data, memory organisation means where the data is kept.

[Complete address we will write we get the data]

fetching → address → buses

* Memory consumption

- Complexity less
- power consumption
- we can hit directly
- Speed increases
- we divide it so, that if one file is lost then others can be used

eg

Building

A B C D E

Building

10 floors

20 house

house

100

house

Only increase the memory it is not necessary that we are increasing the speed. We will do that what type of fragmentation we are doing.

more data \rightarrow more time processor will take.
eg Barati

Interrupt

maskable

cpu can ignore it)

Non-maskable

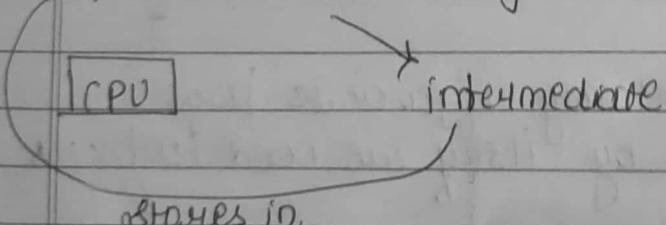
(if heating occurs then PC will shutdown)

To decreases the fetching time we does segmentation.

Therefore we divide the memory into parts

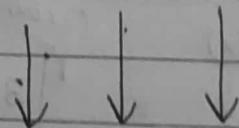
* Segmentation of memory

→ Accumulator Register (old day)



stages in.

Temporary storage \rightarrow old day \rightarrow accumulation



divided in parts

old day

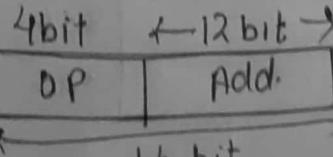
\downarrow CPU

Accumulator

\downarrow

upgrade

general purpose



defragmentation - Arrangement of file
arrange the similar type of file one
side and this create a flag.

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* COMPUTER REGISTER

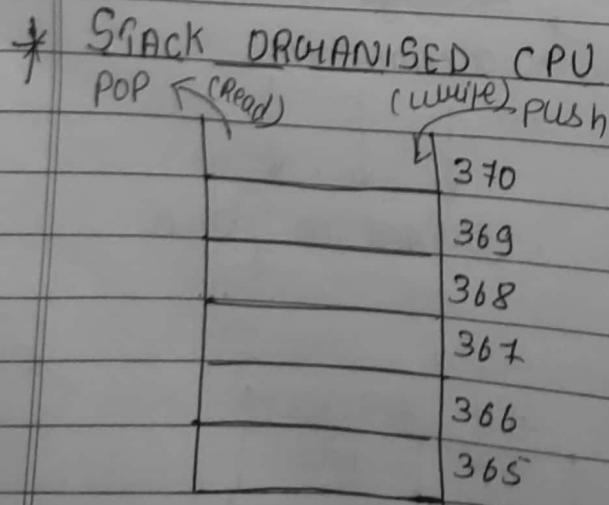
Reg. Symbol	No. of bit	Reg. Name	Function
DR	16	Data Register	Hold memory op.
AR	12	Address Register	Hold add. for mem.
AC	16	Accumulator	Processor Register
IR	16	Instruction Register	Hold instruction
PC	12	Program Counter	Hold add. of the ins.
TR	16	Temporary Register	Hold temporary
INTR	8	Input Register	Hold input char
OUTR	8	Output Register	Hold output char

It works on the basis of software that which register to be choose

Arrangement in memory is Random (like anywhere it settles down)

Eg. Train person leaves the train diff. 10 person enter the train.

In the time of similarity it generate flags
data never comes by itself we need to fix its address of the



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microinstruction - Small instruction use to increment
the function

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O/P 2 Address of the Stack pointer
direct Address can was nor necessarily it automatically
increment & decrement through Stack

* Instruction Format

A computer will usually have a variety of instruction code formats. It is the function of the control unit within the CPU to interpret each instruction code and provide the necessary control function needed to process the instruction.

The most common fields found in instruction formats are :-

- 1) An operation code field that specifies the operation to be performed.
- 2) An address field that designates a memory address or a processor register.
- 3) A mode field that specifies the way, the operand on the effective address is determine

* Addressing mode

Computers use addressing mode techniques for the purpose of accomodating one or both of the following provisions :-

- 1) To give programming versitility to the user by providing such facilities as pointer to memory, counter for loop control, indexing of data and program relocation.

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MOV A, [08H] {memory location }
MOV A, 08H {Data }

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- iii) To reduce the no. of bits in the addressing field of the instruction & reduce fetching time.
The availability of the addressing modes gives the experienced assembly language programmers flexibility for writing programs that are more efficient w.r.t no. of instruction & execution time.
- i) Immediate Addressing - eg : Add 02H, 05H
 - ii) Register Addressing.
 - iii) Direct Addressing
 - iv) Indirect Addressing.
 - v) Register Indirect Addressing.
 - vi) Relative Addressing
 - vii) Stack Addressing.
 - viii) Auto Incremental or Auto Decremental Addressing
 - ix) Implicit (Implied Add) Addressing.
 - x) Index Addressing

* Following notations are used to describe various addressing mode.

(Direct) A → contents of an address field in the instruction (OP code)

(Indirect) R → Content of an addressing field in the instruction that refers to a register (eg - Base register)

(Final add.) EA → Actual (Effective) address of the location containing the referenced operand

(X) → Content of memory location X on register (X)
eg MOV A, [08H]

* Imidiate Addressing mode

In this mode, the operand is specified in the instruction itself. An immediate mode instruction has an operand field instead of a address field.

Advantage

- 1) Low memory requirement

eg MVI B, 08H

2) Register Addressing - When a address field specifies a processor register, the instruction is in the register move.

Advantages

- 1) Only small address field needed.
- 2) No memory reference required.

Disadvantage

- 1) The address space is very limited.

eg ADD A,B

MUL AB

3) Direct Addressing - In this mode the address field of the instruction contains the effective address of operand i.e. the operand resides in memory & its address is given directly by address field of the instruction.
MOV A, [08H]

$$\left\{ \begin{array}{l} k \text{ bit for Reg add} \\ \text{No. of Reg} = 2^k \end{array} \right.$$

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Advantage -
Less fetching time

Disadvantage
Limited address space.

4.) Indirect Addressing - In this mode the address field of the instruction gives the address where the effective address is stored in memory. After fetching the instruction from memory the address part of instruction is used in the memory again to read effective address.

Advantage -
Provide large address space

Disadvantage -
It requires two or more fetch operation.

5.) Displacement Addressing

We look for the next two to see the particular address.

6.) Stack Addressing

It has systematic arrangement, auto decremental is used in stack addressing.

7) Relative Address

Address on the base of address is known relative address. we give one address through this it increments & decrements

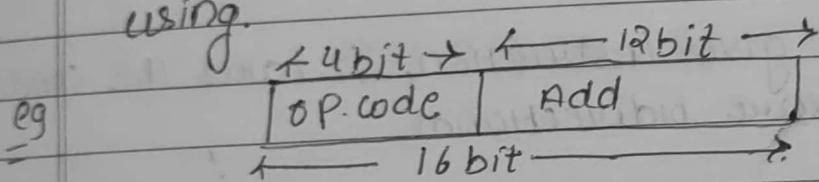
8) Implicit Address

We do not give any address. we give one data and after that it automatically increments by decrements

eg i-- or ++

9) Index Addressing

It tells that what type of addressing we are using.



1010 1110 1110 1111
we highlight index bit or digit

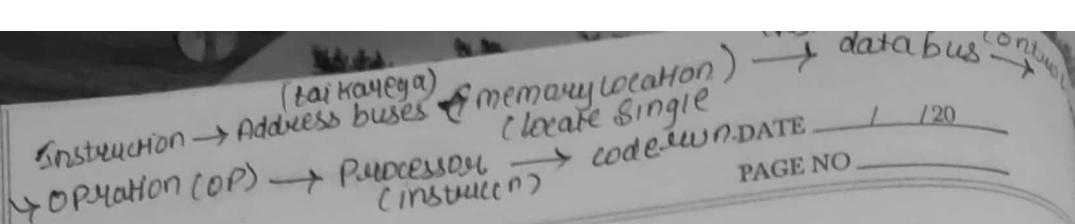
eg 0213CS181098
alg j you unique
name branch Modno

* Control Unit Organisation

When the control signals are generated by hardware using conventional logic design techniques, the control unit is said to be hardwired controlled unit.

A controlled unit whose binary controlled variables are stored in memory is called micro program controlled unit. Each word in control memory

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Contain within it a micro instruction. The micro-instruction specifies one or more operation for the system. A sequence form of microinstruction constitute a micro program. Since alteration in microprogram are not needed, once the control unit is in operation, the control memory can be a Read Only Memory i.e. ROM.

A memory i.e. Part of control unit is referred to as a control memory.

Data bus is bidirectional memory to data, data to memory.

Control buses gives instruction, it takes the condition Address bus is bidirectional

* CONTROL UNIT ORGANIZATION

When the control signals are generated by H/w using conventional logic design technique the control unit said to be hard wired control unit.

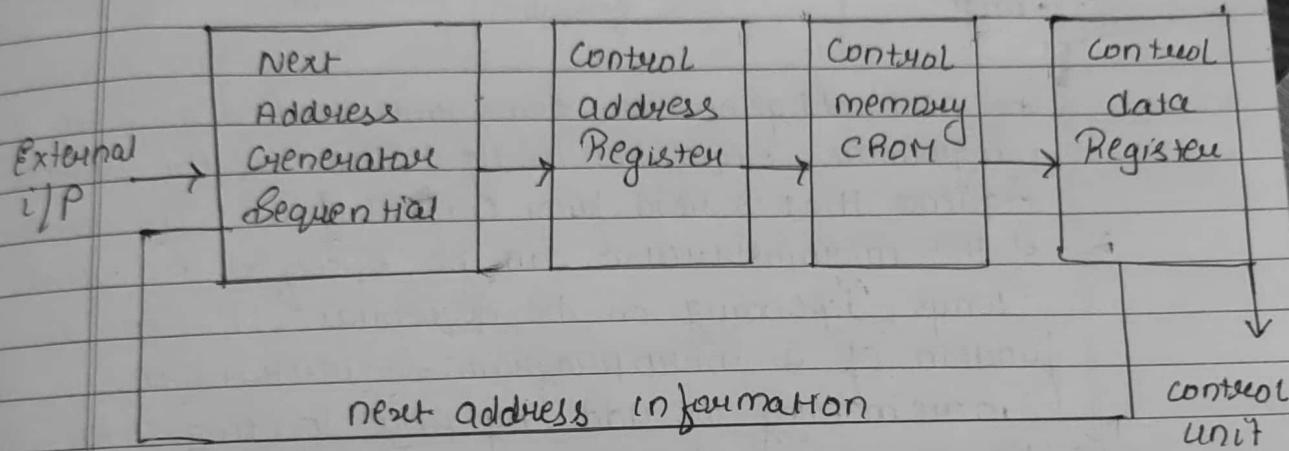
A control unit whose binary control variables are stored in ROM is called microprogram, control unit each word in control ROM contains within it a microinstruction.

The microinstruction specify the one or many micro operation perform for the system. A sequence of micro operation constitute a micro program. Since alteration of micro program are not needed once the control unit is in operation, the control ROM can be a Read Only ROM.

External i/p

A memory that is part of control unit is referred to as a control memory

Microprogram Control Organization:-



This is general configuration of micro program control unit. The control m/u is assume to be a ROM within which all control information is permanently stored. The control m/u add Register specify the add the micro instruction & the control Register data holds

The micro instruction read from the memory the micro instruction contain a control that specify one or more micro operation for the data processor once this operation are executed the control must determine the control add, the location of next micro instruction may be the one in sequence or it may be located some where as in the control m/u for this reason it is necessary to use some bits of present micro instruction control the generation add of the next micro instruction of external i/p condition

Address bus → two way } bi addition
data bus → two way }
Control bus → unidirectional - given DATE / / 120
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while the micro operation the executed

Thus a microinstruction contains bits for initiating microoperation in the data processor part & bits that determine that the add sequence for the control MUX.

The next add generator sometimes called a microprogramme Sequential as it determines the address sequence that is read from control MUX. The address of the microinstruction can be specified in several ways, depending on the sequential I/P typical function of a microprogram Sequential are incrementing the add by one loading into the control add register (CAR) and get add from control MUX & transferring add on loading & initial add to start the control operation.

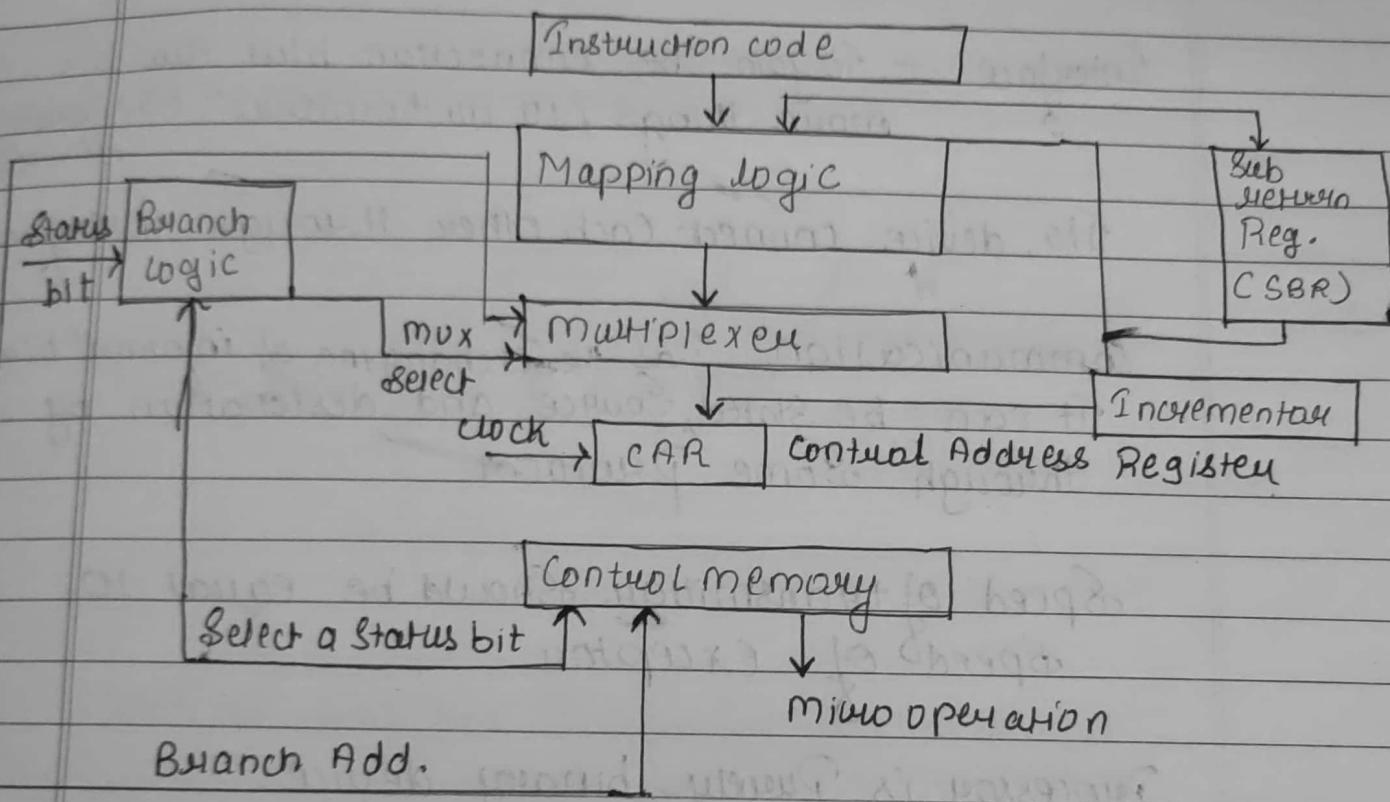
The control data register holds the present micro instruction while the next add is computed and read from the MUX the data Register is some lines called a pipeline Register. It allows the execution of microoperation specify by control word simultaneous with the generation of next micro instruction. The configuration is require two phase clock, with one clock applied to the add register & the other data register.

instruction $\xrightarrow{\text{mapping}}$

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Selection of Address in Control M/M :-



Mapping

The transformation from the instruction code bits to an add in control m/m where the routine is located to as mapping Process

Routine

Sub Routine are program that are used by there routine to accomplish any a within the main body of the micro program

UNIT - 3

INPUT OUTPUT ORGANIZATION

Interface - to join the connection b/w two or more things / to do the interaction b/w peripheral devices

To device connect each other through interface

Communication : as the exchanging of information b/w source and destination by through some protocol

Speed of transmission should be equal to speed of exception

Processor is purely binary device.

Digital form of information is known as data

Keyboard works on ASCII code

$2^8 = 256$. ~~the~~ it has to work including Printable (Alphabets) & non-Printable (Spacebar, Shift, Ctrl).

IEEE → Institute of Electrical & Electronic Engineering.

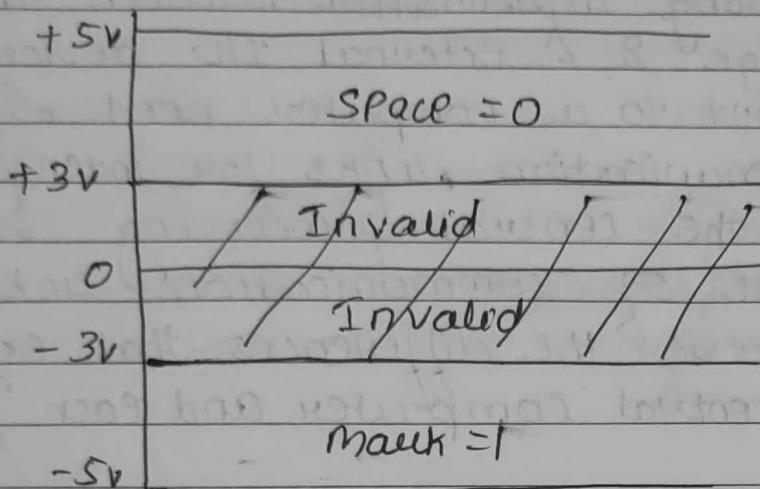
According to IEEE the devices we are using are Universal Serial Bus (USB)

Switz watches are world's best watches bcz they are handmade & found in Switzerland.

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IEEE Standard 8732 states that if it lies b/w +3V to +5V then it is "Space" 0 & if it is -3V to -5V then it is 1



We need clock for Synchronization

Where we use clock is known as Synchronous communication

& where the clock is not use is known as asynchronous communication

Synchronous System are costly

Synchronous System requires more Power requirement
Asynchronous System are used for time boundation

Sender → Receiver
(if received then
valid data)

* Input Output Interfaces

Input output interface provide a method for transferring information between internal storage & external I/O devices. Peripheral connected to a computer need special communication links for interfacing them with the central processing unit. The purpose of communication link is to resolve the differences that exist between the central computer and each peripheral.

The major differences are:

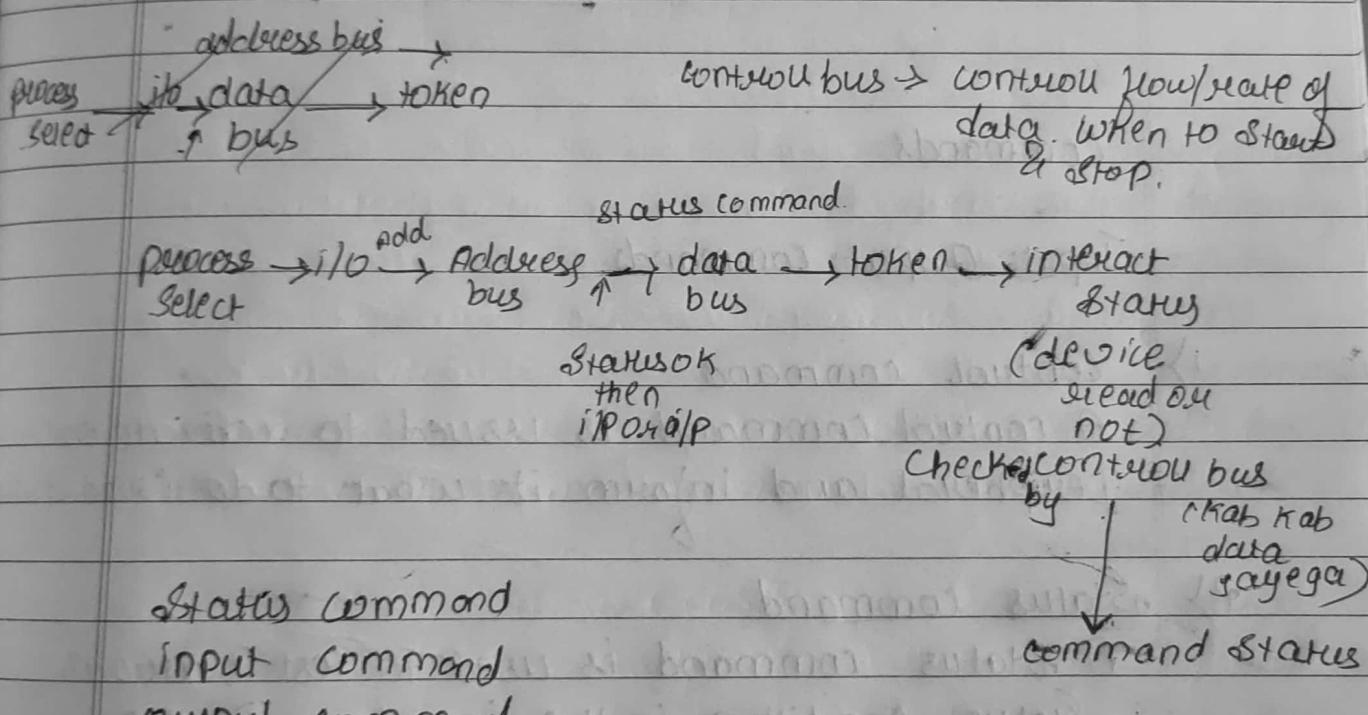
- 1) Peripherals are electro mechanical & electro magnetic devices & their manner of operation is different from the operation of the CPU and memory, which are electronic devices. Therefore, a conversion of signal values may be required.
- 2) The data transfer rate of peripheral is usually slower than the transfer rate of CPU, and consequently, a synchronization mechanism may be needed.
- 3) Data codes and formats in peripherals differ from the word format in CPU & memory.

There is no common interfacing unit for all differ
[all have their own interfacing devices]
Eg. ~~no~~ printer will ~~any~~ print

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4. The operating mode of peripherals are different from each other and each must be controlled so as not to disturb the operation of other peripherals connected to the CPU.

To resolve these differences, computer system include special hardware components b/w the CPU & peripheral to supervise & synchronize all input & output transfers. These components are called interface units.



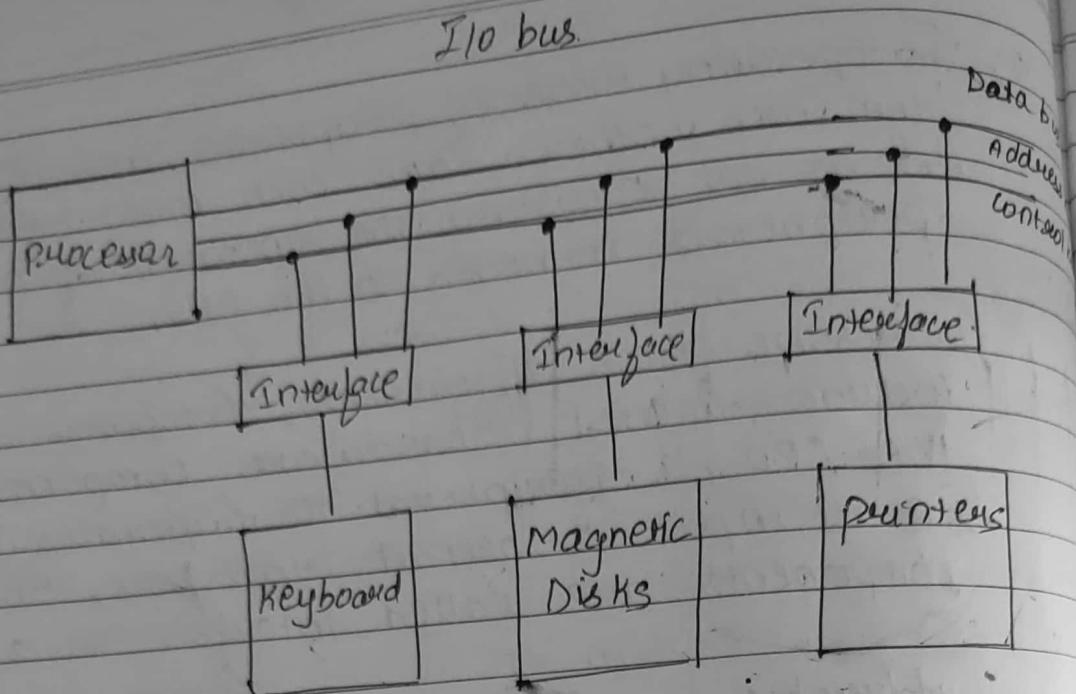
CPU put megway watch in the communication
It checks the status continuously.

driver → Software files
interface → Hardware files

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input - w
OLP - read

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Commands

Input output commands

1) Control command

A control command is issued to activate the peripheral and inform it what to do. (Read & Write)

2) Status command

A status command is used to test various status condition in the interface & the peripherals.

3) Data Output command

The data output command causes the interface to respond by transferring data from the bus into one of its registers.

- 1) Data
2)
3)
4)
5)
6)

4.1 Data input command

The data input command is opposite to data output command. In this case the interface receive an item of data from peripheral & place it in the buffer register.

There are 3 ways that computer buses can be used to communicate with memory and inputoutput devices.

- 1) Use two separate buses , One for memory & other for i/o. : (IOP)

In this system the computer has independent set of data, address, control busses , One for accessing memory & other for accessing i/o's. This is done in computers that provide a separate i/o processor (IOP).

In addition to the central processing unit. The memory communicates with both the CPU & the IOP through memory busses. The IOP communicate also with the I/P & O/P devices through a separate, I/P O/P bus with its own address, data & control lines. The purpose of the IOP is to provide an independent pathway for the transfer of information b/w external devices & internal memory. The IOP is sometimes called as data channel.

DMA - Direct Memory Access

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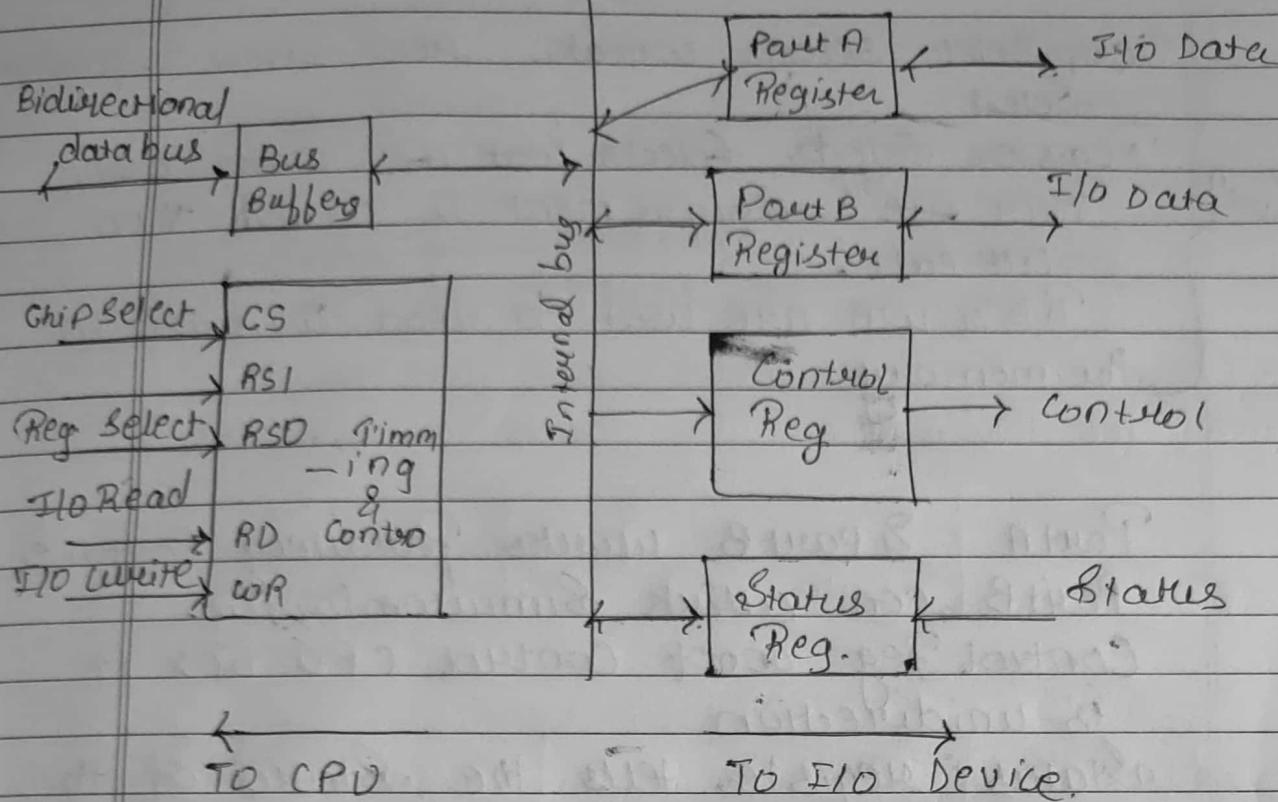
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- 2.) use one common bus for both memory and input output but have separate control lines for each. (isolated i/o method)

The isolated i/o method Many computers use one common bus to transfer information between memory or input output & the CPU. The distinction b/w the memory transfer & I/O/p transfer is made through separate read and write lines. The CPU specifies whether the address on the address line is for the memory word or for a interface register by enabling one of the two possible read or write line. The i/o read & i/o write control lines are enabled during a I/P O/P transfer. The memory read & memory write is enable for memory transfer. This configuration isolates all i/o interface addresses from the addresses assign to the memory & is referred as an isolated i/p o/p method.

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Basic diagram for I/O devices

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Buffers are used for speed mismatch.
data buffers are used to provide delay.

Buffers are used to provide delay.

latches are used to slow down the speed.

e.g. Juki Thela (Speed mismatch)

latch → fix delay (if 20 min means 20 min)
flip flop → when we want delay then only it will be stop.

over run error → latest data we take but not the lower one. i.e. in Juki when we have one then in the place the upper Juki we take & lower one still.

10/02/2020

chip select selects where. read select on write
Select

CPU internal
Registers Selects Selects work one make when
every the requirement is needed then
we call.

RD & WR are used to read & write in
the memory

Port A & Port B. works Parallelly Port A &
Port B can work Simultaneously.
Control Reg don't control CPU bcz it
is unidirectional

Status register tells the status of the
CPU. then only it works as an
interface otherwise not.

e.g.) \rightarrow Signals Green (available) & red (block)

All are integrated circuits i.e. including timing

* Asynchronous Data Transfer
 \rightarrow Strobe Control
 \rightarrow hand shaking

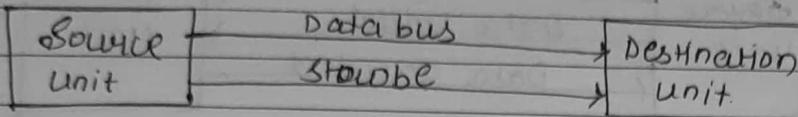
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Timing diagram shows when the light is high & when it is low

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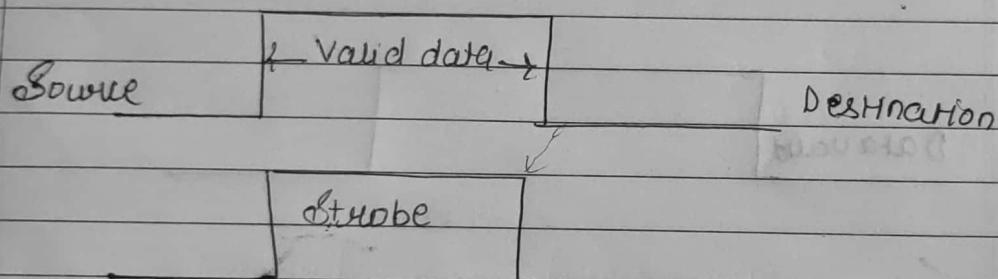
1) Strobe

→ Source initiated

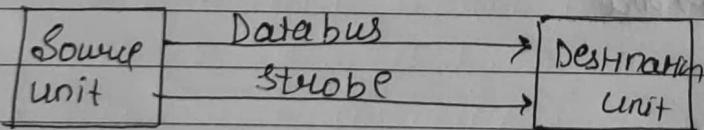


CPU will only allow when the data is valid i.e. it allows valid data.

Timing Diagram

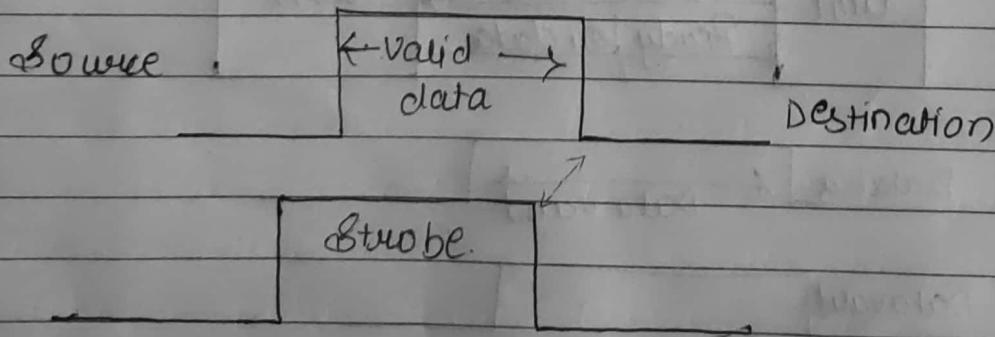


→ Destination initiated

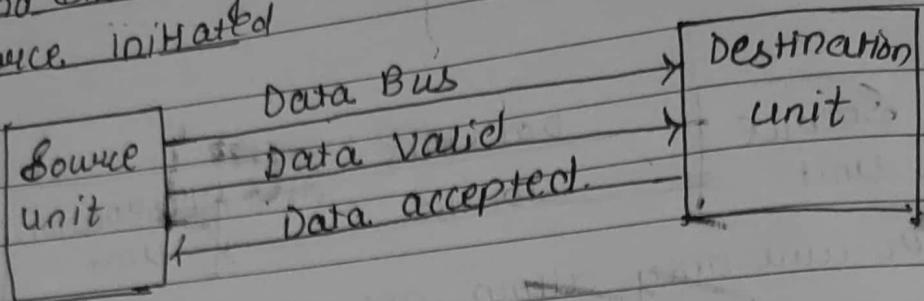


Time

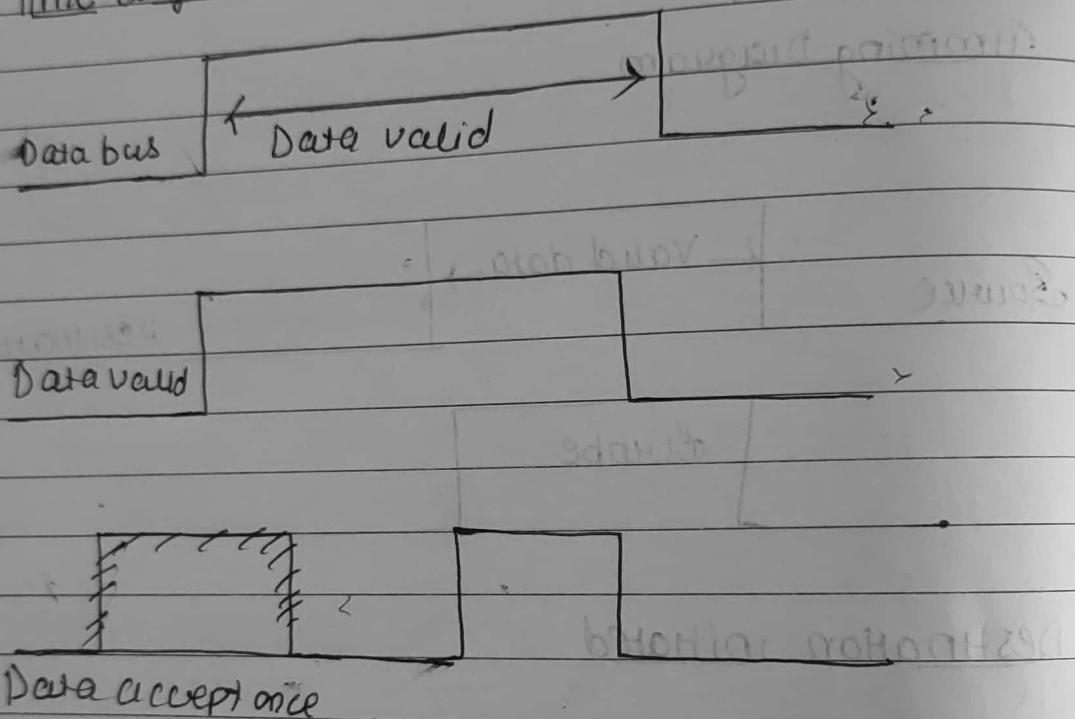
Time diagram



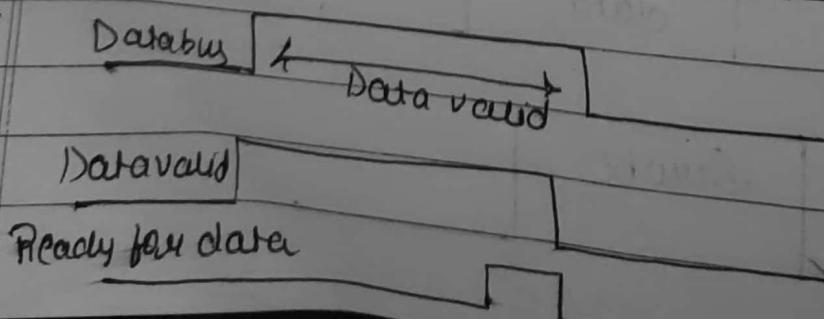
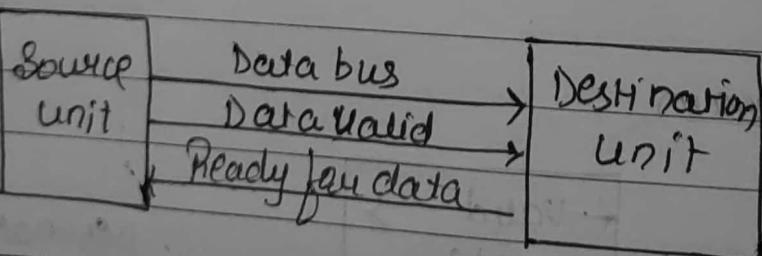
2) Hand Shaking Source initiated



Time diagram



→ Destination initiation



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Parity - bit means signal of 1 & 0 (counting the nos. if even then even parity. DATE 1/20)

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Starts \rightarrow data valid \rightarrow Stop.

* Asynchronous Serial transfer.

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e.g. pointer, procedure

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3) Direct Memory Access (DMA)