VLSI PROJECT REPORT

DESIGN OF 2:4 DECODER USING CMOS AND TRANSMISSION GATE LOGIC

Submitted To:

Prof. Neeta Pandey

Submitted By:

Ankush Chaursiya

2K21/EC/35

Ankit Nain

2K21/EC/31

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Ankush Chaursiya & Ankit Nain

ABSTRACT

In this study, we explore the design and implementation of a 2:4 decoder circuit, a fundamental building block in digital systems. The decoder converts a 2-bit input into a 4-bit output, enabling address decoding, data selection, and control signal generation.

The 2:4 decoder is essential for memory addressing, multiplexing, and demultiplexing tasks. We investigate two distinct logic families for its realization: **CMOS (Complementary Metal-Oxide-Semiconductor)** and **Transmission Gate logic**.

CMOS Logic Design

- We begin by designing the 2:4 decoder using CMOS technology.
- CMOS offers low power consumption, high noise immunity, and scalability.
- The circuit comprises NAND gates and inverters to generate the four output signals based on the input address lines.

Transmission Gate Logic Design

- Next, we explore the implementation using Transmission Gate logic.
- Transmission Gates (TGs) are bilateral switches that allow bidirectional signal flow.
- We construct the 2:4 decoder using TGs to achieve efficient data routing and reduced propagation delays.

Comparison and Trade-offs

- We compare the two designs in terms of:
    - **Area**: CMOS typically requires more transistors, leading to larger area.
    - **Speed**: TGs exhibit faster switching due to their bidirectional nature.
    - **Power Consumption**: CMOS consumes less static power, while TGs may dissipate more dynamic power during switching.
    - **Robustness**: CMOS provides better noise immunity.
- Trade-offs between area, speed, and power guide the choice of logic family based on specific application requirements.

Experimental Results

- We simulate both designs using industry-standard tools (such as SPICE or Verilog).
- Performance metrics include delay, power consumption, and area.
- Comparative analysis reveals insights into the strengths and weaknesses of each approach.

INTRODUCTION

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device that is widely used for switching purposes and the amplification of electronic signals in electronic devices. A MOSFET is either a core or integrated circuit designed and fabricated in a single chip because the device is available in very small sizes. The introduction of the MOSFET device has brought a change in the domain of switching in electronics.

Basic Components:

CMOS circuits are built using two fundamental transistor types: P-type Metal-Oxide-Semiconductor Field-Effect Transistors (PMOS) and N-type Metal-Oxide-Semiconductor Field-Effect Transistors (NMOS). These transistors form the building blocks for creating complex digital logic.

How PMOS and NMOS Work:

PMOS transistors act as switches that are closed when the input voltage is low (0 V) and open when the input voltage is high (5 V).

NMOS transistors behave similarly but in reverse: they are closed when the input voltage is high and open when it is low. The key idea is to combine PMOS and NMOS transistors such that there is never a conducting path from the supply voltage (5 V) to ground. This property minimizes energy consumption.

CMOS Logic Gates:

CMOS logic gates are designed using complementary pairs of NMOS and PMOS transistors.

For example, an NMOS-based switch is ON when the gate-to-source voltage is high (logic 1) and OFF when it is low (logic 0).

Conversely, a PMOS-based switch is ON when the gate-to-source voltage is low (logic 0) and OFF when it is high (logic 1).

Symbolic Representation:

The symbols for NMOS and PMOS transistors are depicted as switches with movable contacts controlled by gate voltages.

NMOS switches are normally open (closed for logic 1), while PMOS switches are normally closed (open for logic 1).

NMOS and PMOS Symbols

Advantages of CMOS:

Low Power Consumption: CMOS circuits consume minimal energy because power dissipation occurs only during switching.

High Noise Immunity: CMOS is robust against noise and interference.

Compatibility: CMOS devices can interface with various integrated circuits.

Fan-Out: CMOS gates can drive multiple inputs (fan-out) without signal degradation.

Fabrication Process:

Substrate Selection:

We start with a silicon wafer as our substrate. The choice of substrate type (P-type or N-type) depends on the desired CMOS technology (N-well or P-well).

Creating Well Regions:

For N-well CMOS: A P-type substrate is used. An N-well (region with N-type doping) is created by implanting or diffusing phosphorus atoms into the substrate.

For P-well CMOS:

An N-type substrate is used. A P-well (region with P-type doping) is formed by implanting or diffusing boron atoms into the substrate.

Growing Oxide Layers:

A thin layer of silicon dioxide (SiO_2) is grown on the wafer surface. This oxide layer acts as an insulator and protects the underlying silicon during subsequent processing steps.

Photolithography and Etching:

A photoresist layer is deposited on the oxide. UV light is used to expose specific regions through a mask. Etching removes the exposed oxide, defining active areas for transistors.

Transistor Formation:

PMOS and NMOS transistors are created side by side. Gate oxide (ultra-thin SiO_2) is grown. Polysilicon (doped silicon) is deposited and patterned to form gate electrodes. Source and drain regions are implanted or diffused using appropriate dopants (boron for PMOS, phosphorus for NMOS).

Metal Layer Deposition and Patterning:

A metal layer (usually aluminum or copper) is deposited. Photolithography defines metal interconnects (wires) that connect transistors. Etching removes excess metal, leaving the desired pattern.

Dielectric Layer Deposition:

Insulating layers (dielectrics) are deposited between metal layers. These prevent short circuits and provide isolation.

Via Formation:

Vias (holes) are etched through the dielectric to connect metal layers vertically. Contacts are formed at the bottom of vias to link transistors to metal lines. Back-End-of-Line (BEOL) Processing:

Additional metal layers, dielectrics, and vias are added. Interconnects become more complex, allowing signal routing across the chip.

Passivation and Packaging:

A protective layer (passivation) covers the chip. Bond pads are exposed for wire bonding or flip-chip attachment. The chip is cut into individual dies and packaged.

Comparison with Other Logic Families:

CMOS vs. TTL (Transistor-Transistor Logic): CMOS consumes less power and offers higher fan-out.

CMOS vs. ECL (Emitter-Coupled Logic): CMOS is compatible with various ICs, while ECL has faster switching speeds.

PASS TRANSISTOR CIRCUIT

In conventional logic families, input is applied to the gate terminal of the transistor but in PTL it is applied to the source/drain terminal. Here the width of PMOS is taken equal to NMOS so that both transistors can pass the signal simultaneously in parallel. Signal degradation occurs in pass transistor logic.

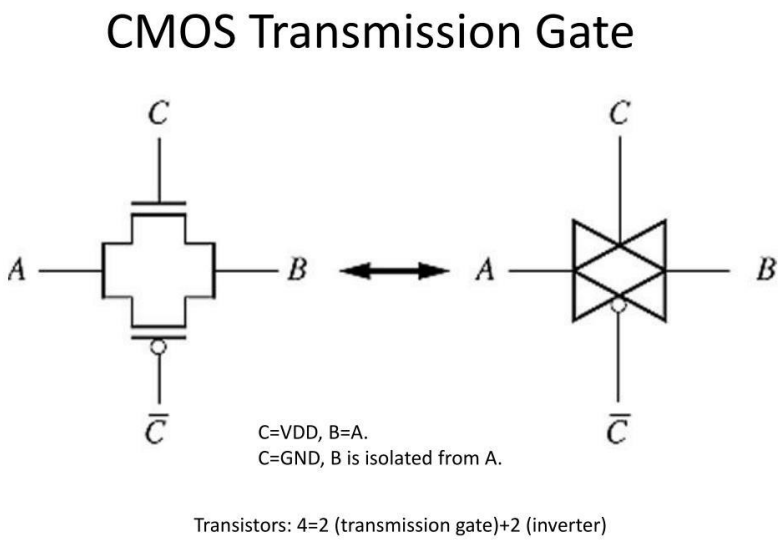
The main advantages of pass transistors are fewer devices to implement the logical functions as compared to CMOS. When control signal g=1 and input s=0 then we get d=0. If the input s=1 then we get degraded output d. Thus, NMOS pass transistors are called Poor 1 and good 0 switches. The diagram is shown in fig below.

NMOS Logic Gate

When control signal g=0 and input s=0 then we get degraded output d. If the input s=1 then we get d=1. Thus, PMOS pass transistor is called Poor 0 and good 1 switch, the diagram is shown in fig below.

PMOS Logic Gate

TRANSMISSION GATE LOGIC



Transistors: 4=2 (transmission gate)+2 (inverter)

The Need for Transmission Gates:

Traditional pass transistor logic (such as simple NMOS or PMOS switches) suffers from voltage drop issues. NMOS devices pass a strong '0' but a weak '1,' while PMOS transistors pass a strong '1' but a weak '0.' Transmission Gate Logic solves this problem by combining the best of both worlds.

Basic Structure:

The fundamental structure of a transmission gate consists of an NMOS transistor in parallel with a PMOS transistor. These transistors act as complementary switches, enabling bidirectional signal flow. The control signals to the transmission gate (usually denoted as 'C' and '—C') are complementary to each other.

Working Principle:

When the gate signal 'C' is high (1), both NMOS and PMOS transistors are ON.

The signal passes through the gate (i.e., output A = input B) when ‘C’ is 1. When ‘C’ is low (0), both MOSFETs are cut off, creating an open circuit between nodes A and B.

Symbol and Control Signals:

The transmission gate is symbolized as shown below, controlled by switching signals ‘X’ and ‘X*’ applied to the gates of NMOS and PMOS, respectively.

Applications:

Multiplexers: Transmission gates are useful for selecting between multiple inputs. XOR (exclusive OR) gates: They play a role in XOR circuit implementations.

Advantages:

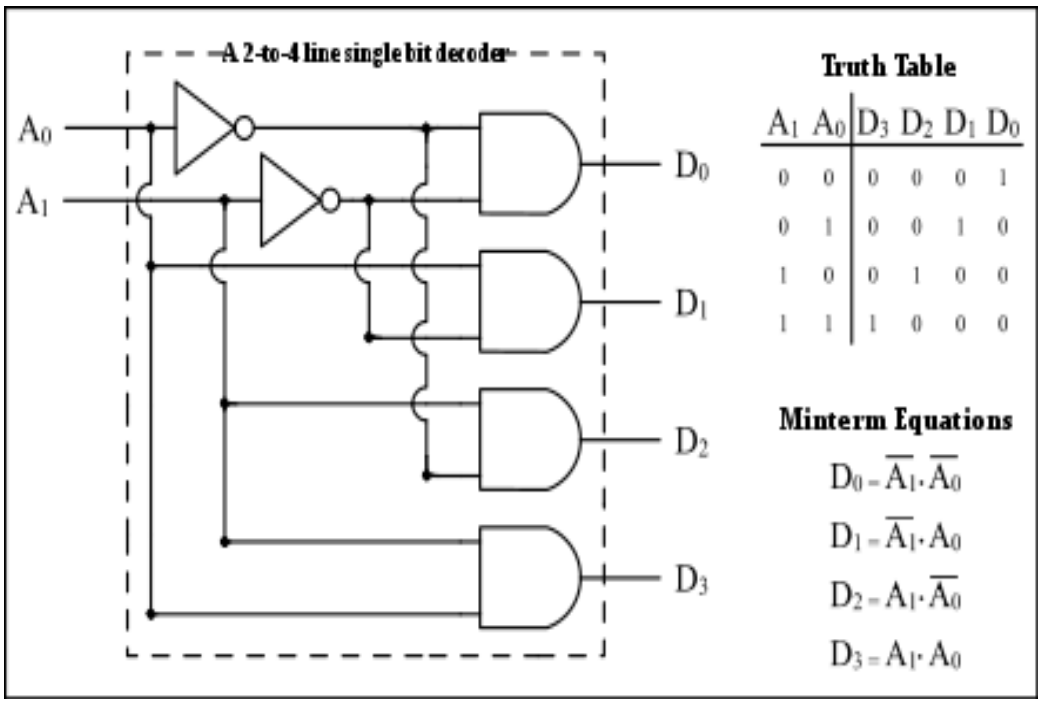
Low Voltage Drop: Transmission gates minimize voltage drop due to their complementary behaviourC.

Bidirectional Flow: They allow signals to flow in both directions.

Efficient Switching: Faster switching due to parallel NMOS and PMOS operation.

DECODER

The encoders and decoders play an essential role in digital electronics, encoders & decoders are used to convert data from one form to another form. These are frequently used in communication systems such as telecommunication, and networking, to transfer data from one end to the other end. Similarly, in the digital domain, for easy transmission of data, it is often encrypted or placed



within codes, and then transmitted. At the receiver, the coded data is decrypted or gathered from the code and is processed to be displayed or given to the load accordingly.

The decoder is an electronic device that is used to convert digital signal to an analogue signal. It allows a single input line and produces multiple output lines. The decoder allows N- inputs and generates 2 power N-numbers of outputs. For example, if we give 2 inputs that will produce 4 outputs by using 4 by 2 decoders.

Working Principle of 2:4 Decoder

The 2:4 decoder's working principle can be explained using a simplified circuit diagram. It consists of AND gates and NOT gates combined in a specific arrangement. Here's how it works:

- Each input line (A and B) is connected to one input of all the AND gates.
- The other input of each AND gate is connected to the complement of the corresponding input line.
- The outputs of the AND gates are connected to the output lines (Y0, Y1, Y2, and Y3).

This arrangement ensures that each output line is activated when the corresponding input combination is detected. When an input line is low (0), its complement becomes high (1), and the corresponding AND gate outputs a low signal (0), regardless of the other input. As a result, only one output line is activated at a time, based on the input combination

Applications of 2:4 Decoder

The 2:4 decoder finds applications in various digital systems and circuits:

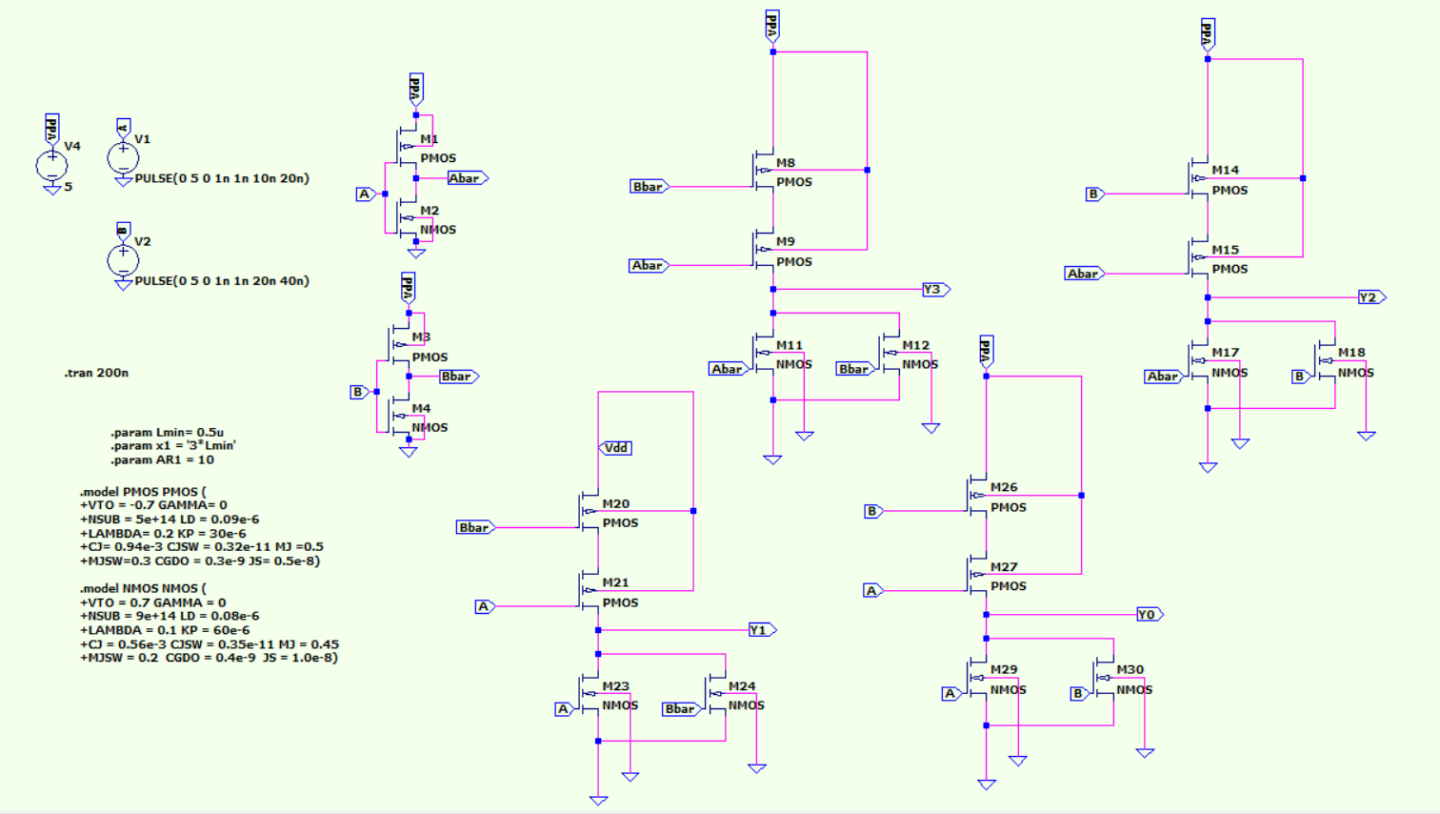
Address Decoding: In computer memory systems, a 2:4 decoder is used to decode memory addresses. It selects the appropriate memory bank based on the address lines.

Display Multiplexing: In display systems, a 2:4 decoder is used for multiplexing. It allows efficient switching between different display segments.

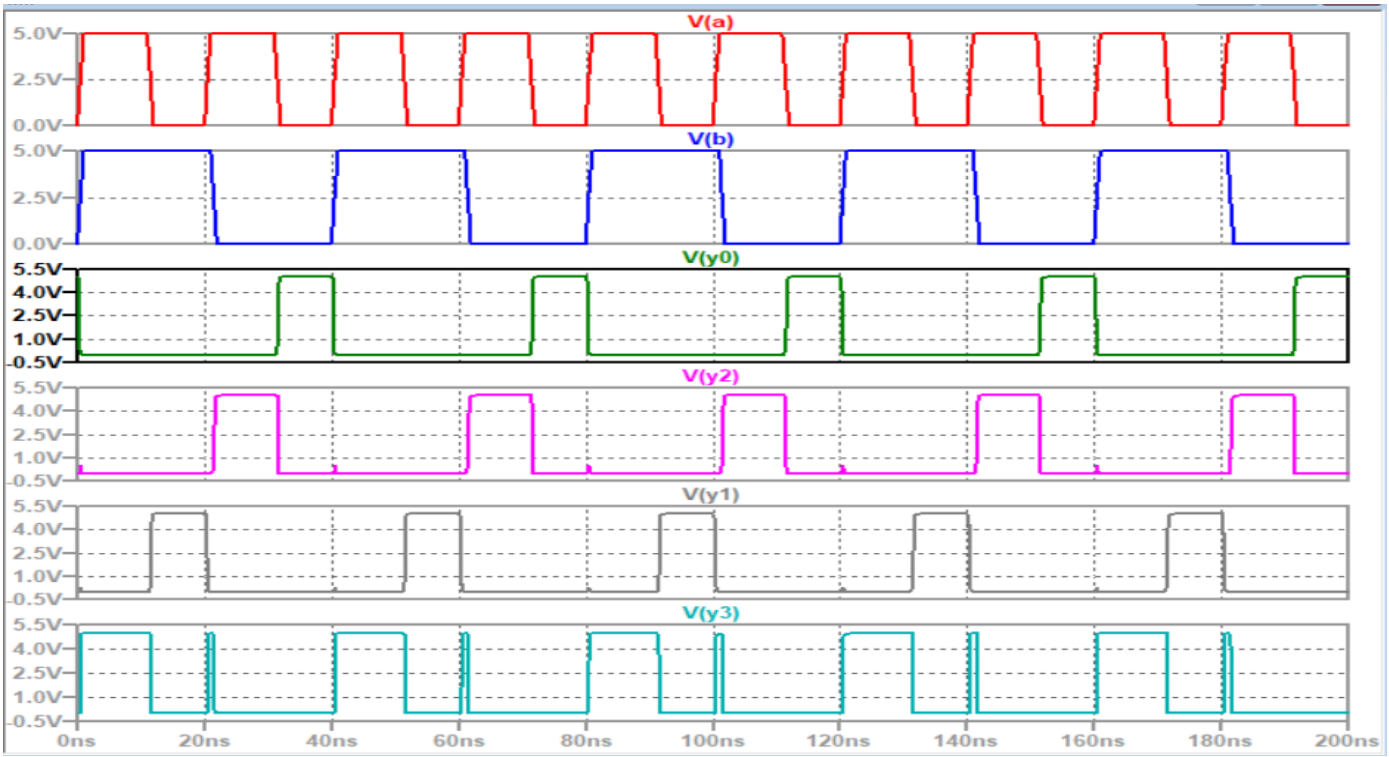
Data Routing: The 2:4 decoder can route data selectively to different output lines based on the input combination.

EXPERIMENTAL WORK

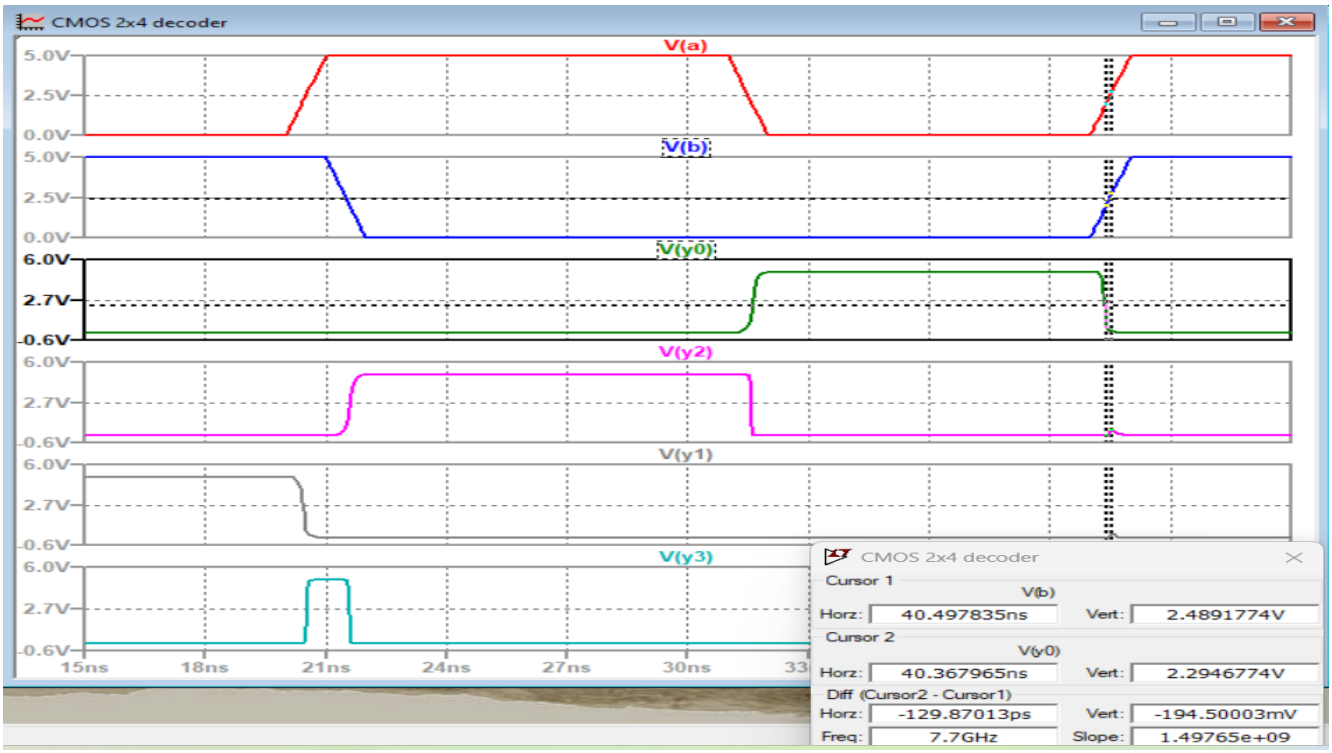
2X4 DECODER CIRCUIT USING CMOS LOGIC



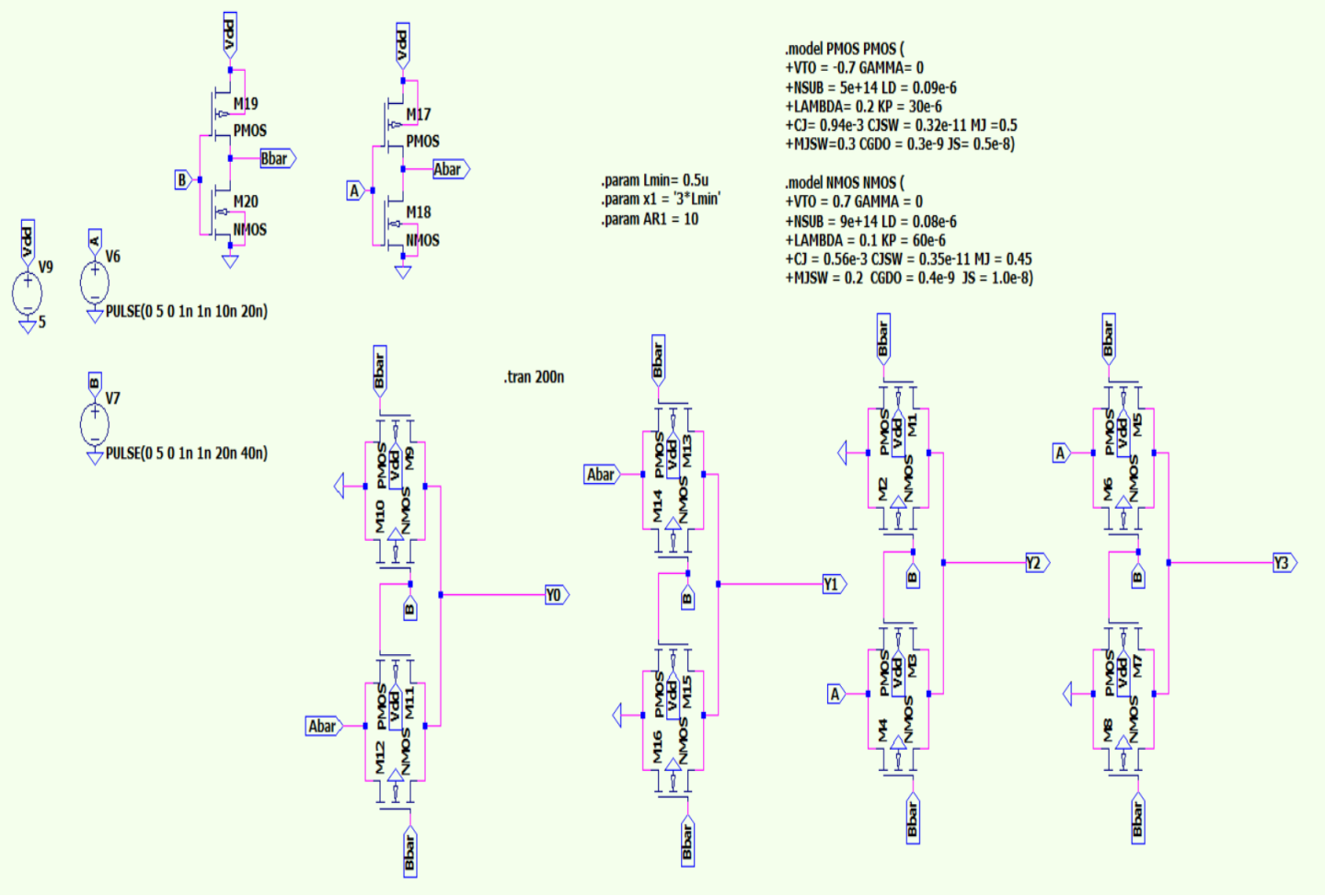
OUTPUT OF 2X4 DECODER USING CMOS LOGIC



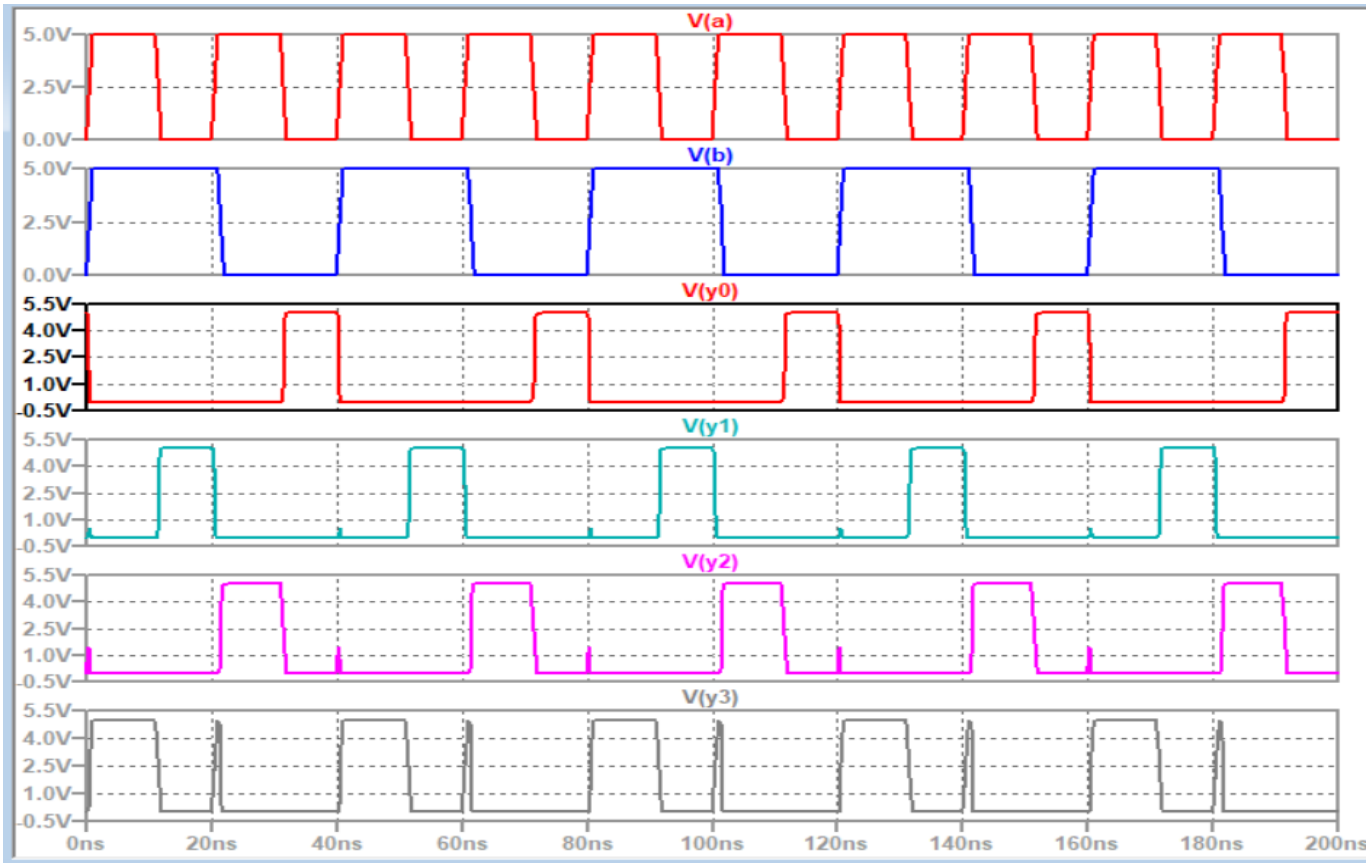
B to Y0 Tlh delay



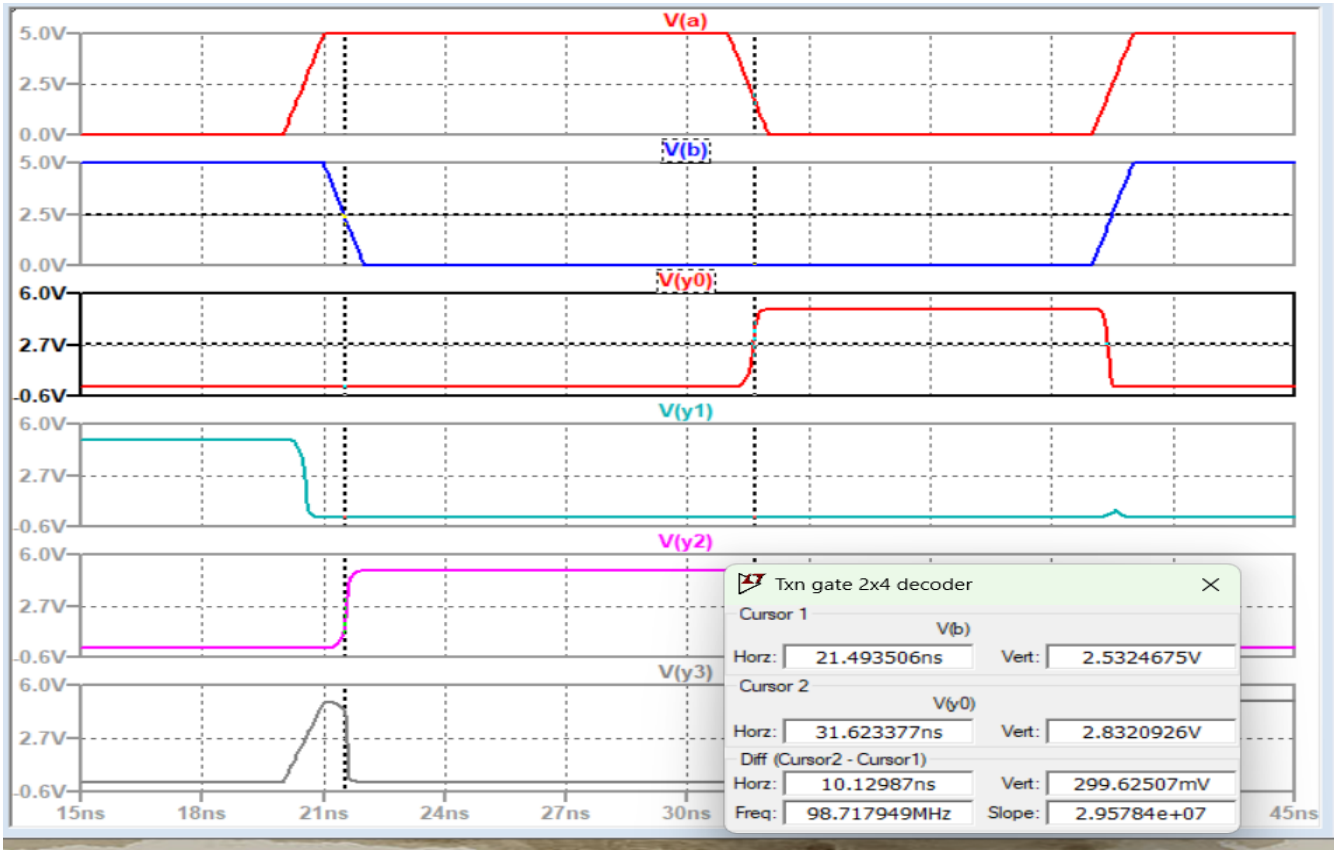
2X4 DECODER CIRCUIT USING TRANSMISSION GATE LOGIC



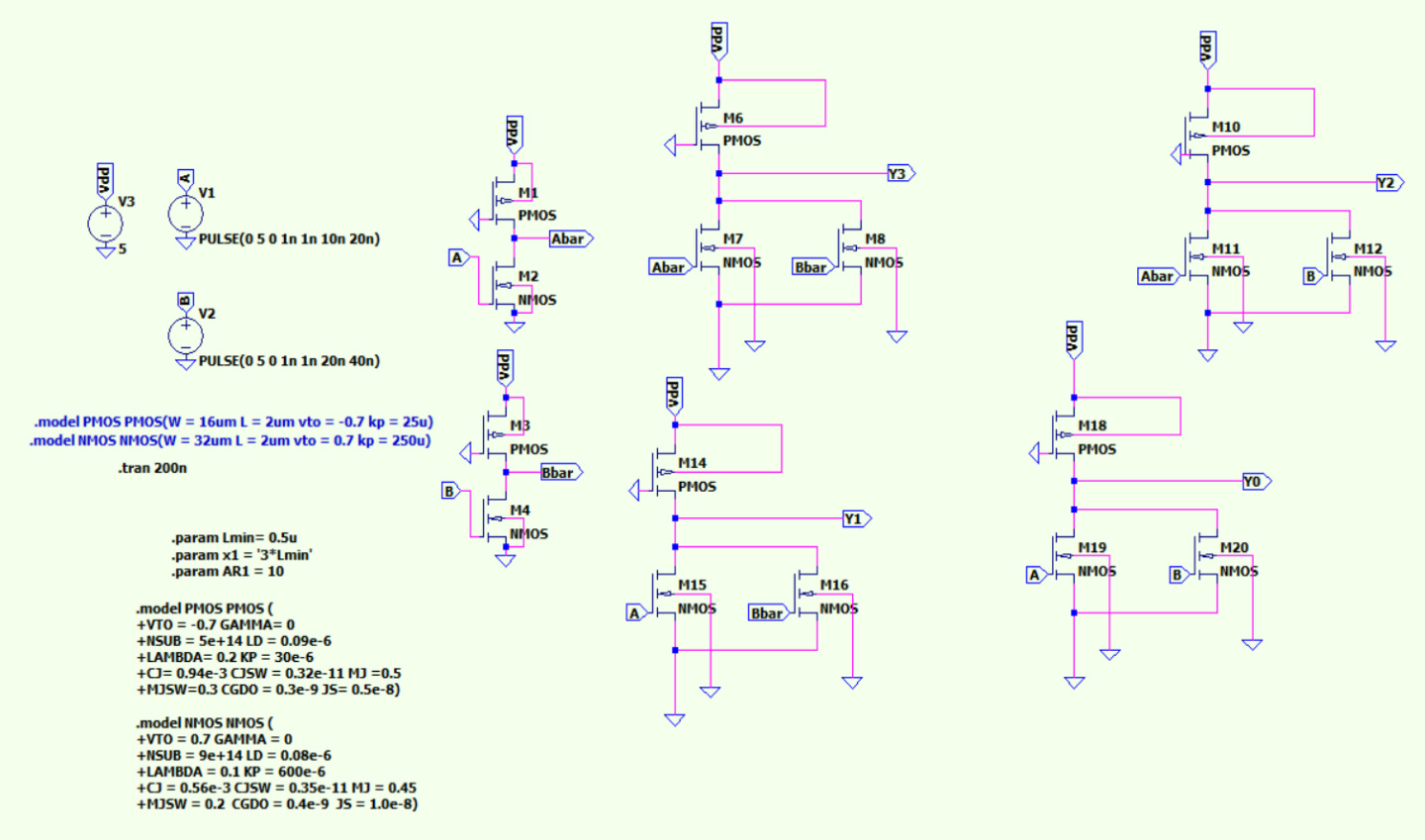
OUTPUT OF 2X4 DECODER USING TRANSMISSION GATE LOGIC



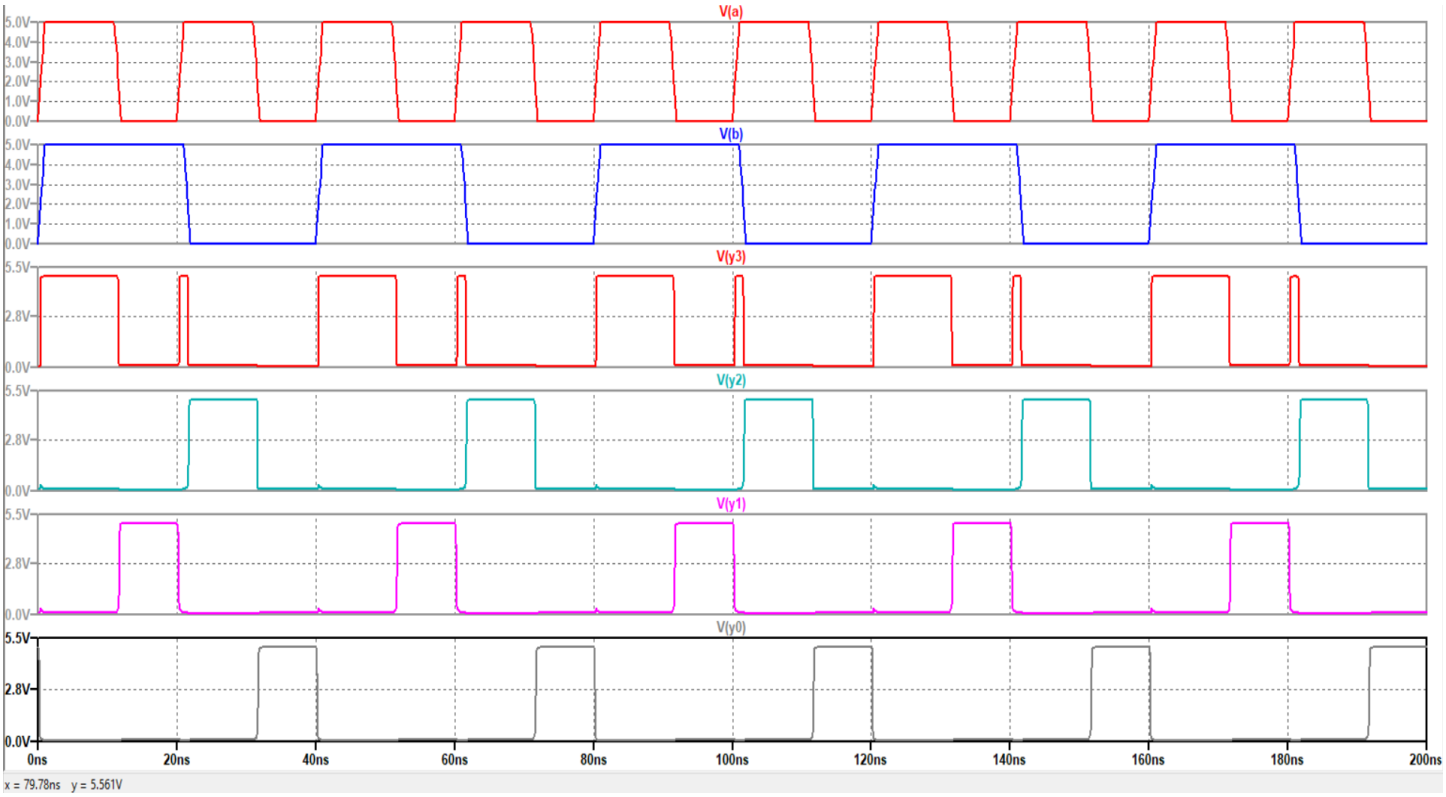
B to Y0 Thl



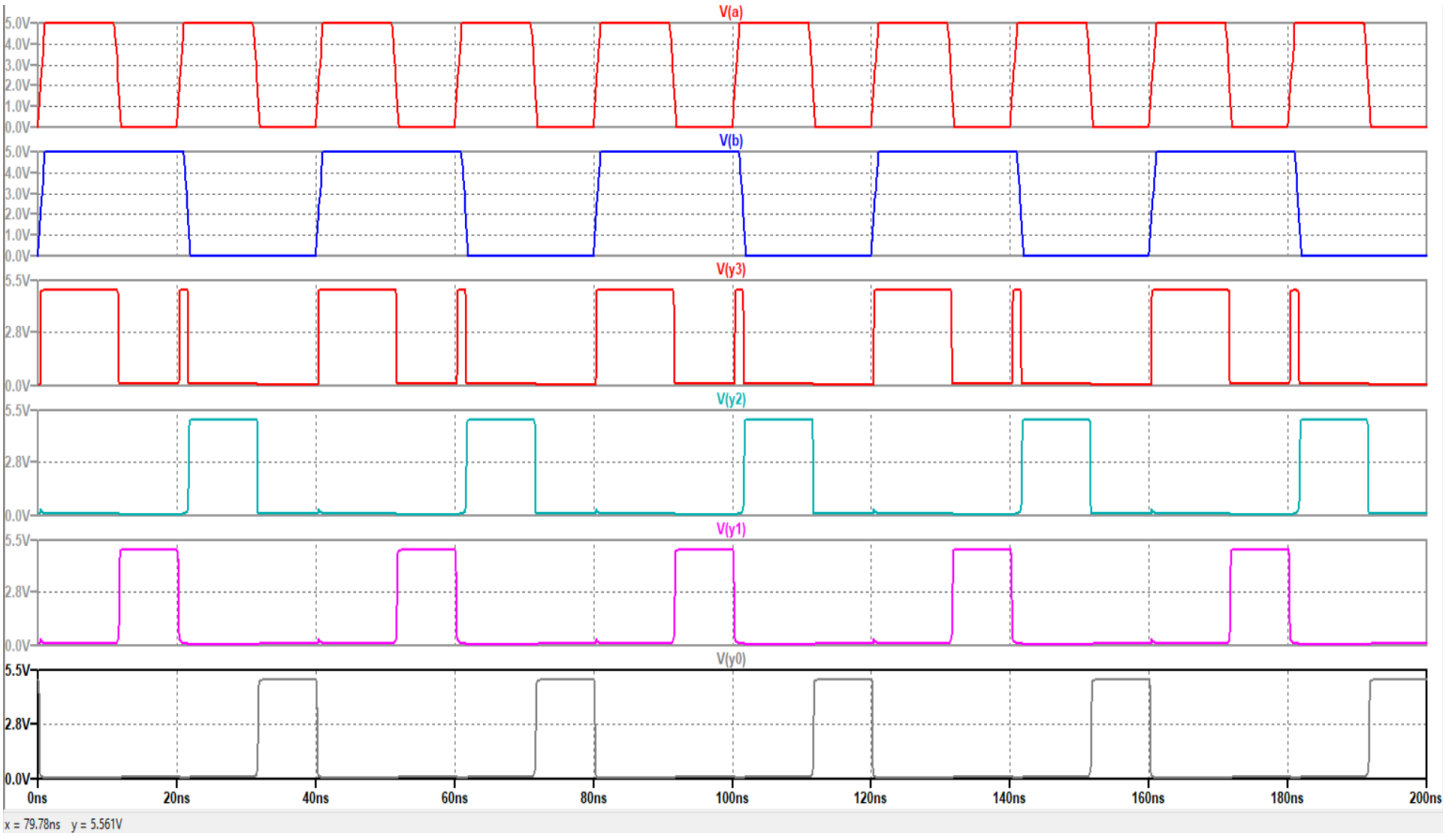
2X4 DECODER CIRCUIT USING PSEUDO NMOS LOGIC



OUTPUT OF 2X4 DECODER USING PSEUDO NMOS LOGIC



B TO Y0 Thl



CONCLUSION

In this project, we explored the design and implementation of a 2:4 decoder using both CMOS (Complementary Metal-Oxide-Semiconductor) and transmission gate logic. Our goal was to create an efficient and reliable decoder that converts a 2-bit binary input into a 4-bit output.

Key Findings

CMOS Implementation:

We designed the 2:4 decoder using CMOS technology, leveraging NMOS (n-channel metal-oxide-semiconductor) and PMOS (p-channel metal-oxide-semiconductor) transistors. The CMOS decoder exhibited excellent noise immunity, low power consumption, and fast switching speeds. By carefully sizing the transistors and optimizing the layout, we achieved a balanced design with minimal static power dissipation.

Transmission Gate Logic:

We also explored an alternative approach using transmission gate logic. Transmission gates are composed of complementary MOSFETs (metal-oxide-semiconductor field-effect transistors) working in parallel. These gates allow bidirectional signal flow and are particularly

useful for multiplexing and demultiplexing applications. The transmission gate-based 2:4 decoder demonstrated comparable performance to the CMOS design.

LTspice Simulation:

We simulated both designs in LTspice, a powerful circuit simulation tool. The simulations validated our theoretical calculations and confirmed the functionality of the decoders. We observed smooth transitions between the output states, minimal propagation delays, and accurate decoding.

Design Trade-offs

Area vs. Speed:

CMOS designs tend to occupy more chip area due to the need for both NMOS and PMOS transistors. Transmission gate logic offers a more compact layout but may sacrifice some speed.

Engineers must carefully consider the trade-offs based on the specific application requirements.

Power Consumption: CMOS designs consume less dynamic power during switching due to the absence of direct current paths. Transmission gates introduce additional leakage currents, impacting overall power efficiency.

System-level considerations should guide the choice between the two approaches.

Future Directions

Scaling and Optimization: As technology nodes continue to shrink, further optimization of the decoder designs is essential. Advanced layout techniques, gate sizing, and transistor stacking can enhance performance. Investigate trade-offs between power, area, and speed for specific applications.

Error Detection and Correction: Extend the decoder functionality to include error detection and correction. Explore Hamming codes or other error-correcting techniques to enhance reliability.

Integration with Larger Systems: Integrate the 2:4 decoder into more complex digital systems.

Consider its role in addressing memory, addressing peripherals, or controlling data flow.

In summary, our project successfully designed and analyzed a 2:4 decoder using both CMOS and transmission gate logic. Whether you prioritize area, speed, or power efficiency, these decoder architectures offer versatile solutions for digital circuitry. As technology evolves, continuous research and innovation will shape the future of decoder design.

Result comparison of 2x4 decoder implemented using static cmos, Transmission gate and pseudo nmos logic.

Comparison Parameter	Static CMOS logic	Transmission gate logic	Pseudo NMOS logic
No. of transistor used	20 including Abar, Bbar signal generation	20	16
Propagation delay T = (Th+Tlh)/2	A to Y0 = 150ps B to Y0 = 5ns	A to Y0 = 92ps B to Y0 = 5ns	A to Y0 = 250ps B to Y0 = 5.2ns
speed	Fastest due to strong pull-up and pull-down networks.	Fast	Slow
Static power dissipation	No	No	Yes
Rail to rail swing	Yes	Yes	No
Ratioed	No	No	Yes without this it won't operate
Noise margin	High	Poor	
Area	Large		Smallest

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