Multi-phase Non-overlapping Clock Generator

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Abstract

A multiphase clock generator is a requirement for wide band multi-path transmission line filter, amongst other relevant applications. There are various implementations for the same. The chosen one here is functionally adept and is verified post-layout, as well. It is fully digital and hence the number of parameters to be taken care is fairly less compared to its analog counterparts. This is designed for a high-frequency (~ 4 GHz) 4-phase non-overlapping clock generation with 25 % duty-cycle.

1 Reference Circuit Details

The circuit is a CMOS transistor-based implementation. It consists of 6 D-Flip Flops, 16 inverters: segregated in 2 types owing to their deliberate sizing for generation of non-overlapping waveforms for 4 different phases: (0°, 90°, 180° and 270°), 12 buffers with uniform tapered dimensions towards output, a NAND gate and a NOT gate. A reference clock signal is utilized for generation of desired signals. A tapered buffer is used to drive the transistor gate, which carries a large capacitive load due to the transistor's parasitic capacitance. The output buffer design was based on using a string of inverters where each has an increasing width compare to the last. By sizing up an inverter, its delay will be reduced, and input capacitance may be increased. The number of stages in the buffer depends on the load capacitance.

2 Reference Circuit

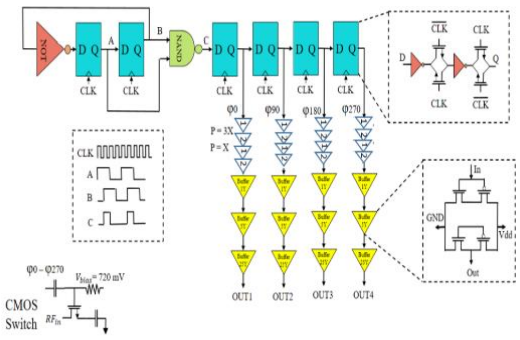

Figure 1: Reference circuit diagram.

3 Reference Circuit Waveforms

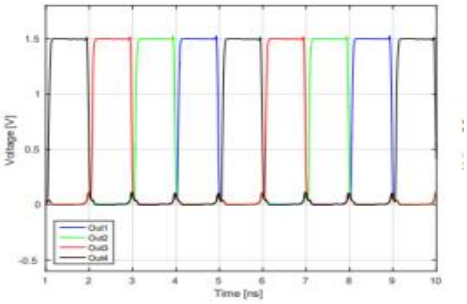

Figure 2: Reference waveform.

References

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