Analog Dynamic Charge Sharing Comparator (AVSD_DCMP_1v8)

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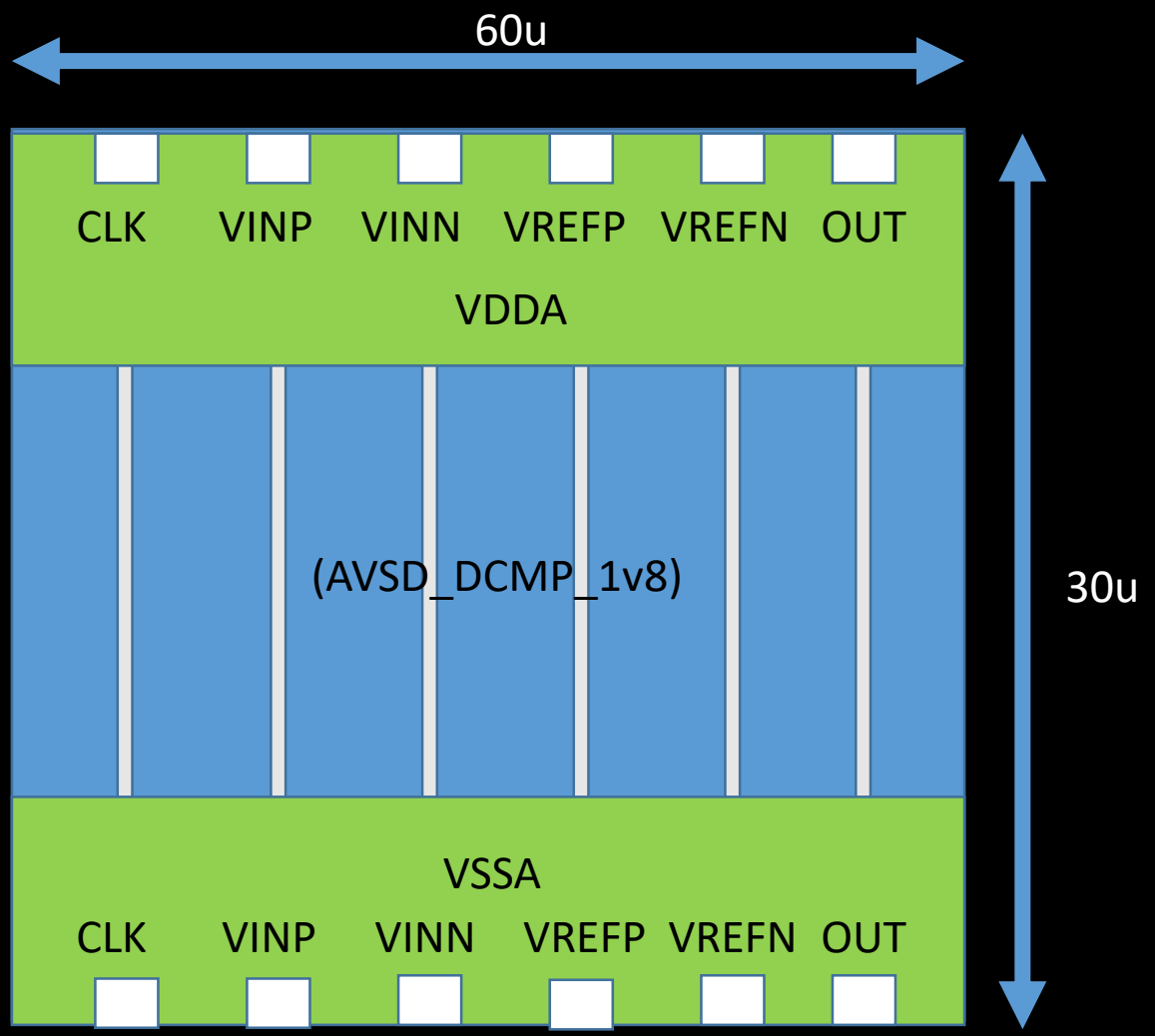
Submitted for Stage-I fulfilment at VSD Corp. Pvt. Ltd.

Bounding box and physical specifications for the Latching Comparator:

Signal pins Metal 2
VDDA Metal 1 (60 X 5)
VSSA Metal 3 (60 X 5)
(The sandwiching of the signal between VDDA and VSSA would provide for shielding)

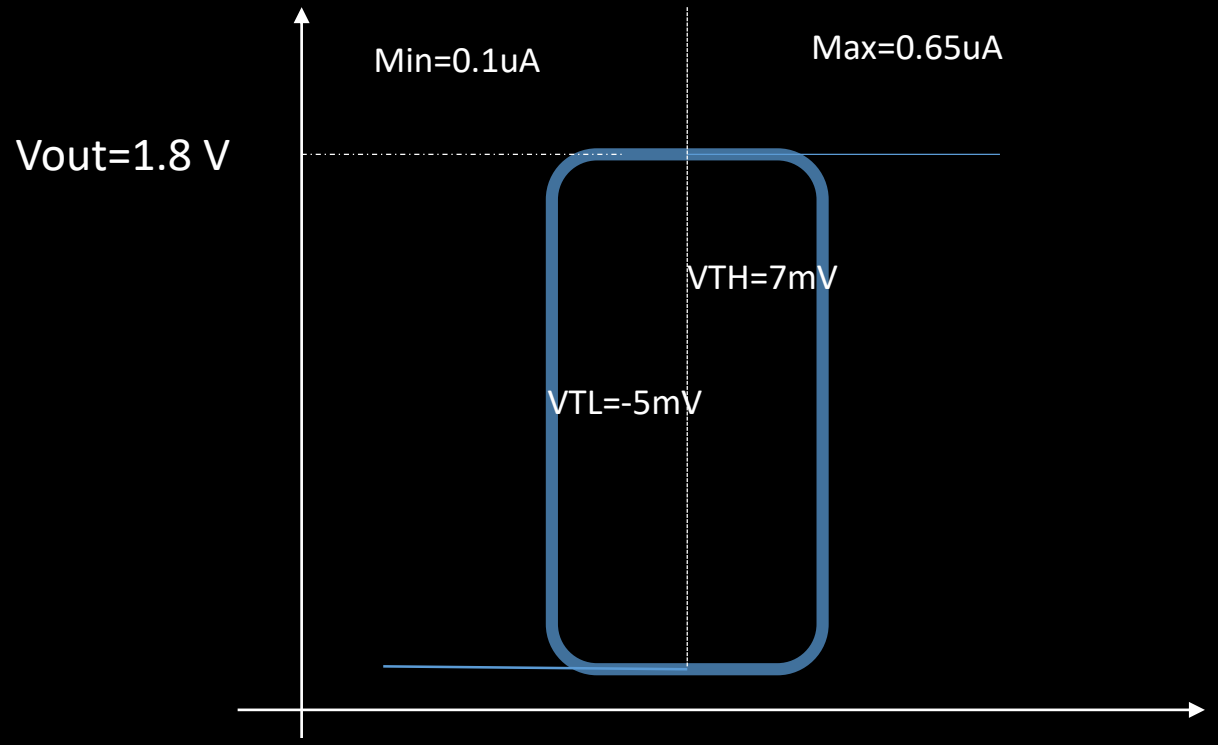
The Area came out to be 1560,
but to maintain an aspect ratio <4
The following dimensions were selected providing a leeway of 240, for overhead adjustments.



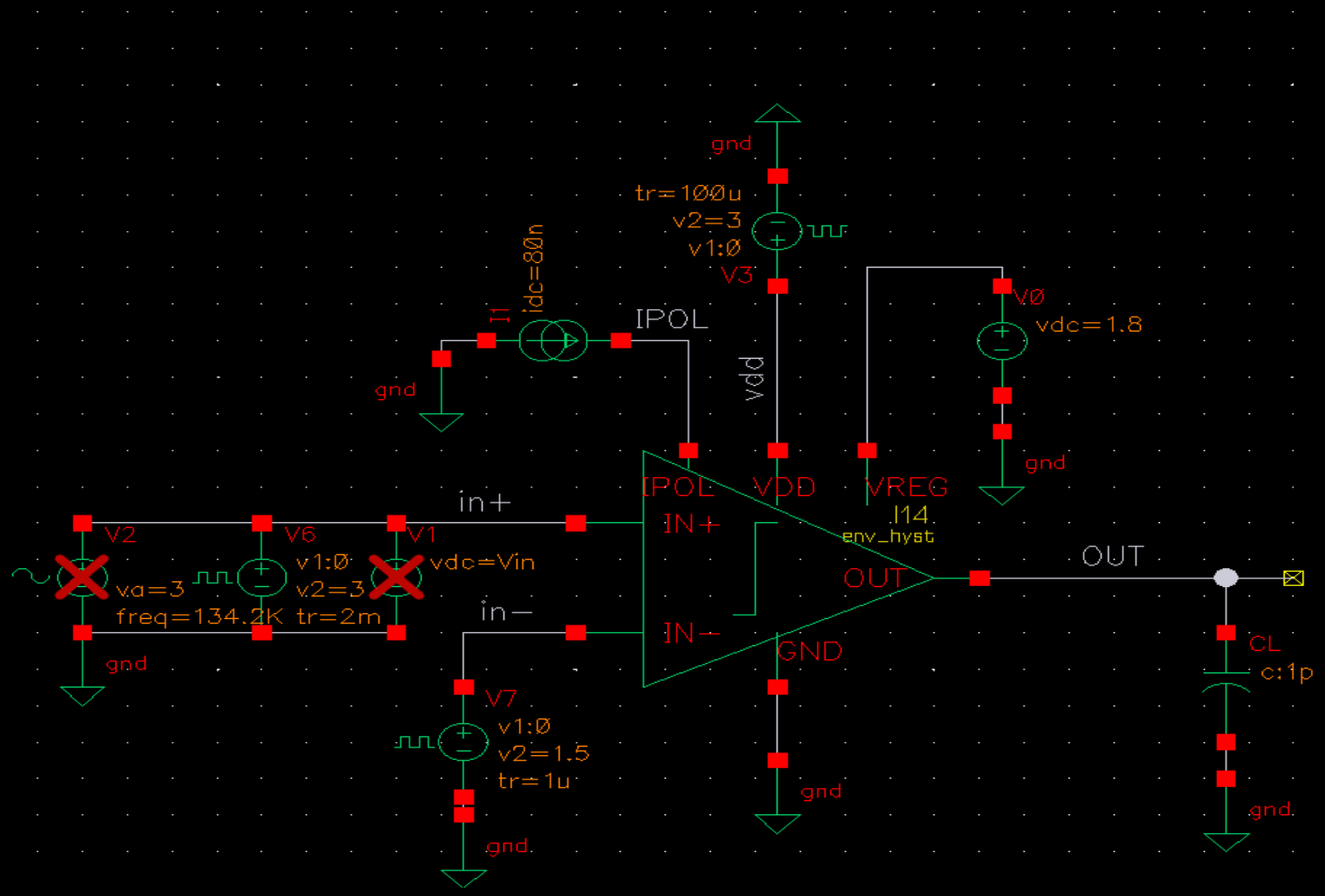
Desired Specifications for the Latching Comparator (AVSD_DCMP_1v8) at 0.13 um node:

- Input Offset Voltage: ~2 mV
- Rise time and Fall time- ~300-750 ns for Vdd = 1.8 V and Vss=-1.8V
- Maximum current consumption: ~30uA
- Applications: General purpose continuous time comparator
- Input Clock frequencies up to 45 kHz

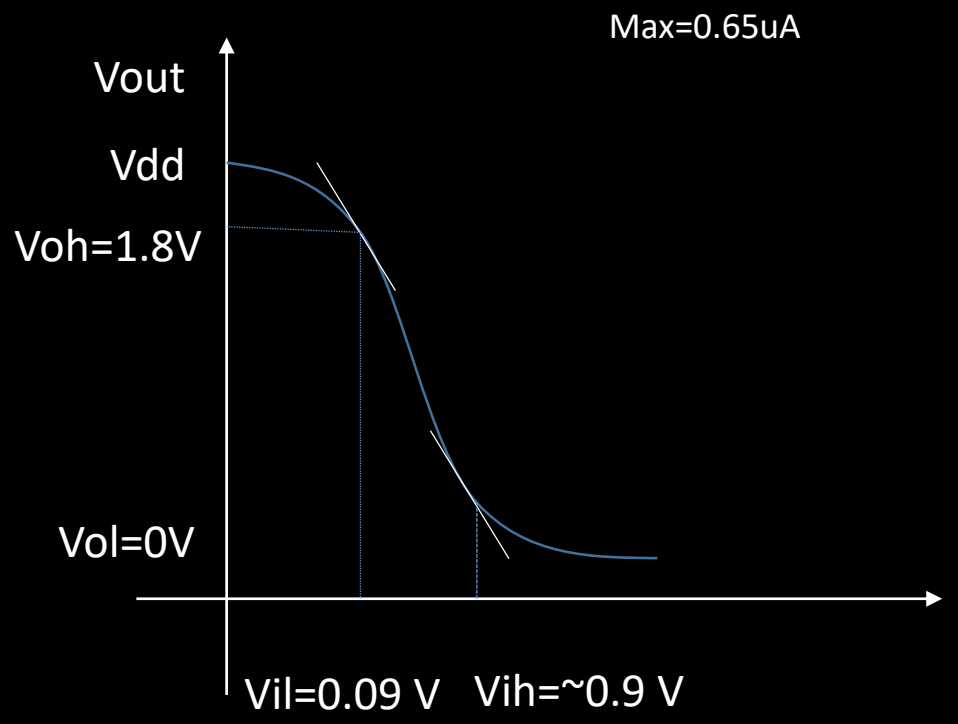
Desired Hysteresis requirements for the Latching Comparator (AVSD_DCMP_1v8) at 0.13 um node:



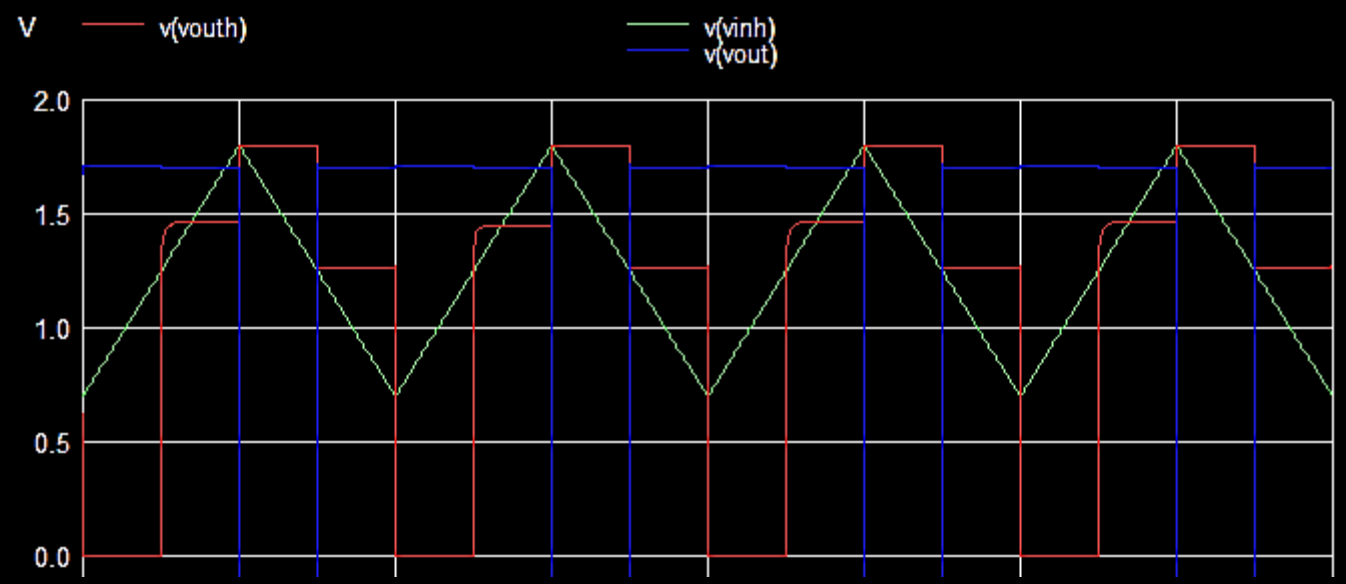
Equivalent test bench for the Comparator (AVSD_DCMP_1v8) at 0.13 um node:



Desired Noise requirements for the Latching Comparator (AVSD_DCMP_1v8) at output load of 10 Mohms at 0.13 um node:



Piecewise linear input for the Latching Comparator (AVSD_DCMP_1v8) at 0.13 um node:



Specs Template Reference

- S3COMP3T18 - 3V Comparator
  - **0.18um TSMC eLL Process.**
  - **Deep NWELL included for Noise Isolation.**
  - **3.0V Power Supplies.**
  - **Internally-generated bias current.**
  - **Input frequencies up to 50kHz.**
  - **Input Referred Offset of < TBD mV.**
  - **Maximum Current Consumption of 29.5 uA.**
  - **Compact Die Area: < 0.0045 mm2**
- https://www.vlsisystemdesign.com/vsd-ip-specs/avsdcmp_3v3