A Tree Architecture based 8-to-1 Serializer

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Abstract

A Serializer/Deserializer (SerDes) is a pair of functional blocks commonly used in high speed communications to compensate for limited input/output. These blocks convert data between serial data and parallel interfaces in each direction. A Serializer, one of the major components of SerDes, is a parallel in serial out architecture. For this the generated clock is taken as is, and the focus is not on clock generation, but on frequency division of the utilized clock. Data from 8 data lines is being serialized at the output.

1 Reference Circuit Details

The circuit is a CMOS transistor-based implementation. It consists of 35 latches, 1 D-FF, 7 MUXs and 3 frequency divide-by-2 blocks. A reference clock signal is utilized for generation of desired signals. The implementation is divided in 3 ranks. The output is taken from the D-FF. Expected Vdd is 2.5 V, and initial clock test frequency to be used is 500 kHz. The frequency will be scaled up to capture the upper limit of performance of the design iteratively. The input is the 8 data lines to the latches as can be seen in the reference circuit.

2 Reference Circuit

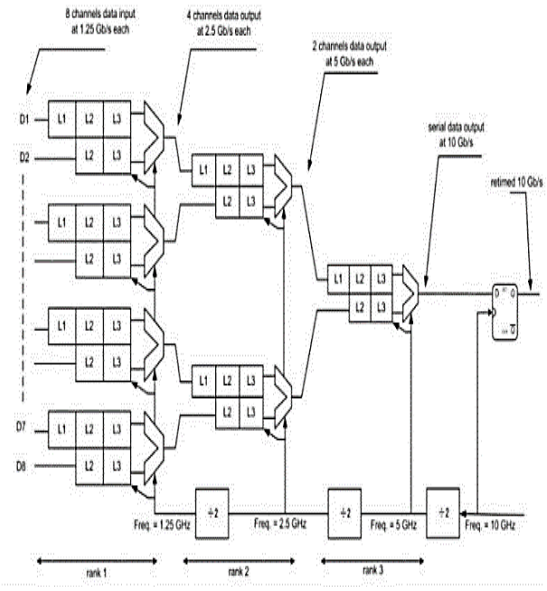

Figure 1: Reference circuit diagram.

3 Reference Circuit Waveforms

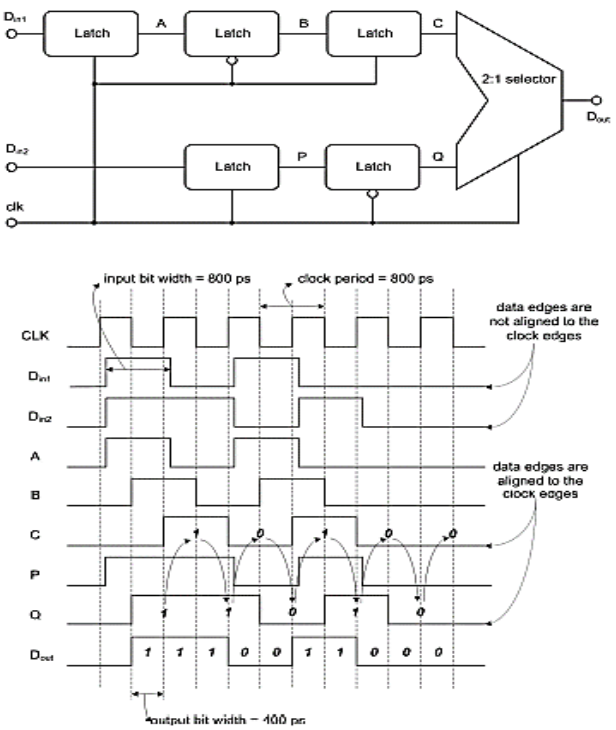

Figure 2: Reference waveform.

References

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