1. Description

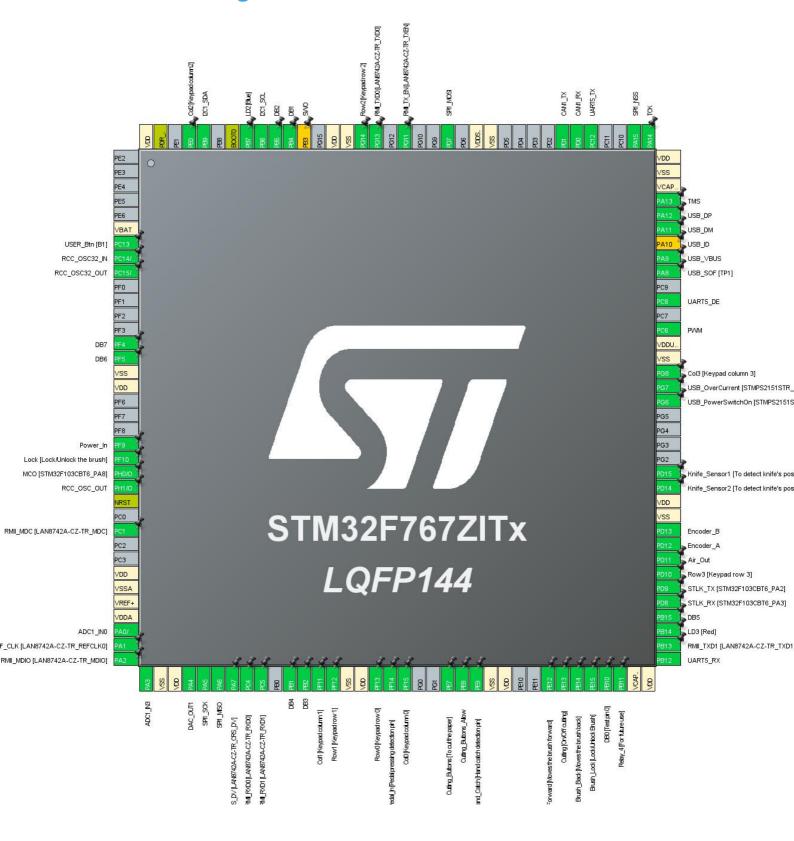
1.1. Project

Project Name	Cutter
Board Name	NUCLEO-F767ZI
Generated with:	STM32CubeMX 5.6.1
Date	08/02/2020

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

(function after reset) VBAT PC13 PC14/OSC32_IN PC15/OSC32_OUT PF4 * PF5 * VSS	Power 1/O 1/O 1/O 1/O 1/O 1/O	GPIO_EXTI13 RCC_OSC32_IN RCC_OSC32_OUT GPIO_Output	USER_Btn [B1]
VBAT PC13 PC14/OSC32_IN PC15/OSC32_OUT PF4 * PF5 * VSS	1/O 1/O 1/O 1/O	RCC_OSC32_IN RCC_OSC32_OUT GPIO_Output	
PC13 PC14/OSC32_IN PC15/OSC32_OUT PF4 * PF5 * VSS	1/O 1/O 1/O 1/O	RCC_OSC32_IN RCC_OSC32_OUT GPIO_Output	
PC14/OSC32_IN PC15/OSC32_OUT PF4 * PF5 * VSS	I/O I/O I/O	RCC_OSC32_IN RCC_OSC32_OUT GPIO_Output	
PC15/OSC32_OUT PF4 * PF5 * VSS	I/O I/O	RCC_OSC32_OUT GPIO_Output	0.77
PF4 * PF5 * VSS	I/O	GPIO_Output	222
PF5 * VSS			
VSS	I/O		DB7
	1	GPIO_Output	DB6
	Power		
VDD	Power		
PF9 *	I/O	GPIO_Input	Power_In
PF10 *	I/O	GPIO_Output	Lock [Lock/Unlock the brush]
PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
PH1/OSC_OUT	I/O	RCC_OSC_OUT	
NRST	Reset		
PC1	I/O	ETH_MDC	RMII_MDC [LAN8742A-CZ- TR_MDC]
VDD	Power		
VSSA	Power		
VREF+	Power		
VDDA	Power		
PA0/WKUP	I/O	ADC1_IN0	
PA1	I/O	ETH_REF_CLK	RMII_REF_CLK [LAN8742A-CZ- TR_REFCLK0]
PA2	I/O	ETH_MDIO	RMII_MDIO [LAN8742A-CZ- TR_MDIO]
PA3	I/O	ADC1_IN3	
VSS	Power		
VDD	Power		
PA4	I/O	DAC_OUT1	
PA5	I/O	SPI1_SCK	
PA6	I/O	SPI1_MISO	
PA7	I/O	ETH_CRS_DV	RMII_CRS_DV [LAN8742A- CZ-TR_CRS_DV]
PC4	I/O	ETH_RXD0	RMII_RXD0 [LAN8742A-CZ- TR_RXD0]
	PF10 * PH0/OSC_IN PH1/OSC_OUT NRST PC1 VDD VSSA VREF+ VDDA PA0/WKUP PA1 PA2 PA3 VSS VDD PA4 PA5 PA6 PA7	PF9 * I/O PF10 * I/O PH0/OSC_IN I/O PH1/OSC_OUT I/O NRST Reset PC1 I/O VDD Power VSSA Power VREF+ Power VDDA Power PA0/WKUP I/O PA1 I/O PA2 I/O PA3 I/O VSS Power VDD Power PA4 I/O PA5 I/O PA6 I/O PA7 I/O	PF9 * I/O GPIO_Input PF10 * I/O GPIO_Output PH0/OSC_IN I/O RCC_OSC_IN PH1/OSC_OUT I/O RCC_OSC_OUT NRST Reset FTH_MDC VDD Power FTH_MDC VSSA Power Power VDDA Power Power VDDA Power POWER PA0/WKUP I/O ADC1_INO PA1 I/O ETH_REF_CLK PA2 I/O ETH_MDIO PA3 I/O ADC1_IN3 VSS Power VDD Power PA4 I/O DAC_OUT1 PA5 I/O SPI1_SCK PA6 I/O SPI1_MISO PA7 I/O ETH_CRS_DV

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
= 2	reset)		1 011011011(0)	
45	PC5	I/O	ETH_RXD1	RMII_RXD1 [LAN8742A-CZ- TR_RXD1]
47	PB1 *	I/O	GPIO_Output	DB4
48	PB2 *	I/O	GPIO_Output	DB3
49	PF11 *	I/O	GPIO_Input	Col1 [Keypad column 1]
50	PF12 *	I/O	GPIO_Input	Row1 [Keypad row 1]
51	VSS	Power		
52	VDD	Power		
53	PF13 *	I/O	GPIO_Input	Row0 [Keypad row 0]
54	PF14 *	I/O	GPIO_Input	Pedal_In [Pedal pressing detection pin]
55	PF15 *	I/O	GPIO_Input	Col0 [Keypad column 0]
58	PE7 *	I/O	GPIO_Input	Cutting_Buttons [To cut the paper]
59	PE8 *	I/O	GPIO_Output	Cutting_Buttons_Allow
60	PE9 *	I/O	GPIO_Input	Hand_Catch [Hand catch detection pin]
61	VSS	Power		
62	VDD	Power		
65	PE12 *	I/O	GPIO_Output	Brush_Forward [Moves the brush forward]
66	PE13 *	I/O	GPIO_Output	Cutting [On/Off cutting]
67	PE14 *	I/O	GPIO_Output	Brush_Back [Moves the brush back]
68	PE15 *	I/O	GPIO_Output	Brush_Lock [Lock/Unlock Brush]
69	PB10 *	I/O	GPIO_Output	DB0 [Test pin 0]
70	PB11 *	I/O	GPIO_Output	Relay_4 [For future use]
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	UART5_RX	
74	PB13	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ- TR_TXD1]
75	PB14 *	I/O	GPIO_Output	LD3 [Red]
76	PB15 *	I/O	GPIO_Output	DB5
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
79	PD10 *	I/O	GPIO_Input	Row3 [Keypad row 3]
80	PD11 *	I/O	GPIO_Output	Air_Out

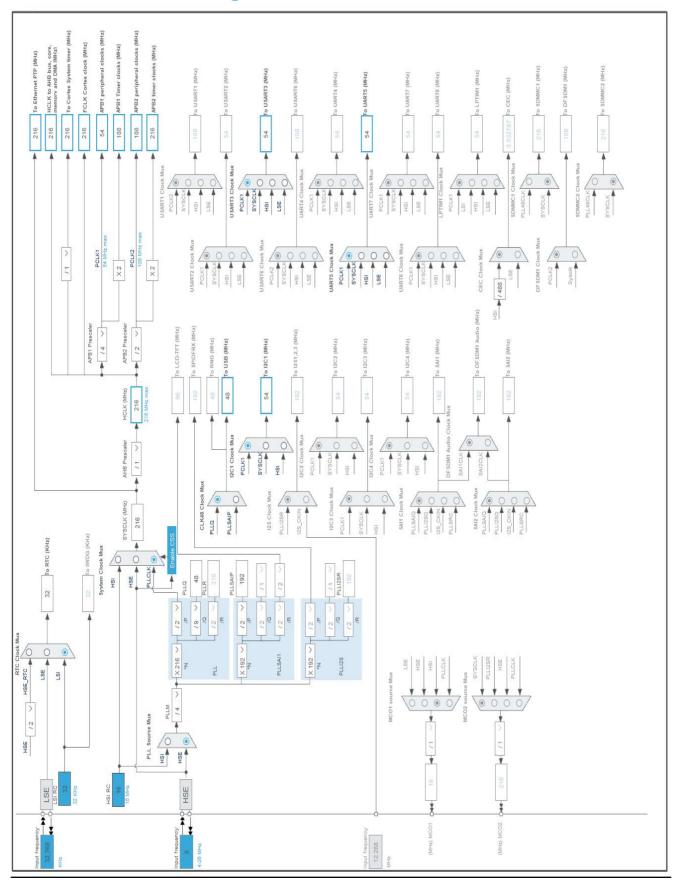
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
81	PD12	I/O	TIM4_CH1	Encoder_A
82	PD13	I/O	TIM4_CH2	Encoder_B
83	VSS	Power	11111_0112	Enocaci_B
84	VDD	Power		
85	PD14 *	I/O	GPIO_Input	Knife_Sensor2 [To detect knife's position]
86	PD15 *	I/O	GPIO_Input	Knife_Sensor1 [To detect knife's position]
91	PG6 *	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7 *	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
93	PG8 *	I/O	GPIO_Input	Col3 [Keypad column 3]
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	TIM3_CH1	PWM
98	PC8	I/O	UART5_DE	
100	PA8	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10 **	I/O	USB_OTG_FS_ID	USB_ID
103	PA11	I/O	USB_OTG_FS_DM	USB_DM
104	PA12	I/O	USB_OTG_FS_DP	USB_DP
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
110	PA15	I/O	SPI1_NSS	
113	PC12	I/O	UART5_TX	
114	PD0	I/O	CAN1_RX	
115	PD1	I/O	CAN1_TX	
120	VSS	Power		
121	VDDSDMMC	Power		
123	PD7	I/O	SPI1_MOSI	
126	PG11	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A- CZ-TR_TXEN]
128	PG13	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ- TR_TXD0]
129	PG14 *	I/O	GPIO_Input	Row2 [Keypad row 2]
130	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
131	VDD	Power		
133	PB3 **	I/O	SYS_JTDO-SWO	SWO
134	PB4 *	I/O	GPIO_Output	DB1
135	PB5 *	I/O	GPIO_Output	DB2
136	PB6	I/O	I2C1_SCL	
137	PB7 *	I/O	GPIO_Output	LD2 [Blue]
138	воото	Boot		
140	PB9	I/O	I2C1_SDA	
141	PE0 *	I/O	GPIO_Input	Col2 [Keypad column2]
143	PDR_ON	Reset		
144	VDD	Power		

^{*} The pin is affected with an I/O function

^{**} The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value
Project Name	Cutter
Project Folder	W:\Cutter_WS\git_project\Cutter\ProjectsSW
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.16.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

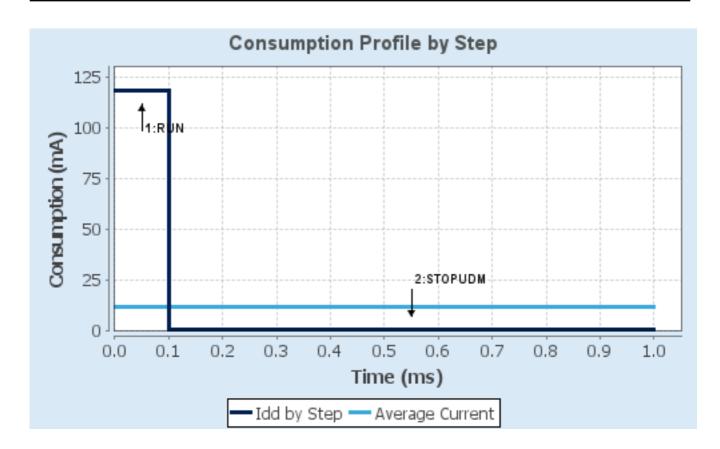
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	89.42	104.98
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24 DMIPS

6.6. Chart



7. IPs and Middleware Configuration 7.1. ADC1

mode: IN0 mode: IN3

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled
DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

Channel Channel 0
Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. CAN1

mode: Mode

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum) 16

Time Quantum 296.2962962963 *

Time Quanta in Bit Segment 1 4 Times *

Time Quanta in Bit Segment 2 4 Times *

ReSynchronization Jump Width 1 Time

Basic Parameters:

Time Triggered Communication Mode

Automatic Bus-Off Management

Disable

Automatic Wake-Up Mode

Disable

Automatic Retransmission

Disable

Receive Fifo Locked Mode

Disable

Transmit Fifo Priority

Disable

Advanced Parameters:

Operating Mode Normal

7.3. CORTEX M7

7.3.1. Parameter Settings:

Cortex Interface Settings:

Flash Interface AXI Interface
ART ACCLERATOR Disabled
Instruction Prefetch Disabled
CPU ICache Disabled
CPU DCache Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode MPU NOT USED

7.4. DAC

mode: OUT1 Configuration 7.4.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer Enable
Trigger None

7.5. ETH

Mode: RMII

7.5.1. Parameter Settings:

Advanced: Ethernet Media Configuration:

Auto Negotiation Enabled

General: Ethernet Configuration:

Ethernet MAC Address 00:80:E1:00:00:00

PHY Address 0 *

Ethernet Basic Configuration:

Rx Mode Polling Mode
TX IP Header Checksum Computation By hardware

7.5.2. Advanced Parameters:

External PHY Configuration:

PHY LAN8742A_PHY_ADDRESS

PHY Address Value 0

PHY Reset delay these values are based on a 1 ms

Systick interrupt

0x00000FF *

PHY Configuration delay

PHY Read TimeOut

Ox0000FFF *

PHY Write TimeOut

Ox0000FFF *

Common: External PHY Configuration:

Transceiver Basic Control Register 0x00 * Transceiver Basic Status Register 0x01 * PHY Reset 0x8000 * Select loop-back mode 0x4000 * Set the full-duplex mode at 100 Mb/s 0x2100 * Set the half-duplex mode at 100 Mb/s 0x2000 * Set the full-duplex mode at 10 Mb/s 0x0100 * Set the half-duplex mode at 10 Mb/s 0x0000 * Enable auto-negotiation function 0x1000 * Restart auto-negotiation function 0x0200 * Select the power down mode 0x0800 * Isolate PHY from MII 0x0400 * Auto-Negotiation process completed 0x0020 * Valid link established 0x0004 * Jabber condition detected 0x0002 *

Extended: External PHY Configuration:

PHY special control/status register Offset

Ox1F *

PHY Speed mask

Ox0004 *

PHY Duplex mask

Ox0010 *

PHY Interrupt Source Flag register Offset

Ox001D *

PHY Link down inturrupt

Ox000B *

7.6. GPIO

7.7. I2C1

I2C: I2C

7.7.1. Parameter Settings:

Timing configuration:

I2C Speed Mode Standard Mode

I2C Speed Frequency (KHz)100Rise Time (ns)0Fall Time (ns)0Coefficient of Digital Filter0

Analog Filter Enabled

Timing 0x20404768 *

Slave Features:

Clock No Stretch Mode Disabled
General Call Address Detection Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

7.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.8.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Over Drive Enabled

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.9. RTC

mode: Activate Clock Source 7.9.1. Parameter Settings:

General:

Hour Format Hourformat 24

Asynchronous Predivider value 127
Synchronous Predivider value 255

7.10. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Input Signal

7.10.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 4 Bits

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 2

Baud Rate 54.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled

NSSP Mode Enabled

NSS Signal Type Input Hardware

7.11. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.12. TIM3

Clock Source: Internal Clock
Channel1: PWM Generation CH1

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 0

Internal Clock Division (CKD)

No Division

auto-reload preload

Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.13. TIM4

Combined Channels: Encoder Mode

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 1 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 65535 *

Internal Clock Division (CKD) No Division auto-reload preload Disable

ringger Output (TNOO) i arameters	Trigger	Output ((TRGO)	Parameters
-----------------------------------	---------	----------	--------	------------

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode TI1

____ Parameters for Channel 1 ____

Polarity Rising Edge
IC Selection Direct
Prescaler Division Ratio No division

Input Filter 0

____ Parameters for Channel 2 ____

Polarity Rising Edge
IC Selection Direct
Prescaler Division Ratio No division
Input Filter 0

7.14. UART5

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
Polarity High
Assertion Time 0
Deassertion Time 0

Advanced Features:

Auto Baudrate Disable
TX Pin Active Level Inversion Disable
RX Pin Active Level Inversion Disable
Data Inversion Disable
TX and RX Pins Swapping Disable

Overrun Enable
DMA on RX Error Enable
MSB First Disable

7.15. USART3

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable Data Inversion Disable TX and RX Pins Swapping Overrun Enable DMA on RX Error Enable MSB First Disable

7.16. USB OTG FS

Mode: Device_Only mode: Activate_SOF mode: Activate_VBUS

7.16.1. Parameter Settings:

Speed Device Full Speed 12MBit/s

Low powerDisabledLink Power ManagementDisabledVBUS sensingEnabled

Signal start of frame	Enabled	
* User modified value		

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0/WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Very High	RMII_MDC [LAN8742A- CZ-TR_MDC]
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_REF_CLK [LAN8742A-CZ- TR_REFCLK0]
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_MDIO [LAN8742A- CZ-TR_MDIO]
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Very High	RMII_CRS_DV [LAN8742A-CZ- TR_CRS_DV]
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	RMII_RXD0 [LAN8742A- CZ-TR_RXD0]
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	RMII_RXD1 [LAN8742A- CZ-TR_RXD1]
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	RMII_TXD1 [LAN8742A- CZ-TR_TXD1]
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Very High	RMII_TX_EN [LAN8742A- CZ-TR_TXEN]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	RMII_TXD0 [LAN8742A- CZ-TR_TXD0]
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	Very High *	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	Very High	
RCC	PC14/OSC3 2_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC3 2_OUT	RCC_OSC32_O UT	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PH0/OSC_I N	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1/OSC_O UT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA15	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	TCK
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	Encoder_A
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	Encoder_B
UART5	PB12	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC8	UART5_DE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	STLK_TX [STM32F103CBT6_PA2]
USB_OTG_ FS	PA8	USB_OTG_FS_ SOF	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USB_SOF [TP1]
	PA9	USB_OTG_FS_ VBUS	Input mode	No pull-up and no pull-down	n/a	USB_VBUS
	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USB_DM
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USB_DP
Single Mapped	PA10	USB_OTG_FS_I D	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USB_ID

Signals PB3 GPIO PC13 PF4 PF5 PF9 PF10 PB1 PB2	SYS_JTDO-SWO GPIO_EXTI13 GPIO_Output GPIO_Output GPIO_Output GPIO_Output GPIO_Output	n/a External Interrupt Mode with Rising edge trigger detection Output Push Pull Output Push Pull Input mode Output Push Pull Output Push Pull	No pull-up and no pull-down No pull-up and no pull-down No pull-up and no pull-down Pull-up * No pull-up and no pull-down	n/a n/a Low Low n/a Low	SWO USER_Btn [B1] DB7 DB6 Power_In Lock [Lock/Unlock the
GPIO PC13 PF4 PF5 PF9 PF10 PB1	SWO GPIO_EXTI13 GPIO_Output GPIO_Output GPIO_Output GPIO_Output GPIO_Output GPIO_Output	External Interrupt Mode with Rising edge trigger detection Output Push Pull Output Push Pull Input mode Output Push Pull	No pull-up and no pull-down No pull-up and no pull-down No pull-up and no pull-down Pull-up *	n/a Low Low n/a	USER_Btn [B1] DB7 DB6 Power_In
PF4 PF5 PF9 PF10	GPIO_Output GPIO_Output GPIO_Input GPIO_Output GPIO_Output GPIO_Output	Rising edge trigger detection Output Push Pull Output Push Pull Input mode Output Push Pull	No pull-up and no pull-down No pull-up and no pull-down Pull-up *	Low Low n/a	DB7 DB6 Power_In
PF5 PF9 PF10 PB1	GPIO_Output GPIO_Output GPIO_Output GPIO_Output GPIO_Output	Output Push Pull Input mode Output Push Pull	No pull-up and no pull-down Pull-up *	Low n/a	DB6 Power_In
PF9 PF10 PB1	GPIO_Output GPIO_Output GPIO_Output	Input mode Output Push Pull	Pull-up *	n/a	Power_In
PF10	GPIO_Output GPIO_Output GPIO_Output	Output Push Pull	•		_
PB1	GPIO_Output GPIO_Output	·	No pull-up and no pull-down	Low	Lock [Lock/Unlock the
	GPIO_Output	Output Push Pull			brush]
PR2			No pull-up and no pull-down	Low	DB4
1 02	0	Output Push Pull	No pull-up and no pull-down	Low	DB3
PF11	GPIO_Input	Input mode	Pull-down *	n/a	Col1 [Keypad column 1]
PF12	GPIO_Input	Input mode	Pull-down *	n/a	Row1 [Keypad row 1]
PF13	GPIO_Input	Input mode	Pull-down *	n/a	Row0 [Keypad row 0]
PF14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Pedal_In [Pedal pressing detection pin]
PF15	GPIO_Input	Input mode	Pull-down *	n/a	Col0 [Keypad column 0]
PE7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Cutting_Buttons [To cut the paper]
PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cutting_Buttons_Allow
PE9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Hand_Catch [Hand catch detection pin]
PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Brush_Forward [Moves the brush forward]
PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cutting [On/Off cutting]
PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Brush_Back [Moves the brush back]
PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Brush_Lock [Lock/Unlock Brush]
PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DB0 [Test pin 0]
PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay_4 [For future use]
PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DB5
PD10	GPIO_Input	Input mode	Pull-down *	n/a	Row3 [Keypad row 3]
PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Air_Out
PD14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Knife_Sensor2 [To detect knife's position]
PD15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Knife_Sensor1 [To detect knife's position]
PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PG8	GPIO_Input	Input mode	Pull-down *	n/a	Col3 [Keypad column 3]
	PG14	GPIO_Input	Input mode	Pull-down *	n/a	Row2 [Keypad row 2]
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DB1
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DB2
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]
	PE0	GPIO_Input	Input mode	Pull-down *	n/a	Col2 [Keypad column2]

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority			
Non maskable interrupt	true	0	0			
Hard fault interrupt	true	0				
Memory management fault	true	0				
Pre-fetch fault, memory access fault	true	0	0			
Undefined instruction or illegal state	true	0	0			
System service call via SWI instruction	true	0	0			
Debug monitor	true	0	0			
Pendable request for system service	true	0	0			
System tick timer	true	0	0			
TIM4 global interrupt	true 0		0			
PVD interrupt through EXTI line 16		unused				
Flash global interrupt	unused					
RCC global interrupt	unused					
ADC1, ADC2 and ADC3 global interrupts	unused					
CAN1 TX interrupts	unused					
CAN1 RX0 interrupts	unused					
CAN1 RX1 interrupt	unused					
CAN1 SCE interrupt	unused					
TIM3 global interrupt	unused					
I2C1 event interrupt		unused				
I2C1 error interrupt		unused				
SPI1 global interrupt		unused				
USART3 global interrupt		unused				
EXTI line[15:10] interrupts		unused				
UART5 global interrupt		unused				
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused					
Ethernet global interrupt		unused				
Ethernet wake-up interrupt through EXTI line 19	unused					
USB On The Go FS global interrupt	unused					
FPU global interrupt	unused					

* User modified value

9. Predefined Views - Category view : Current



10. Software Pack Report