R.V.R. & J.C.COLLEGE OF ENGINEERING (Autonomous)
Chandramoulipuram :: Chowdavaram :: Guntur-522019
(w.e.f. the academic year 2020-2021)
B.Tech., Computer Science and Business Systems (R20 Regulations)

CB212	**Computer Organization &Architecture**			
Semester III (Second Year)	**L**	**T**	**P**	**C**
	3	**-**	**-**	**3**

COURSE OBJECTIVES:

At the end of the course the students will understand

- Working of computer system and the principles of instruction level architecture and instruction execution.
- Concepts of I/O devices, hardware components in CPU, and its working principles.
- State of art in memory system design and concepts of computer Arithmetic.
- Advanced pipelining techniques and basic concepts of parallel processors.

COURSE OUTCOMES:

After successful completion of the course, the students are able to

CO 1: Define the structure of computer and construct control sequence for an instruction.
CO 2: Demonstrate various I/O handling mechanisms and Design control unit organization.
CO3: IllustratememoryhierarchyandImplement algorithmsrelatedtocomputerarithmetic.
CO 4: Develop a pipeline for consistent execution of instructions and define various parallel processing concepts.

UNITI [Text book1,2] [CO 1] (13Periods)

Revision of basics in Boolean logic and Combinational/Sequential Circuits Functional blocks of a computer: CPU, memory, input-output subsystems, control unit.

Instruction set architecture of a CPU: Registers, instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set. Outlining instruction sets of some common CPUs.

Data representation: Signed number representation, fixed and floating point representations, character representation.

UNITII [Textbook 2] [CO 2] (13Periods)

Peripheral devices and their characteristics: Input-output subsystems, I/O device interface, I/O transfers – program controlled, interrupt driven and DMA, privileged and non-privileged instructions, software interrupts and exceptions. Programs and processes – role of interrupts in process state transitions, I/O device interfaces – SCSI, USB

Introduction to x86 architecture.

CPU control unit design: Hardwired and micro-programmed design approaches, design of a simple hypothetical CPU.

UNITIII [Text book 2] [CO 3] (13Periods)

Memory system design: Semiconductor memory technologies, memory organization

Memory organization: Memory interleaving, concept of hierarchical memory organization, cache memory, cache size vs. block size, mapping functions, replacement algorithms, write policies.

Computer arithmetic: Integer addition and subtraction, ripple carry adder, carry look-ahead adder, etc. multiplication – shift-and-add, Booth multiplier, carry save multiplier, etc. Division restoring and non-restoring techniques, floating point arithmetic, IEEE 754format

UNITIV [Textbook 2] [CO 4] (13Periods)

Pipelining: Basic concepts of pipelining, throughput and speedup, pipeline hazards.

Parallel Processors: Introduction to parallel processors, Concurrent access to memory and cache coherency

LEARNING RESOURCES

Text Books:

1. *Computer System Architecture* M. M. Mano: 3rd ed., Prentice Hall of India, New Delhi,1993.
2. *Computer Organization and Embedded Systems*, CarlHamacher.

Reference Books:

1. *Computer Architecture and Organization*, John P.Hayes.
2. *Computer Organization and Architecture: Designing for Performance*, WilliamStallings.
3. *Computer System Design and Architecture*, Vincent P. Heuring and Harry F.Jordan.

CO-PO MAPPING:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CB212.1	3	2	2					2		2		2
CB212.2	3		1		2			2		2	2	2
CB212.3	3		3	2				2		2		2
CB212.4	3	2	2	2	2			2		2		2

CO – PSO MAPPING:

	PSO1	**PSO2**	**PSO3**
CB212.1	3	2	3
CB212.2	3	2	3
CB212.3	3	2	3
CB212.4	3	2	3