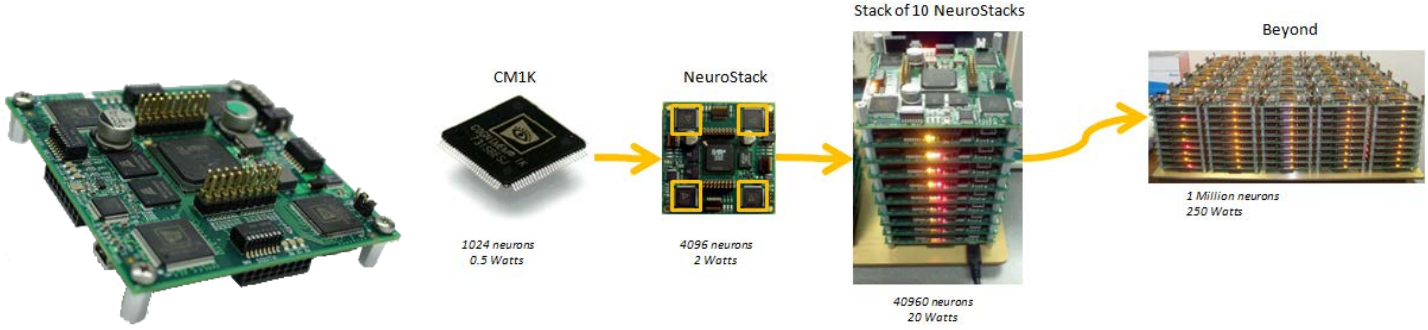
NEUROSTACK BOARD

NeuroStack is a board with a unique architecture featuring four NeuroMem neuromorphic memory chips and a Field Programmable Gate Array to host configurable communication, recognition engines and other IP cores of your choice. NeuroStack is an ideal platform to program applications requiring the modeling and classification of simple and complex datasets at high speed and with a deterministic latency. The neurons can learn and recognize patterns received from an external host or generated on-board from sensor signals connected to the board. The four CM1K chips can be used as a single chain of 4096 neurons or a combination of chains of 1024, 2048 or 3072 neurons. Furthermore, NeuroStack is stackable meaning that the chain of CM1K chips can be seamlessly expanded by increment of four CM1K chips. Applications range from signal recognition and image analytics to massively parallel data mining and sensor fusion. For MatLab users, a toolbox interfaces seamlessly with a single NeuroStack board or a stack of multiple NeuroStack boards.

FEATURES

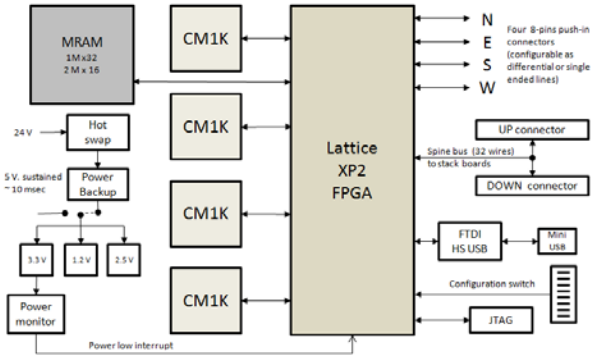
- Chain of 4096 neurons, expandable by stacking NeuroStack boards, reconfigurable by reprogramming the FPGA
- Field Programmable Gate Array (FPGA) to run data acquisition and recognition engines with direct access to chain(s) of neurons
- Non-volatile memory to store input data and/or results of the recognition such as object lists, snapshots showing objects of interest, anomaly reports, etc
- Connectors for interface to sensors and other external devices through single-ended wires or differential pairs such as LVSD, I2C or SPI or else
- USB communication with a host
- Stackable vertically to expand the neuron capacity and the number of run-time engines running on FPGA if applicable



The FPGA is programmed with a default configuration where the 4 CM1Ks are daisy-chained totaling 4096 operating neurons in parallel on a single board, with increment of 4096 neurons for each additional board stacked on top. A simple Read/Write protocol allows controlling the chain of CM1K chips through its 15 registers, as well as accessing to a “Pattern Cruncher” IP core featuring higher level functions to learn and recognize pattern vectors.

FPGA programmers can design their own recognition engines accessing to chains of CM1K chips trained to recognize different features from a same or different input data streams.

Functional diagram



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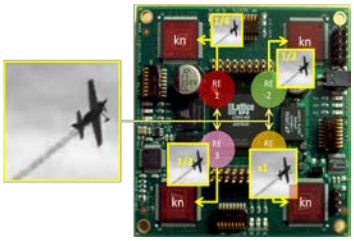
Components	CBX
Neural Network	Configurable chains of neurons with 1024 capacity increment
FPGA	Lattice XP2 FPGA with 40,000 logic elements
Non volatile memory	Two 2M x16bits EverSpin MRAM, 35 ns access time

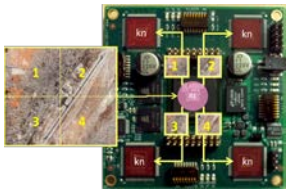
ANN Attributes	CM1K
Neuron capacity	4096
Neuron memory	256 bytes
Categories	15 bits
Distances	16 bits
Contexts	7 bits
Recognition status	Identified, Uncertain or Unknown
Classifiers	Radial Basis Function (RBF) K-Nearest Neighbor (KNN)
Distance Norms	L1 (Manhattan) or Lsup

Electrical and IOs	CBX
Clock frequency	10MHz
Communication	USB high speed 480 Mbit FTDI chip
Cardinal connectors	Four 8-pins push-in connectors configurable through dip switches as - 3 differential pairs and 2 single-ended wires - eight single-ended wires.
Spine connector	Two spring-loaded 18-pins connectors for vertical stack ability of up to 10 boards
Power supply	Via USB for single board 24V otherwise
Power	5 Watts
JTAG Programmer	Connector to program and debug the FPGA
Size	3”x3”

POSSIBLE CONFIGURATIONS FOR IMAGING APPLICATIONS

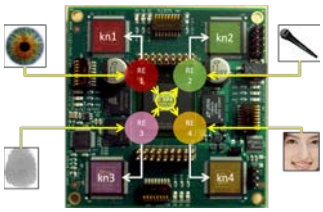


A video stream is broadcasted at different scales to 4 independent networks trained with a same knowledge. One of the network is expected to recognize the target as it gets further from or closer to the camera.

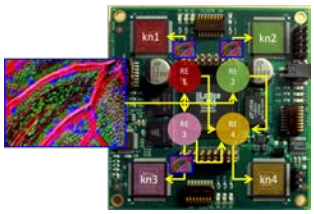


The four quadrants of a large aerial image are broadcasted to 4 independent networks trained with a same knowledge. Recognition time is accelerated by 4.

3 video channels and 1 audio channel are digitized and analyzed by 4 independent networks to recognize individuals. A positive identification is reported if all networks are in agreement with the identified person.



A medical image is analyzed by 3 independent networks trained to recognize different features in cells. Their responses are consolidated by a 4th network.



SOFTWARE

- Default driver
  - Simple API supporting a Register Transfer Level protocol to access the chain of CM1K chips of a single board or a stack of boards. Includes examples in C++ and C#.
- Optional NeuroStack Toolkit for MatLab
  - API to access high-level functions for the learning and recognition of pattern vectors, save and restore of neuron contents, and more.
- Optional Pattern Learning System
  - Application to load vectors from files formatted in csv or text format, and execute batch processes for the learning of reference dataset and recognition of testing datasets. The application produces diagnostics reports about the accuracy and throughput of the knowledge.