# Design of a 256-point 8-bit precision FFT

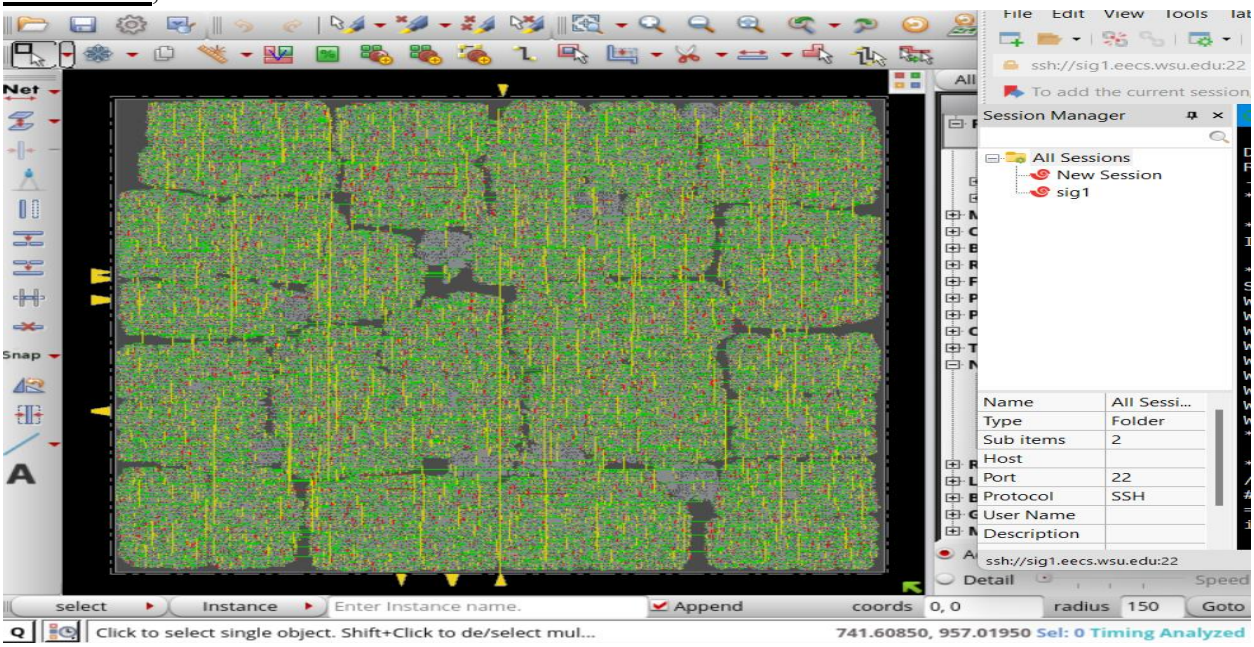
After preCTS optimization, the **WNS, TNS,** and **density** are shown below.

```
+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.002  |  0.002  |  0.084  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  75702  |  75702  |  75702  |
+--------------------+---------+---------+---------+

+-----------------+--------------------------------+--------------------+
|                 |              Real              |       Total        |
|    DRVs         +------------------+-------------+--------------------|
|                 |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)    |
+-----------------+------------------+-------------+--------------------+
|   max_cap       |      0 (0)       |   0.000     |      0 (0)         |
|   max_tran      |      0 (0)       |   0.000     |      0 (0)         |
|   max_fanout    |   8281 (8281)    |    -63      |   8282 (8282)      |
|   max_length    |      0 (0)       |     0       |      0 (0)         |
+-----------------+------------------+-------------+--------------------+

Density: 66.842%
Routing Overflow: 0.00% H and 0.00% V
```

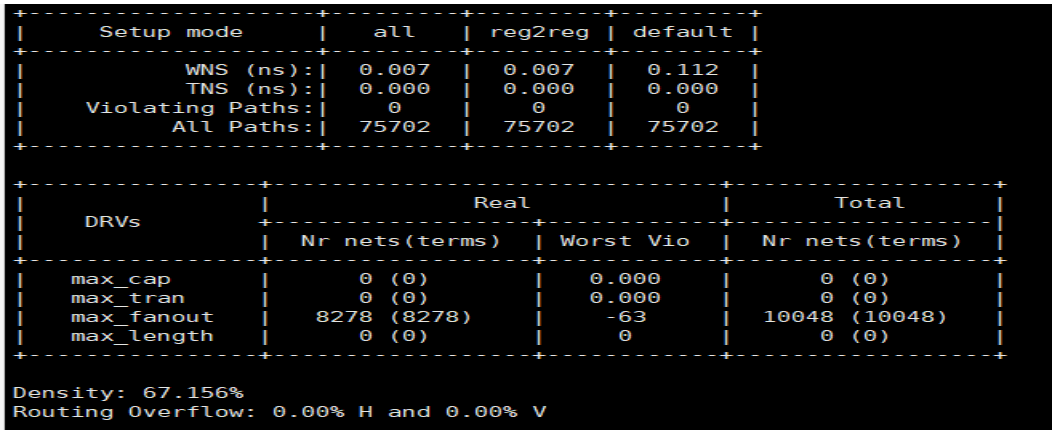
**PreCTS** optimization **power** is:

```
Total Power
-----------------------------------------------------------------------------------------
------
Total Internal Power:      327.98540488            76.7324%
Total Switching Power:      88.45687731            20.6945%
Total Leakage Power:        10.99830593             2.5731%
Total Power:               427.44058813
-----------------------------------------------------------------------------------------
------
```

**After CTS**, the **clock tree** is shown below

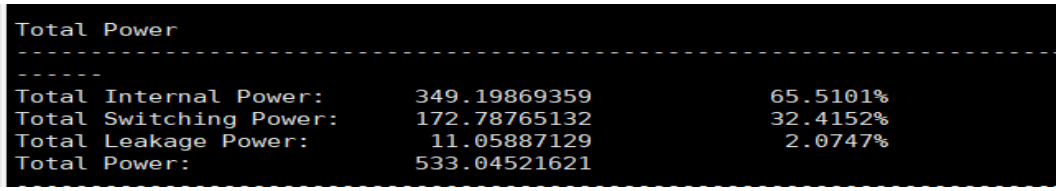


The **WNS, TNS** and **density** are shown below.



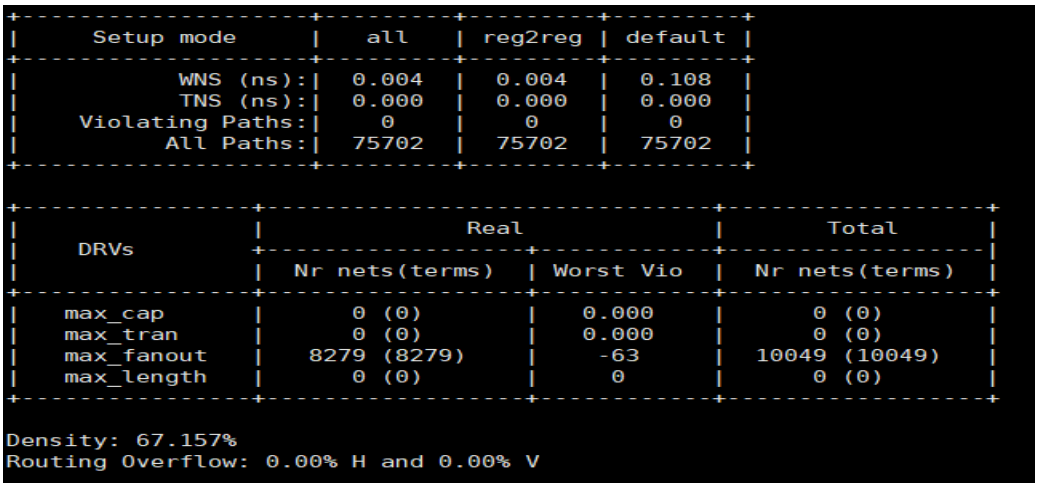
```
+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.007  |  0.007  |  0.112  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  75702  |  75702  |  75702  |
+--------------------+---------+---------+---------+

+-----------------+----------------------------------+-------------------+
|                 |               Real               |       Total       |
|    DRVs         +------------------+-------------+-------------------|
|                 |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)   |
+-----------------+------------------+-------------+-------------------+
|   max_cap       |      0 (0)       |   0.000     |      0 (0)        |
|   max_tran      |      0 (0)       |   0.000     |      0 (0)        |
|   max_fanout    |   8278 (8278)    |    -63      |   10048 (10048)   |
|   max_length    |      0 (0)       |     0       |      0 (0)        |
+-----------------+------------------+-------------+-------------------+

Density: 67.156%
Routing Overflow: 0.00% H and 0.00% V
```

The **Power** is shown as



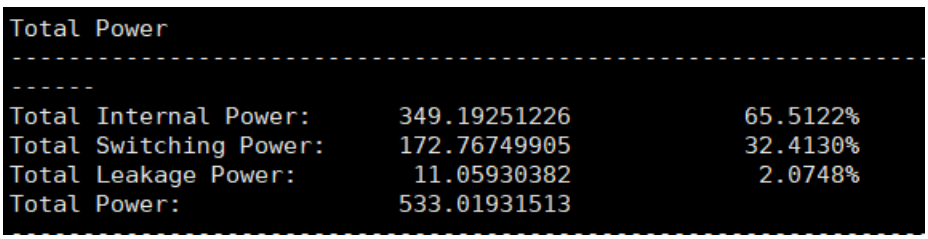
```
Total Power
-----------------------------------------------------------------------------
------
Total Internal Power:      349.19869359            65.5101%
Total Switching Power:     172.78765132            32.4152%
Total Leakage Power:        11.05887129             2.0747%
Total Power:               533.04521621
-----------------------------------------------------------------------------
```

After **postCTS** optimization, the **WNS**, **TNS** and **Density** is given by:



```
+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.004  |  0.004  |  0.108  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  75702  |  75702  |  75702  |
+--------------------+---------+---------+---------+

+-----------------+----------------------------------+-------------------+
|                 |               Real               |       Total       |
|    DRVs         +------------------+-------------+-------------------|
|                 |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)   |
+-----------------+------------------+-------------+-------------------+
|   max_cap       |      0 (0)       |   0.000     |      0 (0)        |
|   max_tran      |      0 (0)       |   0.000     |      0 (0)        |
|   max_fanout    |   8279 (8279)    |    -63      |   10049 (10049)   |
|   max_length    |      0 (0)       |     0       |      0 (0)        |
+-----------------+------------------+-------------+-------------------+

Density: 67.157%
Routing Overflow: 0.00% H and 0.00% V
```

The **Power** is show as:



```
Total Power
-----------------------------------------------------------------------------
------
Total Internal Power:      349.19251226            65.5122%
Total Switching Power:     172.76749905            32.4130%
Total Leakage Power:        11.05930382             2.0748%
Total Power:               533.01931513
-----------------------------------------------------------------------------
```

After **Routing**: the layout is given as:


**WNS, TNS** and **density** after routing is shown as:

```
+--------------------+----------+----------+----------+
|     Setup mode     |   all    | reg2reg  | default  |
+--------------------+----------+----------+----------+
|           WNS (ns):|  0.415   |  0.415   |  0.604   |
|           TNS (ns):|  0.000   |  0.000   |  0.000   |
|    Violating Paths:|    0     |    0     |    0     |
|          All Paths:|  75702   |  75702   |  75702   |
+--------------------+----------+----------+----------+

+-----------------+--------------------------------+--------------------+
|                 |              Real              |       Total        |
|    DRVs         +--------------------+-----------+--------------------|
|                 |  Nr nets(terms)    | Worst Vio |  Nr nets(terms)    |
+-----------------+--------------------+-----------+--------------------+
|   max_cap       |       0 (0)        |   0.000   |       0 (0)        |
|   max_tran      |       0 (0)        |   0.000   |       0 (0)        |
|   max_fanout    |    8279 (8279)     |    -63    |    10049 (10049)   |
|   max_length    |       0 (0)        |     0     |       0 (0)        |
+-----------------+--------------------+-----------+--------------------+

Density: 67.157%
```

The **power** after routing is given as:

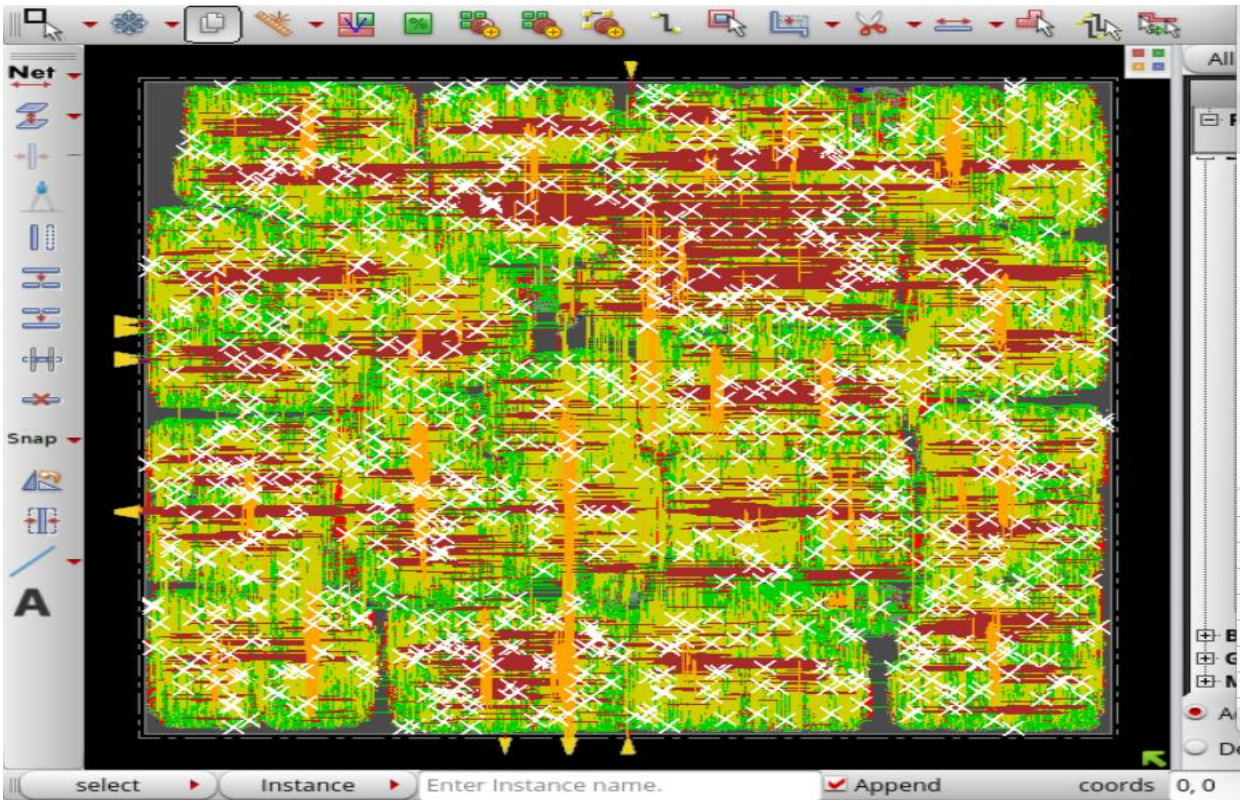
```
        Power Units = 1mW

        Time Units = 1e-09 secs

        report_power

-------------------------------------------------------------------------------
-----


Total Power
-------------------------------------------------------------------------------
-----
Total Internal Power:      348.31655461            66.1326%
Total Switching Power:     167.31847505            31.7677%
Total Leakage Power:        11.05930382             2.0998%
Total Power:               526.69433348
-------------------------------------------------------------------------------
```

**Wire length** is shown as:

```
#Post Route wire spread is done.
#Total number of nets with non-default rule or having extra spacing = 1826
#Total wire length = 3789735 um.
```

After **postRoute** optimization

The layout is shown as:




**WNS, TNS** and **Density** after postRoute Optimization is given by

```
+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.415  |  0.415  |  0.604  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  75702  |  75702  |  75702  |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |   8279 (8279)    |    -63     |  10049 (10049)   |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 67.157%
-----------------------------------------------------------------------
```

The **power** after postRoute optimization is given as:

```
Total Power
-----------------------------------------------------------------------
------
Total Internal Power:      348.31532647           66.1335%
Total Switching Power:     167.31041539           31.7667%
Total Leakage Power:        11.05930382            2.0998%
Total Power:               526.68504568
-----------------------------------------------------------------------
```