HIGH-VOLTAGE MIXED-SIGNAL IC

UC8230s

240RGB x 320 TFT LCD Controller-Driver
w/ 18-bit per RGB On-Chip SRAM

PP Specifications
Revision 0.8

June 30, 2009

ULTRACHIP

The Coolest LCD Drive, Ever!!

TABLE OF CONTENT

UC8230s

Single-Chip, Ultra-Low Power
240RGB x 320 Gate Matrix
Active Color LCD Controller-Driver

INTRODUCTION

The UC8230s handles 262,144 TFT colors and can drive a TFT color liquid crystal display of 240 RGB x 320 dots with an incorporated RAM compliant to graphics display of 240 RGB x 320 dots at maximum, and a 720-channel source driver outputs. The UC8230s incorporates a gate driver and a power circuit for driving liquid crystal display to drive a TFT panel with a single chip.

The UC8230s' bit-operation functions, 8/9/16/18-bit high-speed bus interface, and high-speed RAM-write functions enable efficient transfer of data and high-speed data update on a graphics RAM. The UC8230s' 6/16/18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and DB17 to 0) and VSYNC interface (system interface + VSYNC) provide an interface for moving picture display.

With a window address function that facilitates the moving picture display in an arbitrary area and enables simultaneous display of moving pictures and the contents of the internal RAM, the UC8230s enables moving picture display not constrained by the still picture area. Accordingly, the data transmission is reduced to minimum, thereby saving power consumed by a system as a whole when displaying moving pictures.

The UC8230s supports power-saving operation up to the power supply voltage of 2.5V with a voltage follower circuit that generate voltage to drive liquid crystal. The UC8230s also incorporates 8-color display and standby functions that allow precise power control by software.

These features make this LSI the ideal solution for any medium or small-sized portable battery-driven products such as digital cellular phones supporting WWW browsers or small PDA, where long battery life and board size are major concern.

MAIN APPLICATIONS

- Cellular Phones and other battery operated hand held devices or portable Instruments.

FEATURE HIGHLIGHTS

- Liquid crystal controller/driver for 262,144 TFT-color 240RGB x 320-dot graphics display
- Single chip solution for a TFT display panel
- System interface
  - 8-/9-/16-/18-bit high-speed bus interface
  - Serial Peripheral Interface (SPI)
  - 8-bit transmission x 3 times (262k/65k color modes)
- Interface for moving picture display
  - 6-/16-/18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
  - VSYNC interface (System interface + VSYNC)
- Window address function to write data to the rectangular area of RAM specified by the window address
  - Interface to facilitate moving picture display in an arbitrary area
  - Reduce data transmission by transmitting only the data for the moving picture display area
  - Simultaneous display of moving pictures and the contents of the internal RAM
- Functions for controlling abundant color displays
  - Simultaneous availability of 262,144 colors with γ-correction function
  - Line-unit vertical scrolling

- Low-power architecture: features for low-power operation
  - V_{cc} = 2.5 ~ 3.3 V
    (internal logic regulator power supply circuit)
  - I/OV_{CC} = 1.65 ~ 3.3V
    (reference voltage for interface pin input)
  - V_{D4} = 4.2 ~ 5.2 V
    (Source/COMH/P16V-Pump drive voltage)
  - Power saving function
    (standby mode etc.)
  - Partial liquid crystal drive to display two screens at arbitrary positions
  - Voltage followers for liquid crystal drive power circuit to fend off the direct current from bleeder-resistors
- Step-up circuit generating liquid crystal drive voltage up to 6-time scale
- 172,800-byte internal RAM
- Incorporated liquid crystal display driver with 720 source outputs and 320 gate outputs
- n-raster-row liquid crystal AC drive, enabling polarity inversion by every arbitrary number of raster-rows
- Internal oscillation and hardware reset
- Reversible direction of signals between RAM and source driver
- Exclusive for Cst structure

ORDERING INFORMATION

Gold Bumped Die

Part Number	MTP	Description
UC8230sGAB	Yes	Gold bumped die, with MTP function.

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

MTP LIGHT & ESD SENSITIVITY

The MTP memory cell is sensitive to photon excitation and ESD. Under extended exposure to strong ambient light, or when TST4 pin is exposed to ESD strikes, the MTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light & ESD shields to realize full MTP content retention performance.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

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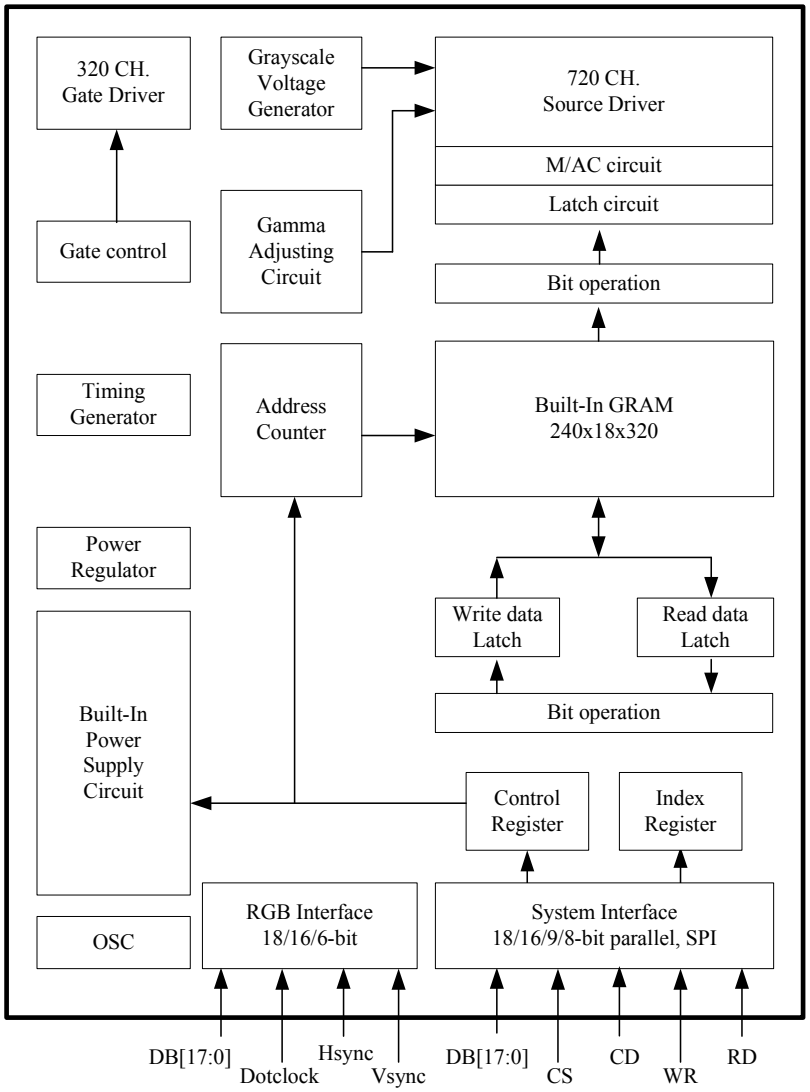
BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>Name</th><th>Type</th><th>Pads</th><th>Description</th></tr>
<tr><td colspan="4">POWER</td></tr>
<tr><td>V_{CC}</td><td>I</td><td>18</td><td>VD1-regulator / BGR / LVD power supply - external power supply. Range: 2.5v~3.3v</td></tr>
<tr><td>IOV_{CC}</td><td>I</td><td>6</td><td>Interface pin power supply - external power supply.
Range: 1.65~3.3</td></tr>
<tr><td>V_{SS}</td><td>GND</td><td>13</td><td>Chip ground</td></tr>
<tr><td>V_{S2}</td><td>GND</td><td>8</td><td>Pump ground</td></tr>
<tr><td>V_{D1}</td><td>O</td><td>11</td><td>Logic/memory power supply - connected internally to V_{D1} regulator output. 1.8V</td></tr>
<tr><td>V_{D2}</td><td>O</td><td>3</td><td>V_{D2} output pin</td></tr>
<tr><td>V_{D1_ON}
V_{D2_ON}</td><td>O</td><td>1
1</td><td>VD1 test pin (For Ultrachip test only)
VD2 test pin (For Ultrachip test only)</td></tr>
<tr><td>V_{D4}</td><td>O</td><td>6</td><td>Source/comH/VCCH-pump/VCCL-pump
Voltage: V_{D2} x 2</td></tr>
<tr><td>$V_{CC}H$</td><td>O</td><td>6</td><td>Gate high power supply.
Voltage: V_{D2}x 4,5,6</td></tr>
<tr><td>$V_{CC}L$</td><td>O</td><td>10</td><td>Gate low power supply.
Voltage: V_{D2} x -3,-4,-5</td></tr>
<tr><td>V_{SN}</td><td>O</td><td>5</td><td>comL power supply.
Voltage: V_{D2} x (-1)</td></tr>
<tr><td colspan="4">MPU-IF</td></tr>
<tr><td>IM3~0</td><td>I</td><td>4</td><td>Select MPU-IF mode
<table>
<tr><th>IM[3:0]</th><th>Bus Mode</th><th>DB Pin</th></tr>
<tr><td>0010</td><td>8080 / 16-bit</td><td>DB17-10,DB8-1</td></tr>
<tr><td>0011</td><td>8080 / 8-bit</td><td>DB17-10</td></tr>
<tr><td>010,ID</td><td>SPI</td><td>DB1~0</td></tr>
<tr><td>011*</td><td>Setting disabled</td><td></td></tr>
<tr><td>1010</td><td>8080 / 18-bit</td><td>DB17~0</td></tr>
<tr><td>1011</td><td>8080 / 9-bit</td><td>DB17-9</td></tr>
<tr><td>11**</td><td>Setting disabled</td><td></td></tr>
</table></td></tr>
<tr><td>CSb</td><td>I</td><td>1</td><td>Chip select, 500nS filter, R=25K(HR-Poly), C=20pF connect to V_{D1}</td></tr>
<tr><td>RS</td><td>I</td><td>1</td><td>Select IR/SR (RS_) or CRs (RS)</td></tr>
<tr><td>WR_SCL</td><td>I</td><td>1</td><td>80-system: write_; SPI: sync clock</td></tr>
<tr><td>RDb</td><td>I</td><td>1</td><td>80-system: read_; SPI: fixed to V_{D1} or V_{SS}</td></tr>
<tr><td>DB17~0</td><td>I/O</td><td>18</td><td>MPU data bus</td></tr>
<tr><td>SDI, SDO</td><td>I, O</td><td>1, 1</td><td>SDI : Serial Data Input. SDO : Serial Data Output</td></tr>
<tr><td>RESETb</td><td>I</td><td>2</td><td>Initialize chip</td></tr>
</table>

Name	Type	Pads	Description
DISPLAY-IF			
VSYNC	I	1	Frame synchronization signal
HSYNC	I	1	Line synchronization signal
DOTCLK	I	1	Dot clock
ENABLE	I	1	Enable signal in RGB-mode
FMARK	O	1	Frame head pulse with amplitude between GND and IOV_{CC}. Use when writing data to RAM in synchronization with FMARK. Leave open when not used.
REF / OSC			
VREG1	I/O	3	Reference voltage for generating gamma curve
EXTERNAL PUMPING CAPACITOR			
C11+, C11-	I/O	5, 5	Connect to external pumping capacitor C11
C12+, C12-	I/O	5, 5	Connect to external pumping capacitor C12
C13+, C13-	I/O	4, 4	Connect to external pumping capacitor C13
C21+, C21-	I/O	7, 7	Connect to external pumping capacitor C21
C22+, C22-	I/O	7, 7	Connect to external pumping capacitor C22
COMMON			
COM	O	7	TFT common electrode
COM_TEST	O	1	TFT common electrode test pin
VcomH	O	6	High level of Vcom
VcomL	O	4	Low level of Vcom
SOURCE			
S1~S720	O	720	TFT source electrode
VGS	I	2	Adjust gamma curve to match different panel
GATE			
G1~G320	O	320	TFT gate electrode
MISC.			
DUMMY	O	46	Dummy
OSC	I	1	Input pin for external clock input.
SRC_TEST	O	1	Source output test pin

CONTROL REGISTERS

UC8230s contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meanings and their default values. Commands supported by UC8230s will be described in the next two sections. First, a summary table, followed by a detailed instruction-by-instruction description.

Name: The Symbolic reference of the register.
Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
ID7-0	8	00h	Specifies index (R00h to RFFh) of the control register
OS	1	0h	”1” : Start power-up sequence,
AOF	1	0h	“1” : Auto power-off (Display off).
TE	1	0h	MTP Write Control **0 : Data-write End** 1 : Data-write Start
MTPS	1	0h	MTP Succeed
MAN	1	1h	**1 : Enable power setup & display sequence MANual mode**
DID	16	8230h	Device ID, = 8230h.
SS	1	0h	Shift direction of Source order: **0 : S1 to S720** 1 : S720 to S1 Rewrite the RAM data when change SS bit **SS=0** DB[17:0] = {S(3n), S(3n+1), S(3n+2)}, n=0…240 SS=1 DB[17:0] = {S(3n+2), S(3n+1), S(3n)}, n=240…0
SM	1	0h	Specifies the scan order of gate driver, **0 : progressive** 1 : interlace
EOR	1	0h	When "1", polarity inversion of a C-pattern waveform (B/C=1) occur by applying an EOR to an odd/even frame select signal and an N-line inversion signal.
BC0	1	0h	**0 : select frame inversion** 1 : select n-line inversion, and n-line =1
AM	1	0h	**0 : horizontally write to GRAM** 1 : vertically write to GRAM
I/D	2	3h	Address counter increment / decrement by 1 after write to GRAM *I/D1 : Vertical.* / *I/D0 : Horizontal.* 0 : decreasing / 0 : decreasing **1 : increasing** / **1 : increasing**
ORG	1	0h	Moves the origin address according to the ID setting when a window address area is made. **ORG = 0 : The origin address is not moved.** ORG = 1 : The origin address “h00000” is moved according to the I/D[1:0] setting.
BGR	1	0h	Reverses the order of RGB dots to BGR for the 18-bit data written to the internal GRAM **BGR=0 S(3n) : red S(3n+1) : green S(3n+2) : blue** BGR=1 S(3n) : blue S(3n+1) : green S(3n+2) : red

<table>
<tr><th>Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>DFM</td><td>1</td><td>0h</td><td>Specifies the Data Format when TRI=1 and using 8-bit or SPI interface
0 : 262k mode (6,6,6 transfer)
1 : 65k mode (5,6,5 transfer)</td></tr>
<tr><td>TRI</td><td>1</td><td>0h</td><td>The RAM write data for a pixel are transferred 3 times through the 8-bits bus when TRI=1.</td></tr>
<tr><td>RSZ</td><td>2</td><td>0h</td><td>RSZ sets the resizing factor.
00b : No resizing (x1) 01b : x 1/2
10b : Setting inhibited 11b : x 1/4</td></tr>
<tr><td>RCH</td><td>2</td><td>0h</td><td>Sets the number of pixels made as the remainder in horizontal direction when resizing a picture.
00b : 0 pixel 01b : 1 pixel
10b : 2 pixels 11b : 3 pixels</td></tr>
<tr><td>RCV</td><td>2</td><td>0h</td><td>Sets the number of pixels made as the remainder in vertical direction when resizing a picture.
00b : 0 pixel 01b : 1 pixel
10b : 2 pixels 11b : 3 pixels</td></tr>
<tr><td>D</td><td>2</td><td>0h</td><td>D1=1, display-on D1=0, display-off
00b : src=vss, internal-display/gate-cntl halt
01b : src=vss, internal-display/gate-cntl operate
10b : non-split display, internal-display/gate-cntl operate
11b : display, internal-display/gate-cntl operate</td></tr>
<tr><td>COL</td><td>1</td><td>0h</td><td>0 : 262k-color mode 1 : 8-color mode</td></tr>
<tr><td>GON/DTE</td><td>2</td><td>0h</td><td>Specifies the output of gate line
<table>
<tr><th>GON, DTE</th><th>Output of gate line</th></tr>
<tr><td>0xb</td><td>VCCH (GON=0, the Vcom level = Vss)</td></tr>
<tr><td>10b</td><td>VCCL</td></tr>
<tr><td>11b</td><td>VCCH or VCCL, depending on display</td></tr>
</table></td></tr>
<tr><td>VON</td><td>1</td><td>0h</td><td>Controls VCOMH, VCOML, VCOM amplitude signal output.
<table>
<tr><th>APE</th><th>AP[1:0]</th><th>VON</th><th>GND</th></tr>
<tr><td>0</td><td>*</td><td>*</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>GND</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Setting disabled</td></tr>
<tr><td>1</td><td>1~3</td><td>0</td><td>GND</td></tr>
<tr><td>1</td><td>1~3</td><td>1</td><td>VCOMH/VCOML</td></tr>
</table></td></tr>
<tr><td>BASEE</td><td>1</td><td>0h</td><td>0: No base image is displayed.
1 : A base image is displayed on the screen.</td></tr>
<tr><td>PTDE</td><td>2</td><td>0h</td><td>PTDE[0] : display enable bit of partial image 1.
PTDE[1] : display enable bit of partial image 2.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>BP
FP</td><td>4
4</td><td>8h
8h</td><td>BP specifies the number of scan line for back porch, BP ≥ 2.
FP specifies the number of scan line for front porch, FP ≥ 2.
4 ≤ (BP+FP) ≤ 16
<table>
<tr><td>0000b</td><td>Setting Disabled</td><td>1000b</td><td>8 lines</td></tr>
<tr><td>0001b</td><td>Setting Disabled</td><td>1001b</td><td>9 lines</td></tr>
<tr><td>0010b</td><td>2 lines</td><td>1010b</td><td>10 lines</td></tr>
<tr><td>0011b</td><td>3 lines</td><td>1011b</td><td>11 lines</td></tr>
<tr><td>0100b</td><td>4 lines</td><td>1100b</td><td>12 lines</td></tr>
<tr><td>0101b</td><td>5 lines</td><td>1101b</td><td>13 lines</td></tr>
<tr><td>0110b</td><td>6 lines</td><td>1110b</td><td>14 lines</td></tr>
<tr><td>0111b</td><td>7 lines</td><td>1111b</td><td>Setting Disabled</td></tr>
</table></td></tr>
<tr><td>ISC</td><td>4</td><td>0h</td><td>Specifies the scan cycle time of gate driver in non-display area.
<table>
<tr><td>0000b</td><td>0 frame</td><td>1000b</td><td>17 frames</td></tr>
<tr><td>0001b</td><td>3 frames</td><td>1001b</td><td>19 frames</td></tr>
<tr><td>0010b</td><td>5 frames</td><td>1010b</td><td>21 frames</td></tr>
<tr><td>0011b</td><td>7 frames</td><td>1011b</td><td>23 frames</td></tr>
<tr><td>0100b</td><td>9 frames</td><td>1100b</td><td>25 frames</td></tr>
<tr><td>0101b</td><td>11 frames</td><td>1101b</td><td>27 frames</td></tr>
<tr><td>0110b</td><td>13 frames</td><td>1110b</td><td>29 frames</td></tr>
<tr><td>0111b</td><td>15 frames</td><td>1111b</td><td>31 frames</td></tr>
</table></td></tr>
<tr><td>PTG</td><td>2</td><td>0h</td><td>Specifies the scan mode of gate driver in non-display area, and source / comV will be based on PT setting.
00b : normal drive 01b : fixed VCCL
10b : interval scan mode 11b : setting disable (=10b)</td></tr>
<tr><td>PTS</td><td>3</td><td>0h</td><td>Determines source output in non-display area when Partial Display is ON.
<table>
<tr><td rowspan="2">PTS</td><td colspan="2">Source Output</td></tr>
<tr><td>Positive</td><td>Negative</td></tr>
<tr><td>000b</td><td>V63</td><td>V0</td></tr>
<tr><td>001b</td><td>Disabled</td><td>Disabled</td></tr>
<tr><td>010b</td><td>Vss</td><td>Vss</td></tr>
<tr><td>011b</td><td>Hi-Z</td><td>Hi-Z</td></tr>
<tr><td>100b</td><td>V63</td><td>V0</td></tr>
<tr><td>101b</td><td>Disabled</td><td>Disabled</td></tr>
<tr><td>110b</td><td>Vss</td><td>Vss</td></tr>
<tr><td>111b</td><td>Hi-Z</td><td>Hi-Z</td></tr>
</table></td></tr>
<tr><td>FMI</td><td>3</td><td>0h</td><td>Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.
000 : 1 frame 001 : 2 frames
011 : 4 frames 101 : 6 frames</td></tr>
<tr><td>FMARKOE</td><td>1</td><td>0h</td><td>When FMARKOE = 1, the UC8230s starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>RIM</td><td>2</td><td>0h</td><td>Specifies the bus mode of RGB interface
00b : 18-bit bus RGB interface mode
01b : 16-bit bus RGB interface mode
10b : 6-bit bus RGB interface mode
11b : setting disable (=00b)</td></tr>
<tr><td>DM</td><td>2</td><td>0h</td><td>Specifies the Display operation Mode. DM allows switching between the internal clock operation and the external display interface mode.
00b : Internal clock operation 01b : RGB interface
10b : VSYNC interface 11b : Setting disabled (=00b)</td></tr>
<tr><td>RM</td><td>1</td><td>0h</td><td>Specifies the access interface of GRAM.
0 : MPU/VSYNC interface 1 : RGB interface</td></tr>
<tr><td>ENC</td><td>3</td><td>0h</td><td>Sets the RAM write cycle via RGB interface.
Set ENC to 0~7 to indicate 1~8 frames, respectively.</td></tr>
<tr><td>FMP</td><td>9</td><td>000h</td><td>Sets the output position of frame cycle signal (frame marker).
<table>
<tr><th>FMP[8:0]</th><th>FMARK Output Position</th></tr>
<tr><td>9’’h000</td><td>0th line</td></tr>
<tr><td>9’’h001</td><td>1st line</td></tr>
<tr><td>9’’h002</td><td>2nd lines</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>9’’h14E</td><td>334th lines</td></tr>
<tr><td>9’’h14F</td><td>335th lines</td></tr>
<tr><td>9’’h150~1FF</td><td>Setting disabled</td></tr>
</table></td></tr>
<tr><td>DPL</td><td>1</td><td>0h</td><td>Sets the signal polarity of DOTCLK pin.
0 : input data on the rising edge of DOTCLK
1 : input data on the falling edge of DOTCLK</td></tr>
<tr><td>EPL</td><td>1</td><td>0h</td><td>Sets the signal polarity of ENABLE pin.
<table>
<tr><th>EPL</th><th>ENABLE = 0</th><th>ENABLE = 1</th></tr>
<tr><td>0</td><td>Writes data DB17-0</td><td>Disables data write operation</td></tr>
<tr><td>1</td><td>Disables data write operation</td><td>Writes data DB17-0</td></tr>
</table></td></tr>
<tr><td>HSPL</td><td>1</td><td>0h</td><td>Sets the signal polarity of HSYNC pin.
0 : Low active 1 : High active</td></tr>
<tr><td>VSPL</td><td>1</td><td>0h</td><td>Sets the signal polarity of VSYNC pin.
0 : Low active 1 : High active</td></tr>
<tr><td>SLP</td><td>1</td><td>0h</td><td>1 : Enter Sleep mode, all operations stop except oscillator.</td></tr>
<tr><td>DSTB</td><td>1</td><td>0h</td><td>1 : Enter Standby mode, all operations stop.</td></tr>
<tr><td>AP</td><td>2</td><td>1h</td><td>Adjusts the bias current of amplifier in COMMON driver to increase / decrease driving capability.
00b : Stop 01b : TBD
10b : TBD 11b : TBD</td></tr>
<tr><td>APE</td><td>1</td><td>0h</td><td>Liquid crystal power supply enable bit. Set APE = 1 and follow the sequence when starting up the liquid crystal power supply.</td></tr>
</table>

Name	Bits	Default	Description
BT	3	0h	Switches the output factor for V_{CC}H_pump and V_{CC}L_pump circuits. *BT* / *V_{D4}_pump* / *V_{CC}H_pump* / *V_{CC}L_pump* **000 / V_{D2} x 2 / V_{D2} x 4 / V_{D2} x (-3)** 001 / V_{D2} x 2 / V_{D2} x 4 / V_{D2} x (-4) 010 / V_{D2} x 2 / V_{D2} x 5 / V_{D2} x (-3) 011 / V_{D2} x 2 / V_{D2} x 5 / V_{D2} x (-4) 100 / V_{D2} x 2 / V_{D2} x 5 / V_{D2} x (-5) 101 / V_{D2} x 2 / V_{D2} x 6 / V_{D2} x (-3) 110 / V_{D2} x 2 / V_{D2} x 6 / V_{D2} x (-4) 111 / V_{D2} x 2 / V_{D2} x 6 / V_{D2} x (-5)
SAP	1	0h	**0 : The grayscale voltage generating circuit is halted** 1 : Grayscale voltages are generated. When starting the operation of LCD power supply circuit in Power ON operation and so on, make sure SAP = 0. Set SAP = 1, after starting up the LCD power supply circuit.
LVDTEN	1	0h	1 : Low-V_{CC} detection control Enabled
VC	3	7h	Sets the Vref voltage.
DC0	2	2h	Sets the operating frequency of V_{D4}_pump and V_{SS}N_pump. 00b : sclk/2 01b : sclk/4 **10b : sclk/8** 11b : sclk/16
DC1	2	2h	Sets operation frequency of V_{CC}H_pump and V_{CC}L_pump. 00b : sclk/16 01b : sclk/32 **10b : sclk/64** 11b : sclk/128
VRH	4	Fh	Sets the Vreg1 voltage.
PON1	1	1h	0 : V_{D4}_pump OFF **1 :** V_{D4}_pump **ON**
PON2	1	1h	0 : V_{CC}H_pump and V_{CC}L_pump OFF **1 : V_{CC}H_pump and V_{CC}L_pump ON**
PON4	1	1h	0 : V_{SS}N_pump OFF **1 : V_{SS}N_pump ON**
PDC1	1	0h	1 : discharge V_{D4}_pump
PDC2	1	0h	1: discharge V_{CC}H_pump and V_{CC}L_pump
PDC4	1	0h	1: discharge V_{SS}N_pump
P5VMD	1	0h	P5V pump mode. **0: Single mode.** 1: Dual mode
VcomG	1	0h	Set VcomL voltage. **0: set VcomL to ground** 1: Set VcomL to (VcomH-VcomA)
VCM	6	37h	Sets VcomH voltage.
VDV	6	28h	Sets VcomA voltage.
AD	8	00h	Set GRAM address to address counter
AD	9	000h	Set GRAM address to address counter
WD	18	0000h	Transform the data into 18-bit before write to GRAM
RD	18	0000h	Read 18-bit data from GRAM

<table>
<tr><th>Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>PKP0~5
PFP1~2
PRP0~1
VRP0~1
PKN0~5
PFN1~2
PRN0~1
VRN0~1</td><td>3x5
2x2
3x2
5x2
3x5
2x2
3x2
5x2</td><td>0h</td><td>Fine-tune V1, V6, V8, V10, V12, V20, V43, V51, V53, V55, and V57
Specify PKP1, PKP4 gray-level
Gradient adjustment: V8, V55
Amplitude adjustment: V0, V63
Fine-tune V1, V6,V8, V10, V12, V20, V43, V51, V53, V55, and V57
Specify PKN1, PKN4 gray-level
Gradient adjustment: V8, V55
Amplitude adjustment: V0, V63</td></tr>
<tr><td>HAS, HEA</td><td>8</td><td>00h</td><td>Specifies the Horizontal Start / End position of a window</td></tr>
<tr><td>VSA, VEA</td><td>8</td><td>00h</td><td>Specifies the Vertical Start / End position of a window</td></tr>
<tr><td>SCN</td><td>6</td><td>00h</td><td>Sets the scanning starting position
<table>
<tr><th></th><th>SM=0, GS=0</th><th>SM=0, GS=1</th><th>SM=1, GS=0</th><th>SM=1, GS=1</th><th></th><th>SM=0, GS=0</th><th>SM=0, GS=1</th><th>SM=1, GS=0</th><th>SM=1, GS=1</th></tr>
<tr><td>6’h00</td><td>G1</td><td>G320</td><td>G1</td><td>G320</td><td>6’h14</td><td>G161</td><td>G160</td><td>G2</td><td>G319</td></tr>
<tr><td>6’h01</td><td>G9</td><td>G312</td><td>G17</td><td>G304</td><td>6’h15</td><td>G169</td><td>G152</td><td>G18</td><td>G303</td></tr>
<tr><td>6’h02</td><td>G17</td><td>G304</td><td>G33</td><td>G288</td><td>6’h16</td><td>G177</td><td>G144</td><td>G34</td><td>G287</td></tr>
<tr><td>6’h03</td><td>G25</td><td>G296</td><td>G49</td><td>G272</td><td>6’h17</td><td>G185</td><td>G136</td><td>G50</td><td>G271</td></tr>
<tr><td>6’h04</td><td>G33</td><td>G288</td><td>G65</td><td>G256</td><td>6’h18</td><td>G193</td><td>G128</td><td>G66</td><td>G255</td></tr>
<tr><td>6’h05</td><td>G41</td><td>G280</td><td>G81</td><td>G240</td><td>6’h19</td><td>G201</td><td>G120</td><td>G82</td><td>G239</td></tr>
<tr><td>6’h06</td><td>G49</td><td>G272</td><td>G97</td><td>G224</td><td>6’h1A</td><td>G209</td><td>G112</td><td>G98</td><td>G223</td></tr>
<tr><td>6’h07</td><td>G57</td><td>G264</td><td>G113</td><td>G208</td><td>6’h1B</td><td>G217</td><td>G104</td><td>G114</td><td>G207</td></tr>
<tr><td>6’h08</td><td>G65</td><td>G256</td><td>G129</td><td>G192</td><td>6’h1C</td><td>G225</td><td>G96</td><td>G130</td><td>G191</td></tr>
<tr><td>6’h09</td><td>G73</td><td>G248</td><td>G145</td><td>G176</td><td>6’h1D</td><td>G233</td><td>G88</td><td>G146</td><td>G175</td></tr>
<tr><td>6’h0A</td><td>G81</td><td>G240</td><td>G161</td><td>G160</td><td>6’h1E</td><td>G241</td><td>G80</td><td>G162</td><td>G159</td></tr>
<tr><td>6’h0B</td><td>G89</td><td>G232</td><td>G177</td><td>G144</td><td>6’h1F</td><td>G249</td><td>G72</td><td>G178</td><td>G143</td></tr>
<tr><td>6’h0C</td><td>G97</td><td>G224</td><td>G193</td><td>G128</td><td>6’h20</td><td>G257</td><td>G64</td><td>G194</td><td>G127</td></tr>
<tr><td>6’h0D</td><td>G105</td><td>G216</td><td>G209</td><td>G112</td><td>6’h21</td><td>G265</td><td>G56</td><td>G210</td><td>G111</td></tr>
<tr><td>6’h0E</td><td>G113</td><td>G208</td><td>G225</td><td>G96</td><td>6’h22</td><td>G273</td><td>G48</td><td>G226</td><td>G95</td></tr>
<tr><td>6’h0F</td><td>G121</td><td>G200</td><td>G241</td><td>G80</td><td>6’h23</td><td>G281</td><td>G40</td><td>G242</td><td>G79</td></tr>
<tr><td>6’h10</td><td>G129</td><td>G192</td><td>G257</td><td>G64</td><td>6’h24</td><td>G289</td><td>G32</td><td>G258</td><td>G63</td></tr>
<tr><td>6’h11</td><td>G137</td><td>G184</td><td>G273</td><td>G48</td><td>6’h25</td><td>G297</td><td>G24</td><td>G274</td><td>G47</td></tr>
<tr><td>6’h12</td><td>G145</td><td>G176</td><td>G289</td><td>G32</td><td>6’h26</td><td>G305</td><td>G16</td><td>G290</td><td>G31</td></tr>
<tr><td>6’h13</td><td>G153</td><td>G168</td><td>G305</td><td>G16</td><td>6’h27</td><td>G313</td><td>G8</td><td>G306</td><td>G15</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>6’h28~ 6’h3F</td><td>Setting disabled</td><td>Setting disabled</td><td>Setting disabled</td><td>Setting disabled</td></tr>
</table></td></tr>
<tr><td>NL</td><td>6</td><td>00h</td><td>Sets the number of lines to drive the LCD at an interval of 8 lines.</td></tr>
<tr><td>GS</td><td>1</td><td>0h</td><td>Sets the direction of scan by the gate driver.</td></tr>
<tr><td>REV</td><td>1</td><td>0h</td><td>Enables the grayscale inversion of the image by setting REV = 1.</td></tr>
<tr><td>VLE</td><td>1</td><td>0h</td><td>Vertical scroll display enable
0 :Fixed 1 : Enable scrolling</td></tr>
<tr><td>NDL</td><td>1</td><td>0h</td><td>Sets the source output level in non-lit display area.
Non-display area:
<table>
<tr><th>ND</th><th>Positive</th><th>Negative</th></tr>
<tr><td>0</td><td>V63</td><td>V0</td></tr>
<tr><td>1</td><td>V0</td><td>V63</td></tr>
</table></td></tr>
</table>

Name	Bits	Default	Description
VL	9	000h	Specifies the number of scrolling lines. **000h** **0 line** 001h 1 line 002h 2 lines … … 13dh 317 lines 13eh 318 lines 13fh 319 lines
PTDP0 PTDP1	9 9	000h 000h	Sets the display position of partial image 1. Sets the display position of partial image 2.
PTSA0 PTEA0	9 9	000h 000h	Sets the start line and end line addresses of the RAM area, respectively for the partial image 1. Ensure that PTSA0 ≤ PTEA0.
PTSA1 PTEA1	9 9	000h 000h	Sets the start line and end line addresses of the RAM area, respectively for the partial image 2. In setting, make sure that PTSA1 ≤ PTEA1.
FSEL	1	0h	FSEL: Sets OSC Frequency. **0 : OSC = 376 kHz** 1 : OSC = 600 kHz
RTNI	5	10h	Sets period H (line). 00000b~**10000b** **16 clock cycles** 10001b 17 clock cycles 10010b 18 clock cycles … … 11101b 29 clock cycles 11110b 30 clock cycles 11111b 31 clock cycles
DIVI	2	0h	Sets the division ratio of the internal clock frequency. DIVI Frequency **00b** **f-sclk/1** 01b f-sclk/2 10b f-sclk/4 11b f-sclk/8
NOWI	3	0h	Sets the non-overlap period of adjacent gate outputs. **000b** **0 internal clock** 001b 1 internal clock … … 110b 6 internal clock 111b 7 internal clock
MPCI	3	0h	Sets the source output timing by the number of internal clock from the reference point. **000b** **0 internal clock** 001b 1 internal clock … … 110b 6 internal clock 111b 7 internal clock

Name	Bits	Default	Description
VEQWI	2	0h	Set VCOM equalize period. **0 : 0 clock** 1 : 1 clock 2 : 2 clock 3 : 3 clock
RTNE	6	1Eh	Setting is enabled in display operation via RGB interface.
DIVE	2	0h	Set the division ratio of DTOCLK frequency.
NOWE	4	0h	Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.
MCPE	3	0h	Sets the source output timing by the number of internal clock from the reference point. The setting is enabled in display operation via RGB interface.
MTPC[1:0]	2	0h	MTP Command. **00b : Halt** 01b : Data-write 10b : Erase data 11b : Read MTP Cell
MTPEN	1	0h	1 : Enable MTP function.
MTPIGN	1	0h	**0 : Disable MTP Function** 1 : Enable MTP Function
MATCH	1	0h	**0 : if Read-out data do not match Program data** 1 : if Read-out data match Program data
RD_TIMER[7:0]	8	00h	MTP Timing setting
WR_TIMER[15:7]	8	00h	MTP Timing setting
MVDV[5:0]	6	00h	MTP for VDV
MVCM[6:0]	7	00h	MTP for VCM
MTP ID	2	0h	MTP ID
DAE	1	0h	DAta checksum engine Enable. **0 : Disabled** 1 : enabled
IRE	1	0h	IR checksum engine Enable. **0 : Disabled** 1 : Enabled
IRCK	8	00h	IR cheCKsum
DACK	16	0000h	DAta cheCKsum.

COMMAND TABLE

The following is a list of host commands supported by UC8230s:
R/W: Read Cycle / Write Cycle RS: 0: Index/Status / 1: Control Register

	Command	Reg.	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1.	Index	IR	W	0	0	0	0	0	0	0	0	0	ID[7: 0]								
2.	Status	SR	R	0	0	0	0	0	0	0	0	0	0	TE	MTPS	0	0	0	0	0	
3.	Set Display Enable	R00H	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	AOF	MAN	OS	
4.	Device Code Read	R00H	R	1	1	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	
5.	Drive Output Control	R01H	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0	0000H
6.	LCD Drive Waveform Control	R02H	W	1	0	0	0	0	0	1	BC0	EOR	0	0	0	0	0	0	0	0	0400H
7.	Entry Mode	R03H	W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	ID1	ID0	AM	0	0	0	0030H
8.	Resize Control	R04H	W	1	0	0	0	0	0	0	RCV[1:0]		0	0	RCH[1:0]		0	0	RSZ[1:0]		0000H
9.	Display Control (1)	R07H	W	1	0	0	PTDE[1:0]		0	0	0	BASE	0	VON	GON	DTE	COL	0	D1	D0	
10.	Display Control (2)	R08H	W	1	0	0	0	0	FP[3:0]				0	0	0	0	BP[3:0]				0808H
11.	Display Control (3)	R09H	W	1	0	0	0	0	0	0	PTS[1:0]		0	0	PTG[1:0]		ISC[3:0]				0000H
12.	Display Control (4)	R0AH	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMAR KOE	FMI[2:0]			
13.	Ext. Display Interface Ctrl 1	R0CH	W	1	0	ENC[2:0]			0	0	0	RM	0	0	DM[1:0]		0	0	RIM[1:0]		0000H
14.	Frame Marker Control	R0DH	W	1	0	0	0	0	0	0	0	FMP[8:0]									0000H
15.	Ext. Display Interface Ctrl 2	R0FH	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL	0000H
16.	Power Control (1)	R10H	W	1	0	0	0	SAP	0	BT[2:0]			APE	0	AP[1:0]		0	DSTB	SLP	0	0000H
	Power Control (2)	R11H	W	1	0	0	0	0	0	0	DC1[1:0]		0	0	DC0[1:0]		0	VC[2:0]			0000H
	Power Control (3)	R12H	W	1	P5V MD	0	0	0	0	PDC4	PDC2	PDC1	1	PON 4	PON2	PON1	VRH[3:0]				00F0H
	Power Control (4)	R13H	W	1	VCO MG	0	VDV[5:0]						0	0	VCM[5:0]						
17.	Setting Disable	R17H	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE	
18.	RAM Address Set - Horizontal	R20H	W	1	0	0	0	0	0	0	0	0	AD[7:0]								
19.	RAM Address Set - Vertical	R21H	W	1	0	0	0	0	0	0	0	AD[16:8]									
20.	RAM Data Write / Read	R22H	W	1	WR17-0																
			R	1	RD17-0																
21.	γ- Control (1)	R30H	W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]			00H
	γ- Control (2)	R31H	W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]			00H
	γ- Control (3)	R32H	W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]			00H
	γ- Control (4)	R33H	W	1	0	0	0	0	0	0	PFP1[1:0]		0	0	0	0	0	0	0	0	00H
	γ- Control (5)	R34H	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PFP2[1:0]		00H
	γ- Control (6)	R35H	W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]			00H
	γ- Control (7)	R36H	W	1	0	0	0	VRP1[4:0]					0	0	0	VRP0[4:0]					00H
	γ- Control (8)	R37H	W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]			00H
	γ- Control (9)	R38H	W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]			00H
	γ- Control (10)	R39H	W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]			00H
	γ- Control (11)	R3AH	W	1	0	0	0	0	0	0	PFN1[1:0]		0	0	0	0	0	0	0	0	00H
	γ- Control (12)	R3BH	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PFN2[1:0]		00H
	γ- Control (13)	R3CH	W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]			00H
	γ- Control (14)	R3DH	W	1	0	0	0	VRN1[4:0]					0	0	0	VRN0[4:0]					00H
22.	Checksum Control	R41H	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DAE	IRE	0000H
23.	IR Checksum	R42H	W	1	0	0	0	0	0	0	0	0	IRCK[7:0]								0000H
24.	DT Checksum	R43H	W	1	DACK[15:0]																0000H
25.	Windows Horizontal Start Addr.	R50H	W	1	0	0	0	0	0	0	0	0	HSA[7:0]								
26.	Windows Horizontal End Addr.	R51H	W	1	0	0	0	0	0	0	0	0	HEA[7:0]								
27.	Windows Vertical Start Addr.	R52H	W	1	0	0	0	0	0	0	0	VSA[8:0]									
28.	Windows Vertical End Addr.	R53H	W	1	0	0	0	0	0	0	0	VEA[8:0]									
29.	Driver Output Control	R60H	W	1	GS	0	NL[5:0]						0	0	SCN[5:0]						
30.	Base Image Display Control	R61H	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV	
31.	Vertical Scroll Control	R6AH	W	1	0	0	0	0	0	0	0	VL[8:0]									
32.	Partial Image 1 Display Position	R80H	W	1	0	0	0	0	0	0	0	PTDP0[8:0]									
33.	Partial Image 1 Start RAM Addr.	R81H	W	1	0	0	0	0	0	0	0	PTSA0[8:0]									
34.	Partial Image 1 End RAM Addr.	R82H	W	1	0	0	0	0	0	0	0	PTEA0[8:0]									
35.	Partial Image 2 Display Position	R83H	W	1	0	0	0	0	0	0	0	PTDP1[8:0]									
36.	Partial Image 2 Start RAM Addr.	R84H	W	1	0	0	0	0	0	0	0	PTSA1[8:0]									
37.	Partial Image 2 End RAM Addr.	R85H	W	1	0	0	0	0	0	0	0	PTEA1[80]									
38.	Panel Interface Control 1	R90H	W	1	0	0	0	0	FSEL	0	DIVI[1:0]		0	0	0	RTNI[4:0]					
	Panel Interface Control 2	R92H	W	1	0	0	0	0	0	NOWI[2:0]			0	0	0	0	0	0	0	0	
	Panel Interface Control 3	R93H	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI[2:0]			
	Panel Interface Control 4	R95H	W	1	0	0	0	0	0	0	DIVE[1:0]		0	0	RTNE[5:0]						
	Panel Interface Control 5	R97H	W	1	0	0	0	0	NOWE[3:0]				0	0	0	0	0	0	0	0	
	Panel Interface Control 6	R98H	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE[2:0]			

	Command	Reg.	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
39.	MTP Register	R46H	W	1	--	--	--	--	--	--	--	MATCH	--	--	MP1	MP0	--	--	MTPign	MTP_EN	
40.	MTP Timer	RC9H	W	1	WRTIMER								RDTIMER								
41.	MTP Cell	RCAH	W	1	MTPID [1:0]		MVDV[5:0]						--	--	--	MVCM[5:0]					

COMMAND DESCRIPTION

(1) INDEX (IR)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	0	0	0	0	0	0	0	0	ID[7:0]							

The index register specifies the index R00h to RFFh of the control register or RAM control to be accessed using a binary number from “0000_0000” to “1111_1111”. The access to the register and instruction bits in it is prohibited unless the index is specified in the index register.

(2) STATUS READ (SR)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	0	0	0	0	0	0	0	0	0	0	TE	MTPS	0	0	0	0	0

MTPS : MTP succeed

TE : MTP write control

0 : Data write end
1 : Data write Start

(3) SET DISPLAY ENABLE (R00H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	AOF	MAN	OS

OS : 1 - Start power-up sequence.

MAN : Manual mode.
0b : Auto mode 1b : Manual mode power setup & display sequence.

AOF : "1" - Auto Power Off (Display OFF).

(4) DRIVE CODE READ (R00H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	1	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0

The device code “8230”H is read out when reading out this register forcibly.

(5) DRIVE OUTPUT CONTROL (R01H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.

When SS = “0”, the source driver output shift from S1 to S720.
When SS = “1”, the source driver output shift from S720 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S720.

When SS = “0” and BGR = “0”, RGB dots are assigned one to one from S1 to S720.
When SS = “1” and BGR = “1”, RGB dots are assigned one to one from S720 to S1.

When changing the SS and BGR bits, RAM data must be rewritten.

SM: Controls the scan mode in combination with GS setting. See “ Scan mode setting”.

(6) LCD DRIVE WAVEFORM CONTROL (R02H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	1	BC0	EOR	0	0	0	0	0	0	0	0

EOR: Enables liquid-crystal line-inversion drive when EOR = 1 and BC0 = 1.

BC0: Selects the liquid crystal drive waveform VCOM.

BC = 0: frame inversion waveform is selected.
BC = 1: line inversion, line inverted=1

In either liquid crystal drive method; the polarity inversion is halted in blank period (back and front porch periods).

(7) ENTRY MODE (R03H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	ID1	ID0	AM	0	0	0

The entry mode register includes instruction bits for setting how to write data from the microcomputer to the internal GRAM of the UC8230s.

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the UC8230s writes data to the internal GRAM.

AM = “0”, sets the horizontal direction.
AM = “1”, sets the vertical direction.

When making a window address area, the data is written only within the area in the direction determined by I/D1-0, AM bits.

I/D[1:0]: Either increase (+1) or decrease (-1) the address counter (AC) automatically as the data is written to the GRAM. The I/D[0] bit sets either increment or decrement in horizontal direction (updates the address AD[7:0]). The I/D[1] bit sets either increment or decrement in vertical direction (updates the address AD[8:16]). The AM bit sets either horizontal or vertical direction in updating RAM address counter automatically when writing data to the internal RAM.

ORG: Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data within the window address area using high-speed RAM write function. Also see Figure 1 and Figure 2.

ORG = 0: The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.

ORG = 1: The origin address “h00000” is moved according to the I/D[1:0] setting.

Notes:

1. When ORG = 1, only the origin address “h00000” can be set in the RAM address set registers (R20h, R21h).

2. In RAM read operation, make sure to set ORG = 0.

BGR: Reverses the order from RGB to BGR in writing 18-bit pixel data in the GRAM.

BGR = 0: Write data in the order of RGB to the GRAM.
BGR = 1: Reverse the order from RGB to BGR in writing data to the GRAM.

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BGR = 0	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
BGR = 1	B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

DFM: In combination with the TRIREG setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface. Make sure to set DFM = 0 when not transferring data via 16-bit or 8-bit interface.

TRIREG: Selects the format to transfer data bits via 16-bit or 8-bit interface.

In 8-bit interface operation,

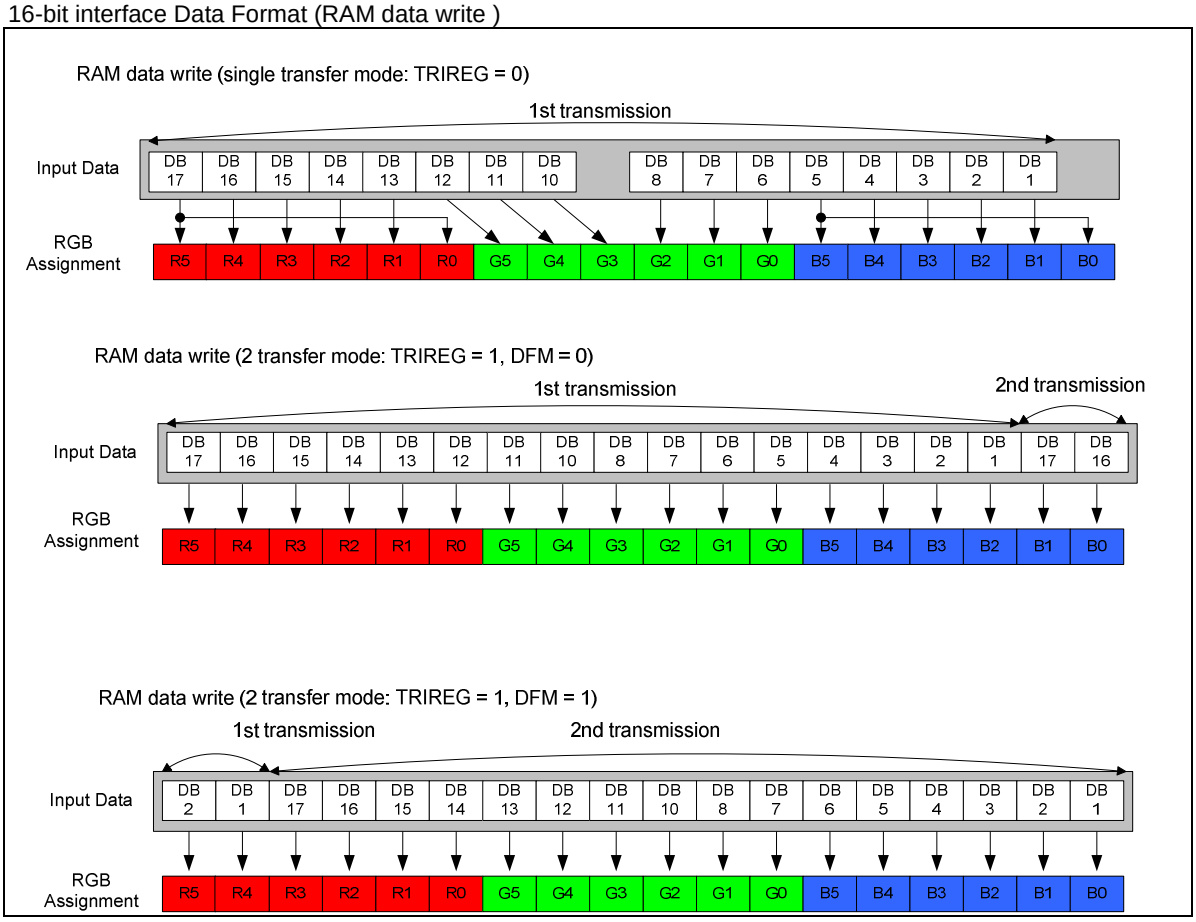
TRIREG = 0: 16-bit RAM data is transferred in two transfers.
TRIREG = 1: 18-bit RAM data is transferred in three transfers.

In 16-bit bus interface operation,

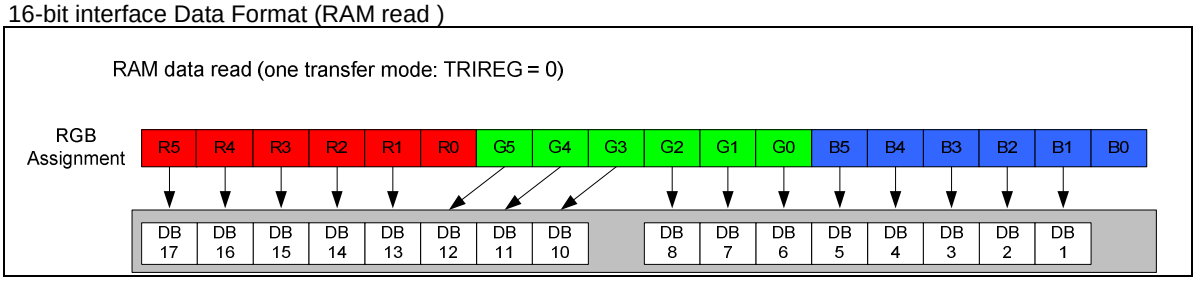
TRIREG = 0: 16-bit RAM data is transferred in one transfer.
TRIREG = 1: 18-bit RAM data is transferred in two transfers.

Make sure TRIREG = 0 when not transferring data via 16-bit or 8-bit interface. Also, set TRIREG = 0 during read operation.

16-bit interface Data Format (RAM data write)



16-bit interface Data Format (RAM read)



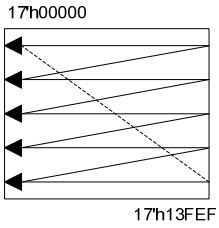
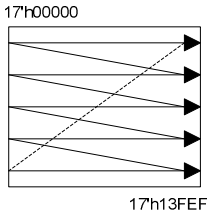
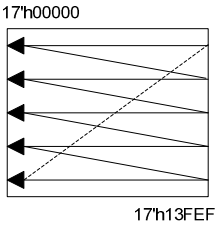
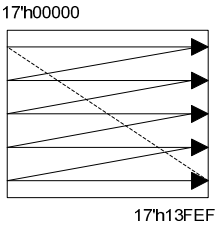
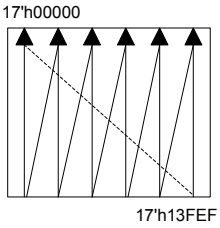
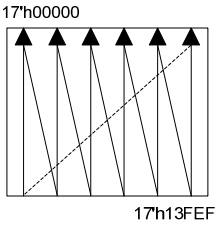
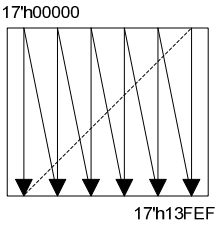
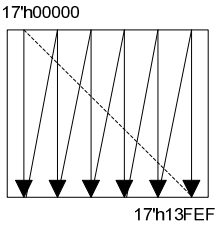
ORG=0	ID[1:0]=00b Horizontal : Decrease Vertical : Decrease	ID[1:0]=01b Horizontal : Increase Vertical : Decrease	ID[1:0]=10b Horizontal : Decrease Vertical : Increase	ID[1:0]=11b Horizontal : Increase Vertical : Increase
AM ="0" Horizontal				
AM ="1" Vertical				

Figure 1 Automatic address update (ORG = 0, AM, ID)

Note:

When writing data within the window address area with ORG = 0, any address within the window address area can be designated as the starting point of RAM write operation.

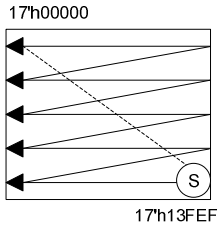
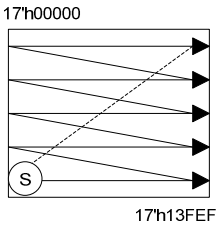
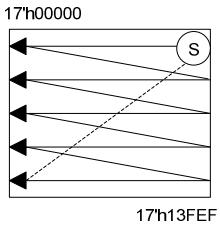
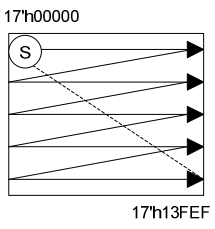
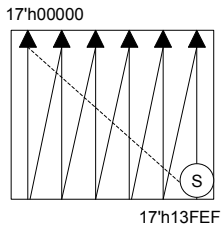
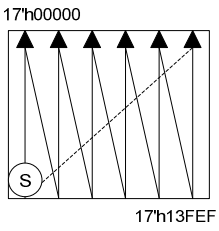
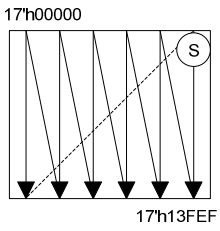
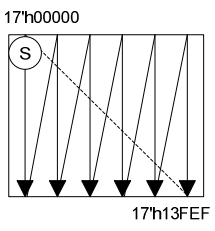
ORG=1	ID[1:0]=00b Horizontal : Decrease Vertical : Decrease	ID[1:0]=01b Horizontal : Increase Vertical : Decrease	ID[1:0]=10b Horizontal : Decrease Vertical : Increase	ID[1:0]=11b Horizontal : Increase Vertical : Increase
AM ="0" Horizontal				
AM ="1" Vertical				

Figure 2 Automatic address update (ORG = 1, AM, ID)

Notes:

1. When ORG = 1, make sure to set the address “h00000” in the RAM address set registers (R210h, R21h). Setting other addresses is inhibited.

2. When ORG = 1, the starting point of writing data within the window address area can be set at either corner of the window address area (“S” in circle in the above figure).

(8) RESIZE CONTROL (R04H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	RCV[1:0]		0	0	RCH[1:0]		0	0	RSZ[1:0]	

RSZ[1:0]: Sets the resizing factor. When the RSZ bits are set for resizing, the UC8230s writes the data according to the resizing factor so that the original image is displayed in horizontal and vertical dimensions contracted according to the factor . See “Resizing function”.

RCH[1:0]: Sets the number of pixels made as the remainder in horizontal direction when resizing a picture. By specifying the number of remainder pixels with RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2’h0 when not using the resizing function (RSZ = 2’h0) or there are no remainder pixels.

RCV[1:0]: Sets the number of pixels made as the remainder in vertical direction when resizing a picture. By specifying the number of remainder pixels with the RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2’h0 when not using the resizing function (RSZ = 2’h0) or there are no remainder pixels.

Table 1 Resizing factor (RSR)

RSZ [1:0]	Resizing Scale
2’b0	No resizing (x1)
2’b1	x 1/2
2’b2	Setting inhibited
2’b3	x 1/4

Table 2 Remainder Pixels in Horizontal Direction (RCH)

RCH [1:0]	Number of remainder Pixels in Horizontal Direction
2’b0	0 pixel
2’b1	1 pixel
2’b2	2 pixels
2’b3	3 pixels

Table 3 Remainder Pixels in Vertical Direction (RCV)

RCV [1:0]	Number of remainder Pixels in Vertical Direction
2’b0	0 pixel
2’b1	1 pixel
2’b2	2 pixels
2’b3	3 pixels

Note: 1 pixel = 1RGB

(9) DISPLAY CONTROL 1 (R07H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	PTDE[1:0]		0	0	0	BASEE	0	VON	GON	DTE	COL	0	D[1:0]	

D[1:0]: A graphics display is turned on when writing D1 = “1”, and is turned off when writing D1 = “0”. When writing D1 = “0”, the graphics display data is retained in the internal GRAM and the UC8230s displays the data when writing D1 = “1”. When D1 = “0”, i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D1-0 = 2’b01, the UC8230s continues internal display operation. When the display is turned off by setting D1-0 = 2’b00, the UC8230s’ internal display operation is halted completely. In combination with the GON setting, the D[1:0] setting controls display ON/OFF. For details, see “Instruction Setting”.

Table 4 Source output level and display operation

D[1:0]	BASEE	Source Output (S1-720)	FMARK signal	Internal Operation
2'h0	*	GND	Halt	Halt
2'h1	*	GND	Operation	Operation
2'h2	*	Non-lit display	Operation	Operation
2'h3	0	Non-lit display	Operation	Operation
	1	Base-image display	Operation	Operation

Notes:

1: The data write operation from the microcomputer is not affected by the D[1:0] setting.
2: The PTS bits set the source output level for "Non-lit display".
3: The LCD drive level during non-lit display period is determined by NDL setting.

COL: When COL = 1, 62 grayscale amplifiers other than V0 and V63 halt to display using less power. When setting 8-color display mode, follow the sequence of 8-color display mode setting.

Table 5

COL	Operating amplifier	Display color
0	32	262,144
1	2	8

Note: When COL = 1, do not write the data corresponding to the grayscales, for which the operation of amplifier is halted.

GON, DTE: The combination of GON and DTE settings set the output level form gate lines (G1 ~ G320). When GON = 0, the VCOM output level becomes the GND level.

Table 6

APE	GON	DTE	G1~G320
0	*	*	VGL (= GND)
1	0	0	VGH
	0	1	VGH
	1	0	VGL
	1	1	VGH/VGL

VON: Controls VCOMH, VCOML, VCOM amplitude signal output.

Table 7

APE	AP[1:0]	VON	VCOM output
0	*	*	GND
1	0	0	GND
	0	1	Setting disabled
	1 ~ 3	0	GND
	1 ~ 3	1	VCOMH/VCOML

BASEE: Base image display enable bit.

BASEE = 0: No base image is displayed. The UC8230s drives liquid crystal with non-lit display level or drives only partial image display areas.

BASEE = 1: A base image is displayed on the screen.

The D[1:0] setting has precedence over the BASEE setting.

PTDE[1:0]: PTDE[0] is the display enable bit of partial image 1. PTDE[1] is the display enable bit of partial image 2. When PTDE1/0 = 0, the partial image is turned off and only base image is displayed on the screen. When PTDE1/0 = 1, the partial image is displayed on the screen. In this case, turn off the base image by setting BASEE = 0.

(10) DISPLAY CONTROL 2 (R08H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FP[3:0]				0	0	0	0	BP[3:0]			

FP [3:0]: Sets the number of lines for a front porch period (a blank period following the end of display).
BP [3:0]: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

Note to Setting BP and FP : Set the BP and FP bits as follows in respective operation modes.

Table 8 BP and FP Settings

Internal clock operation mode	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
RGB interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Table 9 Front and Back Porch period (Line periods)

FP[3:0] BP[3:0]	Front and Back Porch period (Line periods)
4'h0	Setting inhibited
4'h1	Setting inhibited
4'h2	2 lines
4'h3	3 lines
4'h4	4 lines
4'h5	5 lines
4'h6	6 lines
4'h7	7 lines
4'h8	8 lines
4'h9	9 lines
4'hA	10 lines
4'hB	11 lines
4'hC	12 lines
4'hD	13 lines
4'hE	14 lines
4'hF	Setting inhibited

Note : The output timing to the LCD panel is delayed by two line periods from the synchronous signal (VSYNC) input timing.

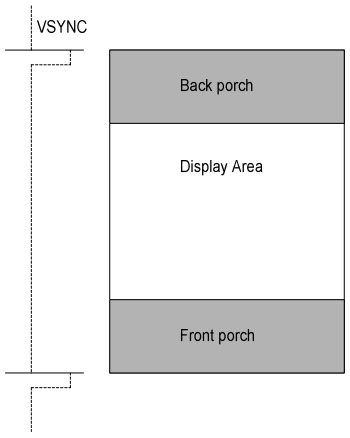


Figure 3 Front and Back Porch periods

(11) DISPLAY CONTROL 3 (R09H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	PTS[1:0]		0	0	PTG[1:0]		ISC[3:0]			

ISC [3:0]: Set the scan cycle when PTG[1:0] selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

Table 10

ISC[3:0]	Scan cycle	Time for interval when (fFLM) = 60Hz	ISC[3:0]	Scan cycle	Time for interval when (fFLM) = 60Hz
4'h0	Setting disabled	-	4'h8	17 frames	284mS
4'h1	3 frames	50mS	4'h9	19 frames	317mS
4'h2	5 frames	84mS	4'hA	21 frames	351mS
4'h3	7 frames	117mS	4'hB	23 frames	384mS
4'h4	9 frames	150mS	4'hC	25 frames	418mS
4'h5	11 frames	184mS	4'hD	27 frames	451mS
4'h6	13 frames	217mS	4'hE	29 frames	484mS
4'h7	15 frames	251mS	4'hF	31 frames	518mS

PTG[1:0]: Sets the scan mode in non-display area. The scan mode selected by PTG[1:0] bits is applied in the non-display area when the base image is turned off and the non-display area other than the first and second partial display areas.

Table 11

PTG[1]	PTG[0]	Scan mode in non-display area	Source output level in non-display area	VCOM output
0	0	Normal scan	PTS[2:0] setting	VCOMH/VCOML amplitude
0	1	Setting disabled	-	-
1	0	Interval scan	PTS[2:0] setting	VCOMH/VCOML amplitude
1	1	Setting disabled	-	-

Note: Select frame-inversion AC drive when interval scan is selected.

PTS[2:0]: Sets the source output level in non-display area drive period. When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

Table 12 Source output level and voltage generating operation in non-display drive period

PTS[2:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Pos. polarity	Neg. polarity		
3'h0	V63	V0	V0 to V63	Register setting (DC0, DC1)
3'h1	Setting inhibited	Setting inhibited	-	-
3'h2	GND	GND	V0 to V63	Register setting (DC0, DC1)
3'h3	Hi-Z	Hi-Z	V0 to V63	Register setting (DC0, DC1)
3'h4	V63	V0	V0 and V63	1/2 the frequency set by DC0, DC1
3'h5	Setting inhibited	Setting inhibited	-	-
3'h6	GND	GND	V0 and V63	1/2 the frequency set by DC0, DC1
3'h7	Hi-Z	Hi-Z	V0 and V63	1/2 the frequency set by DC0, DC1

Notes: 1. The power efficiency improved by halting grayscale amplifiers and slowing down the step-up clock frequency can be obtained in non-display drive period.
2. The gate output level in non-display drive period is controlled by the PTG setting (off-scan mode).

(12) DISPLAY CONTROL 4 (R0AH)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI[2:0]		

FMI[2:0]: Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

Table 13

FMI[2]	FMI[1]	FMI[0]	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting disabled

FMARKOE: When FMARKOE = 1, the UC8230s starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits.

(13) EXTERNAL DISPLAY INTERFACE CONTROL 1 (R0CH)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	ENC[2:0]			0	0	0	RM	0	0	DM[1:0]		0	0	RIM[1:0]	

RIM[1:0]: Sets the interface format when RGB interface is selected by RM and DM bits. Set RIM[1:0] bits before starting display operation via RGB interface. Do not change the setting while the UC8230s performs display operation.

Table 14 RGB interface operation

RIM[1:0]	RGB Interface operation	Colors
2'h0	18-bit RGB interface (1 transfer/pixel) via DB17-0	262,144
2'h1	16-bit RGB interface (1 transfer/pixel) via DB17-13 and DB11-1	65,536
2'h2	6-bit RGB interface (3 transfers/pixel) via DB17-12	262,144
2'h3	Setting inhibited	--

Notes: 1: Instruction bits are set via system interface.
2: Transfer the RGB dot data one by one in synchronization with DOTCLK in 6-bit RGB interface operation.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

Table 15 Display Interface

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting inhibited

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

Table 16 RAM Access Interface

RM	RAM Access Interface
0	System interface/VSYNC interface
1	RGB interface

ENC[2:0]: Sets the RAM write cycle via RGB interface.

Table 17 RAM Write Cycle

ENC[2:0]	RAM Write Cycle (frame periods)	ENC[2:0]	RAM Write Cycle (frame periods)
3'h0	1 frame	3'h4	5 frames
3'h1	2 frames	3'h5	6 frames
3'h2	3 frames	3'h6	7 frames
3'h3	4 frames	3'h7	8 frames

(14) FRAME MARKER CONTROL (R0DH)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	FMP[8:0]								

FMP[8:0]: Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9'h000, a high-active pulse FMARK is outputted at the start of back porch period for 1H period (IOVCC-IOGND amplitude signal). FMARK can be used as the trigger signal for frame synchronous write operation. See "FMARK" for details.

Make sure the setting restriction 9'h000 ≤ FMP ≤ BP+NL+FP.

Table 18

FMP[8:0]	FMARK output position
9' h000	0th line
9' h001	1st line
9' h002	2nd line
:	:
9' h14E	334th line
9' h14F	335th line
9' h150~1FF	Setting disabled

(15) EXTERNAL DISPLAY INTERFACE CONTROL 2 (R0FH)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

DPL: Sets the signal polarity of DOTCLK pin.
DPL = 0: input data on the rising edge of DOTCLK
DPL = 1: input data on the falling edge of DOTCLK

EPL: Sets the signal polarity of ENABLE pin.
EPL = 0: writes data DB17-0 when ENABLE = "0" and disables data write operation when ENABLE = "1".
EPL = 1: writes data DB17-0 when ENABLE = "1" and disables data write operation when ENABLE = "0".

HSPL: Sets the signal polarity of HSYNC pin.
HSPL = 0: low active
HSPL = 1: high active

VSPL: Sets the signal polarity of VSYNC pin.
VSPL = 0: low active
VSPL = 1: high active

(16) POWER CONTROL 1~4 (R10H ~ R13H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	LVDTEN	0	0	SAP	0	BT[2:0]			APE	0	AP[1:0]		0	DSTB	SLP	0
W	1	0	0	0	0	0	0	DC1 [1:0]		0	0	DC0[1:0]		0	VC[2:0]		
W	1	P5VMD	0	0	0	0	PDC4	PDC2	PDC1	1	PON4	PON2	PON1	VRH[3:0]			
W	1	VCOMG	0	VDV[5:0]						0	0	VCM[5:0]					

SLP: When SLP = 1, the UC8230s enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. No change to the GRAM data and instruction setting is accepted and he GRAM data and the instruction setting are maintained in sleep mode.

DSTB: When DSTB = 1, the UC8230s enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the UC8230s enters the deep standby mode, and they must be reset after exiting deep standby mode.

AP[1:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP1-0 = 2'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

Table 19 Constant current in amplifier in LCD power supply, grayscale voltage generating circuits

AP[1:0]	LCD power supply circuits	Grayscale voltage generating circuit
2'h0	Halt operation	Halt operation
2'h1	0.5	0.62
2'h2	0.75	0.71
2'h3	1	1

Note: In this table, the constant current in operational amplifiers is the ratio to the constant current when AP[1:0] is set to 2'h3.

APE: Liquid crystal power supply enable bit. Set APE = 1 and follow the sequence when starting up the liquid crystal power supply.

Table 20

APE	Liquid crystal power supply circuit	Grayscale voltage generating circuit
0	Halt	Halt
1	Operate	Operate

BT[3:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT	V_{D4}_pump	vcch_pump	vccl_pump
000	VD2 x 2	VD2 x 4	VD2 x (-3)
001	VD2 x 2	VD2 x 4	VD2 x (-4)
010	VD2 x 2	VD2 x 5	VD2 x (-3)
011	VD2 x 2	VD2 x 5	VD2 x (-4)
100	VD2 x 2	VD2 x 5	VD2 x (-5)
101	VD2 x 2	VD2 x 6	VD2 x (-3)
110	VD2 x 2	VD2 x 6	VD2 x (-4)
111	VD2 x 2	VD2 x 6	VD2 x (-5)

SAP: The grayscale voltage generating circuit is halted by setting SAP = 0. Grayscale voltages are generated when SAP = 1. When starting the operation of LCD power supply circuit in Power ON operation and so on, make sure SAP = 0. Set SAP = 1, after starting up the LCD power supply circuit.
LVDTEN: "1" - Low-VCC detection control Enabled.

VC[2:0] :

VC	VD4	VD2	VSN
7	5.5V	2.75V	– 2.75V
6	5.4V	2.7V	–2.7V
5	5.3V	2.65V	–2.65V
4	5.2V	2.6V	–2.6V
3	5.1V	2.55V	–2.55V
2	5.0V	2.5V	–2.5V
1	4.9V	2.45V	–2.45V
0	4.8V	2.4V	–2.4V

DC0[1:0] :

Table 21 Step-up V_{D4} and VssN

DC0[1:0]	Frequency
3'h0	sclk/2
3'h1	sclk/4
3'h2	sclk/8
3'h3	sclk/16

DC1[1:0] :

Table 22 Step-up VccH and VccL

DC1[1:0]	Frequency
3'h0	sclk/16
3'h1	sclk/32
3'h2	sclk/64
3'h3	sclk/128

Note: set operation frequency of VccH_pump and VccL_pump

VRH[3:0]: Sets the factor to generate VREG1OUT from VCILVL.

VRH	VREG1 (V)
15	5.250
14	5.100
13	4.950
12	4.800
11	4.650
10	4.500
9	4.350
8	4.200
7	4.050
6	3.900
5	3.750
4	3.600
3	3.450
2	3.300
1	3.150
0	3.000

PON:

PON1=0 : V_{D4}_pump OFF
PON2=0 : V_{CCH}_pump and V_{CCL}_pump OFF
PON4=0 : V_{SSN}_pump OFF

PON1=1 : V_{D4}_pump ON
PON2=1 : V_{CCH}_pump and V_{CCL}_pump ON
PON4=1 : V_{SSN}_pump ON

PDC:

PDC1=1 : discharge V_{D4}_pump
PDC4=1 : discharge V_{SSN}_pump

PDC2=1 : discharge V_{CCH}_pump

P5VMD: P5V pump mode.
0 : Single mode 1 : Dual mode

VCM[5:0]: set VcomH voltage,

VCOMG: set VcomL voltage
0 : set VcomL to ground 1 : set VcomL to (VcomH – VcomA)

VDV[4:0]: set VcomA voltage (VcomA = VcomH-VcomL).

VCM:

VCM[5:0]	VCOMH	VCM[5:0]	VCOMH	VCM[5:0]	VCOMH	VCM[5:0]	VCOMH
0	2.500	16	3.300	32	4.100	48	4.900
1	2.550	17	3.350	33	4.150	49	4.950
2	2.600	18	3.400	34	4.200	50	5.000
3	2.650	19	3.450	35	4.250	51	5.050
4	2.700	20	3.500	36	4.300	52	5.100
5	2.750	21	3.550	37	4.350	53	5.150
6	2.800	22	3.600	38	4.400	54	5.200
7	2.850	23	3.650	39	4.450	55	5.250
8	2.900	24	3.700	40	4.500	56	5.250
9	2.950	25	3.750	41	4.550	57	5.250
10	3.000	26	3.800	42	4.600	58	5.250
11	3.050	27	3.850	43	4.650	59	5.250
12	3.100	28	3.900	44	4.700	60	5.250
13	3.150	29	3.950	45	4.750	61	5.250
14	3.200	30	4.000	46	4.800	62	5.250
15	3.250	31	4.050	47	4.850	63	5.250

Table 23 VDV Setting

VDV[5:0]	VCOMA	VDV[5:0]	VCOMA	VDV[5:0]	VCOMA	VDV[5:0]	VCOMA
0	4.000	16	4.800	32	5.600	48	6.000
1	4.050	17	4.850	33	5.650	49	6.000
2	4.100	18	4.900	34	5.700	50	6.000
3	4.150	19	4.950	35	5.750	51	6.000
4	4.200	20	5.000	36	5.800	52	6.000
5	4.250	21	5.050	37	5.850	53	6.000
6	4.300	22	5.100	38	5.900	54	6.000
7	4.350	23	5.150	39	5.950	55	6.000
8	4.400	24	5.200	40	6.000	56	6.000
9	4.450	25	5.250	41	6.000	57	6.000
10	4.500	26	5.300	42	6.000	58	6.000
11	4.550	27	5.350	43	6.000	59	6.000
12	4.600	28	5.400	44	6.000	60	6.000
13	4.650	29	5.450	45	6.000	61	6.000
14	4.700	30	5.500	46	6.000	62	6.000
15	4.750	31	5.550	47	6.000	63	6.000

Note: Set VDV[4:0] so that VCOM amplitude becomes 6.0V or less.

(17) SETTING DISABLE (R17H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE

PSE: Power supply startup enable bit.

PSE = 1: The UC8230s' power supply is started by setting PON1, PON2, and PON4 when PSE =1. When completing the power supply generating operation, PSE is set to 0.

PSE = 0: Power supply sequencer is reset. When halting the operating power supply sequencer, set PSE = 0. When starting up power supply without power supply sequencer, set PSE = 0. The power sequencer enables the register settings sequentially at the designated timing and order.

(18) RAM ADDRESS SET - HORIZONTAL (R20H)

(19) RAM ADDRESS SET - VERTICAL (R21H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD[7:0]							
W	1	0	0	0	0	0	0	0	AD[16:8]								

AD[16:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the UC8230s writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note : 1. In RGB interface operation (RM = "1"), the address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.
2: In internal clock operation and VSYNC interface operation (RM = "0"), the address AD16-0 is set when executing the instruction.

Table 24 GRAM Address setting range

AD[16:0]	GRAM Data Setting
17'h00000 – 17'h000EF	Bitmap data on the first line
17'h00100 – 17'h001EF	Bitmap data on the second line
17'h00200 – 17'h002EF	Bitmap data on the third line
17'h00300 – 17'h003EF	Bitmap data on the fourth line
17'h00400 – 17'h004EF	Bitmap data on the fifth line
:	:
17'h13600 – 17'h13CEF	Bitmap data on the 317th line
17'h13700 – 17'h13DEF	Bitmap data on the 318th line
17'h13800 – 17'h13EEF	Bitmap data on the 319th line
17'h13900 – 17'h13FEF	Bitmap data on the 320th line

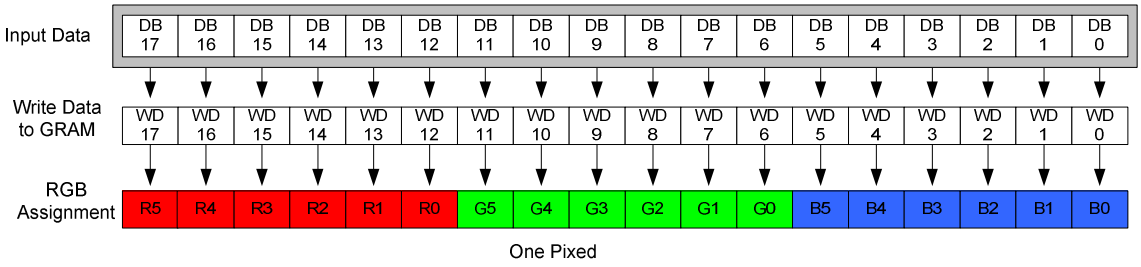
(20) RAM DATA WRITE/READ (R22H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	WD[17:0]															
R	1	RD[17:0]															

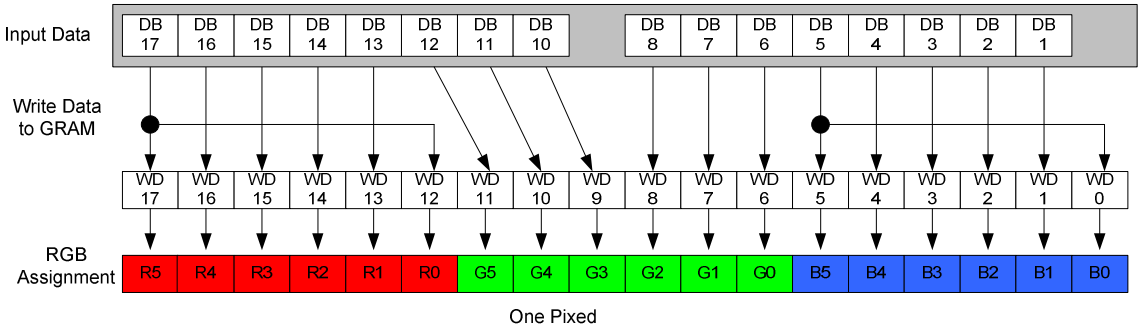
WD[17:0]: The UC8230s develops data into 18 bits internally in write operation. The format to develop data into 18 bits is different in different interface operation.

The GRAM data represents the grayscale level. The UC8230s automatically updates the address according to AM and I/D[1:0] settings as it writes data in the GRAM. The DFM bit sets the format to develop 16-bit data into the 18-bit data in 16-bit or 8-bit interface operation.

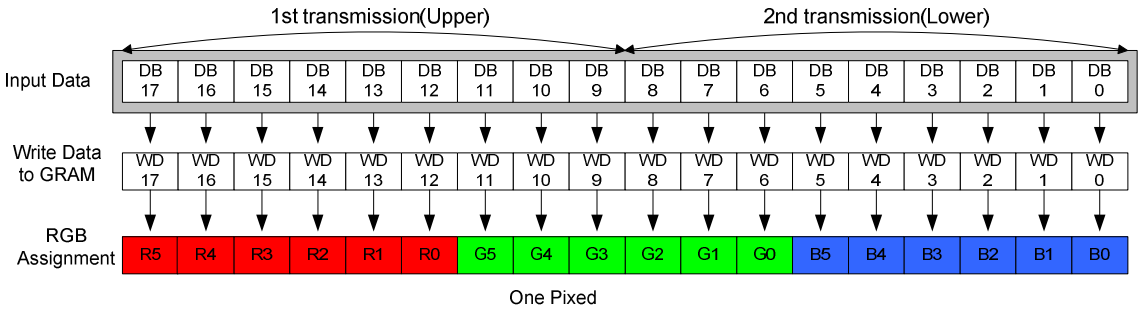
18-bit Interface (262,144 Colors)



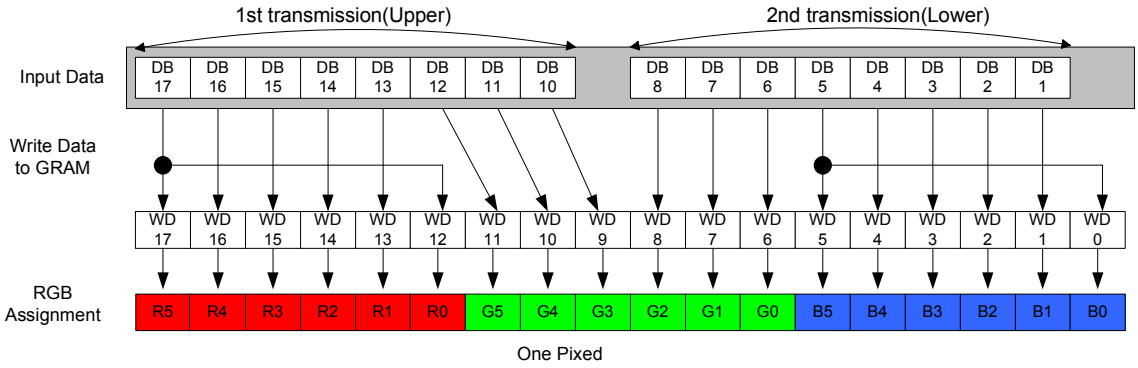
16-bit Interface (65,536 Colors)

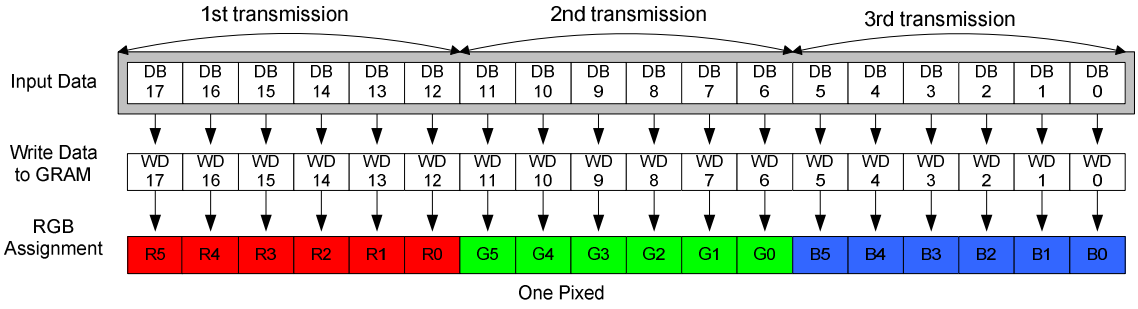


9-bit Interface (262,144 Colors)

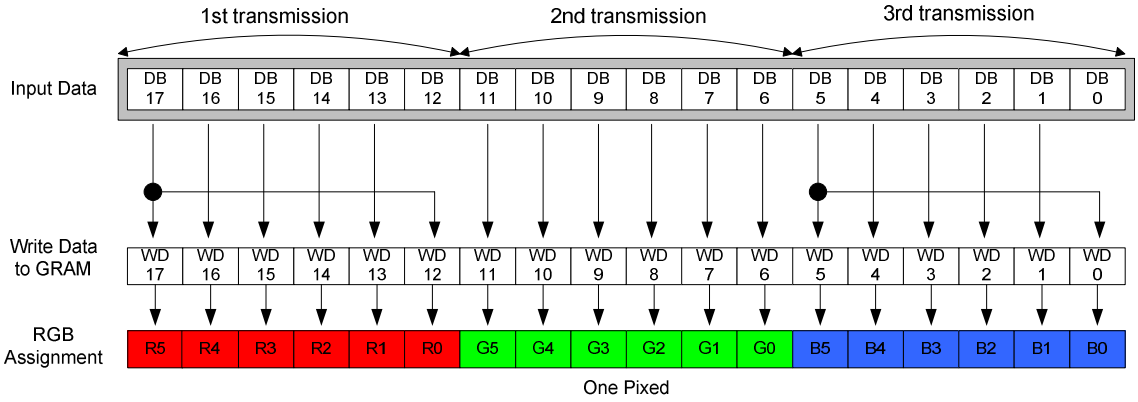


8-bit Interface (65,536 Colors) TRI=0

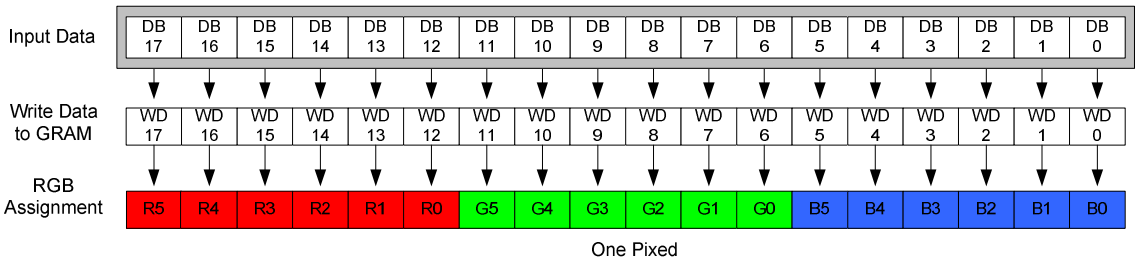




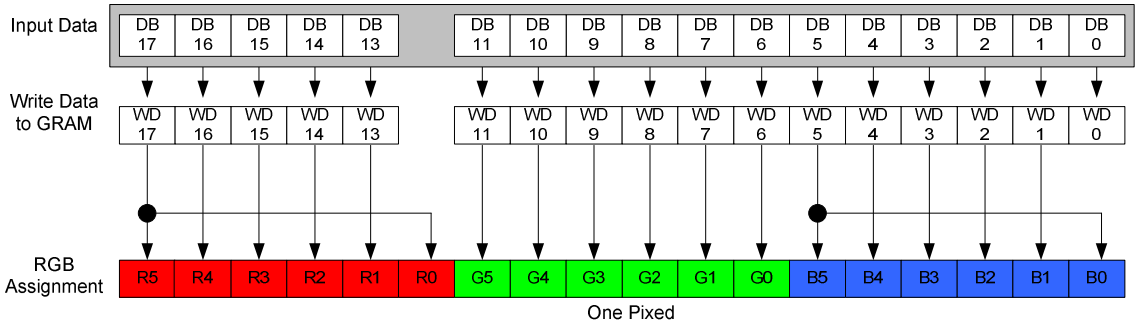
8-bit Interface (65,536 Colors) TRI=1



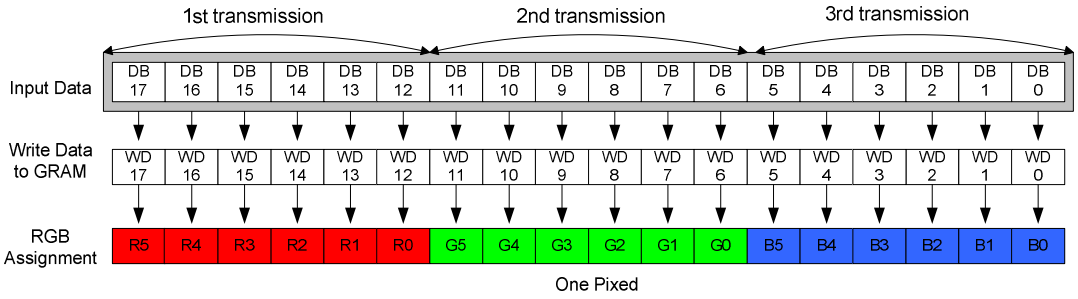
18-bit RGB Interface (262,144 Colors)



16-bit RGB Interface (65,536 Colors)



6-bit RGB Interface (262,144 Colors)



Note: When writing data in the GRAM via system interface while using the RGB interface, make sure that write operations via two interfaces do not conflict one another.

Table 25 Example of VREG1=5 Volt

Display Data	Grayscale			
	Negative polarity		Positive Polarity	
	Formula	Effect. Volt.	Formula	Effect. Volt.
0	V0	4.783	V63	0.652
1	V1	4.212	V62	1.114
2	V2	3.995	V61	1.352
3	V3	3.850	V60	1.510
4	V4	3.723	V59	1.649
5	V5	3.614	V58	1.768
6	V6	3.524	V57	1.867
7	V7	3.433	V56	1.966

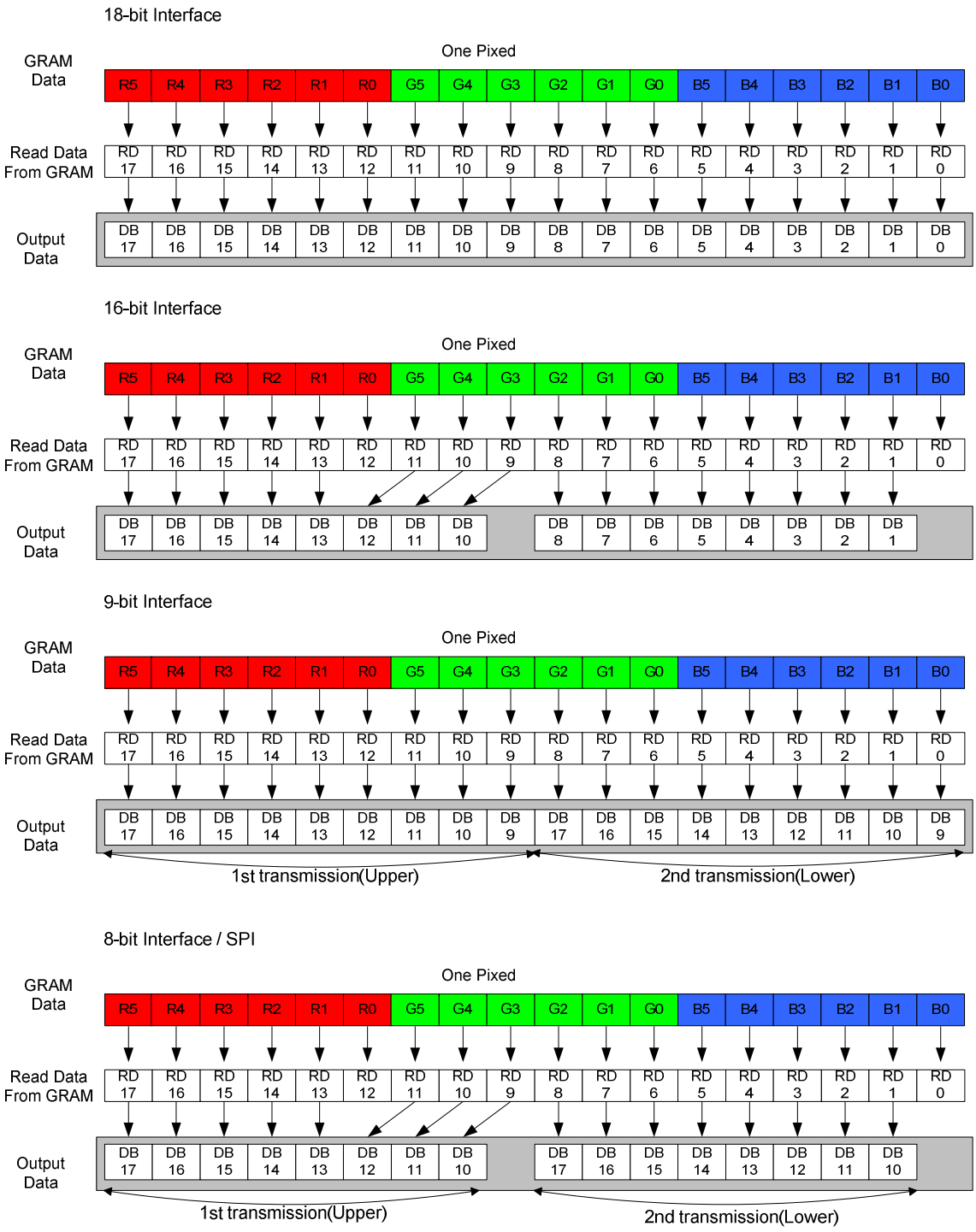
Display Data	Grayscale			
	Negative polarity		Positive Polarity	
	Formula	Effect. Volt.	Formula	Effect. Volt.
32	V32	2.690	V31	2.717
33	V33	2.663	V30	2.745
34	V34	2.636	V29	2.772
35	V35	2.609	V28	2.799
36	V36	2.582	V27	2.826
37	V37	2.554	V26	2.853
38	V38	2.527	V25	2.880
39	V39	2.500	V24	2.908

Display Data	Grayscale			
	Negative polarity		Positive Polarity	
	Formula	Effect. Volt.	Formula	Effect. Volt.
8	V8	3.342	V55	2.065
9	V9	3.315	V54	2.092
10	V10	3.288	V53	2.120
11	V11	3.261	V52	2.147
12	V12	3.234	V51	2.174
13	V13	3.207	V50	2.201
14	V14	3.179	V49	2.228
15	V15	3.152	V48	2.255
16	V16	3.125	V47	2.283
17	V17	3.098	V46	2.310
18	V18	3.071	V45	2.337
19	V19	3.043	V44	2.364
20	V20	3.016	V43	2.391
21	V21	2.989	V42	2.418
22	V22	2.962	V41	2.446
23	V23	2.935	V40	2.473
24	V24	2.908	V39	2.500
25	V25	2.880	V38	2.527
26	V26	2.853	V37	2.554
27	V27	2.826	V36	2.582
28	V28	2.799	V35	2.609
29	V29	2.772	V34	2.636
30	V30	2.745	V33	2.663
31	V31	2.717	V32	2.690

Display Data	Grayscale			
	Negative polarity		Positive Polarity	
	Formula	Effect. Volt.	Formula	Effect. Volt.
40	V40	2.473	V23	2.935
41	V41	2.446	V22	2.962
42	V42	2.418	V21	2.989
43	V43	2.391	V20	3.016
44	V44	2.364	V19	3.043
45	V45	2.337	V18	3.071
46	V46	2.310	V17	3.098
47	V47	2.283	V16	3.125
48	V48	2.255	V15	3.152
49	V49	2.228	V14	3.179
50	V50	2.201	V13	3.207
51	V51	2.174	V12	3.234
52	V52	2.147	V11	3.261
53	V53	2.120	V10	3.288
54	V54	2.092	V9	3.315
55	V55	2.065	V8	3.342
56	V56	1.966	V7	3.433
57	V57	1.867	V6	3.524
58	V58	1.768	V5	3.614
59	V59	1.649	V4	3.723
60	V60	1.510	V3	3.850
61	V61	1.352	V2	3.995
62	V62	1.114	V1	4.212
63	V63	0.652	V0	4.783

RD [17:0]: Read 18-bit data from GRAM. The bit assignment for the data that are read out from GRAM is different according to the interface.

When data are read out from GRAM to the microcomputer, the first word read immediately after GRAM address set are latched in the internal read-data latch, and thereby the data in the data bus (DB17–0) are nullified. The second word is read as valid data. When the UC8230s performs an internal bit processing, such as logical operation, the data latched in the read-data latch are used to complete it by single read out operation. The data are expanded internally into 18 bits before going through the logical operation. When the 8-/16-bit interfaces are selected, GRAM data in the LSB of R and B pixels are not read out. This function is not available in the RGB interface mode.



Read data from GRAM

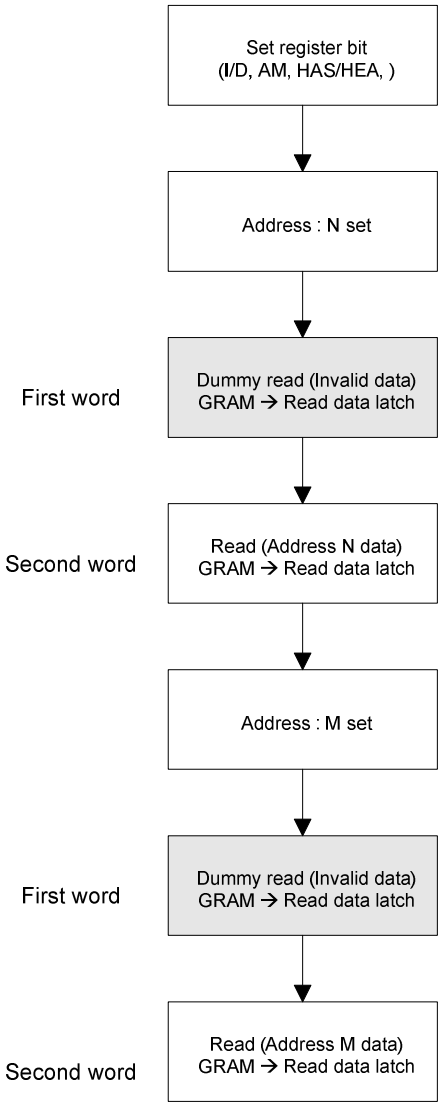


Figure 4. GRAM read sequence

(21) GAMMA CONTROL 1~10 (R30H~R3DH)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	0	PFP1[1:0]		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PFP2[1:0]	
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	VRP1[4:0]					0	0	0	VRP0[4:0]				
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	0	PFN1[1:0]		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PFN2[1:0]	
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRN1[4:0]					0	0	0	VRN0[4:0]				

PKP0 fine-tune V1
PKP1 fine-tune V6, V8, V10 or V12 depending on PFP1
PKP2 fine-tune V20
PKP3 fine-tune V43
PKP4 fine-tune V57, V55, V53 or V51 depending on PFP2
PKP5 fine-tune V55
PFP1 Specify PKP1 graylevel ('b00 : V6, 'b01:V8, 'b10 : V10, 'b11 : V12)
PFP2 Specify PKP4 graylevel ('b00 : V57, 'b01 : V55, 'b10 : V53, 'b11 : V51)
PRP0 Gradient adjustment: V8 Variable resistance
PRP1 Gradient adjustment: V55 Variable resistance
VRP0 Amplitude adjustment: V0 Variable resistance
VRP1 Amplitude adjustment: V63 Variable resistance
PKN0 fine-tune V1
PKN1 fine-tune V6,V8, V10 or V12 depending on PFN1
PKN2 fine-tune V20
PKN3 fine-tune V43
PKN4 fine-tune V57, V55, V53 or V51 depending on PFN2
PKN5 fine-tune V55
PFN1 Specify PKN1 graylevel ('b00 : V6, 'b01 : V8, 'b10 : V10, 'b11 : V12)
PFN2 Specify PKN4 graylevel ('b00 : V57, 'b01 : V55, 'b10 : V53, 'b11 : V51)
PRN0 Gradient adjustment: V8 Variable resistance
PRN1 Gradient adjustment: V55 Variable resistance
VRN0 Amplitude adjustment: V0 Variable resistance
VRN1 Amplitude adjustment: V63 Variable resistance

(22) CHECKSUM CONTROL (R41H)

(23) IR CHECKSUM (R42H)

(24) DT CHECKSUM (R43H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DAE	IRE
W	1	0	0	0	0	0	0	0	0	IRCK[7:0]							
W	1	DACK[15:0]															

IRE: Enable of the checksum engine for the Index
0 = off, checksum engine disabled.
1 = on, enable the checksum.

DAE: Enable of the checksum engine for the register content
0 = off, checksum engine disabled.
1 = on, enable the checksum.

IRCK: Checksum for the IR index
IRCK_new = IR XOR IRCK_old
This register is read-only for host and will be self cleared after read by user.

DACK: Checksum for the Register content write
DTCK_new = (Register Content Write) XOR DTCK_old
This register is read-only for host and will be self cleared after read by user.

(25) WINDOWS HORIZONTAL START ADDRESS (R50H)

(26) WINDOWS HORIZONTAL END ADDRESS (R51H)

(27) WINDOWS VERTICAL START ADDRESS (R52H)

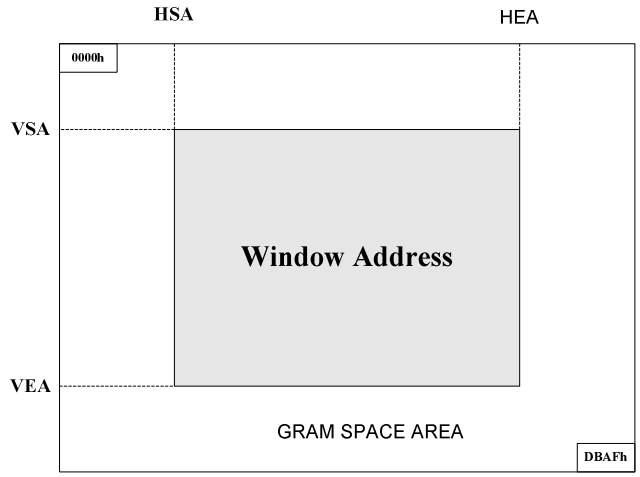
(28) WINDOWS VERTICAL END ADDRESS (R53H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	HSA[7:0]							
W	1	0	0	0	0	0	0	0	0	HEA[7:0]							
W	1	0	0	0	0	0	0	0	VSA[8:0]								
W	1	0	0	0	0	0	0	0	VEA[8:0]								

HSA[7:0], HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data.

Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that 8'h00 ≤ HAS < HEA ≤ 8'hEF and 8'h04 ≤ HEA – HSA.

VSA[8:0], VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that 9'h000 ≤ VSA < VEA ≤ 9'h13F.



Window address setting range:
00H ⩽ HAS[7:0] ⩽ HEA[7:0] ⩽ EFH
00H ⩽ VAS[8:0] ⩽ VEA[8:0] ⩽ 13FH

Figure 5 GRAM Address Map and Window Address Area

(29) DRIVER OUTPUT CONTROL (R60H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	GS	0	NL[5:0]						0	0	SCN[5:0]					

SCN[5:0]: Specifies the gate line where the gate driver starts scan.

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

GS: Sets the direction of scan by the gate driver. Set GS bit in combination with SM and SS bits for the convenience of the display module configuration and the display direction.

(30) BASE IMAGE DISPLAY CONTROL (R61H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the UC8230s to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by register setting (PTS).

Table 26 GRAM Data-grayscale level inversion

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000 : 18'h3FFFFF	V63 : V0	V0 : V63
1	18'h00000 : 18'h3FFFFF	V0 : V63	V63 : V0

VLE: Vertical scroll display enable bit. When VLE = 1, the UC8230s starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display.

Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

Table 27

VLE	Base image
0	Fixed
1	Enable scrolling

NDL: Sets the source output level in non-lit display area. NDL bit can keep the non-display area lit on.

Table 28

NDL	Non-display area	
	Positive	Negative
0	V63	V0
1	V0	V63

(31) VERTICAL SCROLL CONTROL (R6AH)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	VL[8:0]								

VL[8:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[8:0]. Make sure VL[8:0] ≤ 320.

Table 29

NL[5:0]	Number of Lines	NL[5:0]	Number of Lines	NL[5:0]	Number of Lines
6'h00	Setting inhibited	6'h0E	Setting inhibited	6'h1C	Setting inhibited
6'h01	Setting inhibited	6'h0F	Setting inhibited	6'h1D	240 (lines)
6'h02	Setting inhibited	6'h10	Setting inhibited	6'h1E	248
6'h03	Setting inhibited	6'h11	Setting inhibited	6'h1F	256
6'h04	Setting inhibited	6'h12	Setting inhibited	6'h20	264
6'h05	Setting inhibited	6'h13	Setting inhibited	6'h21	272
6'h06	Setting inhibited	6'h14	Setting inhibited	6'h22	280
6'h07	Setting inhibited	6'h15	176 lines	6'h23	288
6'h08	Setting inhibited	6'h16	Setting inhibited	6'h24	296
6'h09	Setting inhibited	6'h17	Setting inhibited	6'h25	304
6'h0A	Setting inhibited	6'h18	Setting inhibited	6'h26	312
6'h0B	Setting inhibited	6'h19	Setting inhibited	6'h27	320
6'h0C	Setting inhibited	6'h1A	Setting inhibited	6'h28-6'h3F	Setting inhibited
6'h0D	Setting inhibited	6'h1B	Setting inhibited		

Table 30

SCN [5:0]	Gate Line No (Scan start position) See note.				SCN [5:0]	Gate Line No (Scan start position) See note.			
	SM=0		SM=1			SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1		GS=0	GS=1	GS=0	GS=1
6'h00	G1	G320	G1	G320	6'h15	G169	G152	G18	G303
6'h01	G9	G312	G17	G304	6'h16	G177	G144	G34	G287
6'h02	G17	G304	G33	G288	6'h17	G185	G136	G50	G271
6'h03	G25	G296	G49	G272	6'h18	G193	G128	G66	G255
6'h04	G33	G288	G65	G256	6'h19	G201	G120	G82	G239
6'h05	G41	G280	G81	G240	6'h1A	G209	G112	G98	G223
6'h06	G49	G272	G97	G224	6'h1B	G217	G104	G114	G207
6'h07	G57	G264	G113	G208	6'h1C	G225	G96	G130	G191
6'h08	G65	G256	G129	G192	6'h1D	G233	G88	G146	G175
6'h09	G73	G248	G145	G176	6'h1E	G241	G80	G162	G159
6'h0A	G81	G240	G161	G160	6'h1F	G249	G72	G178	G143
6'h0B	G89	G232	G177	G144	6'h20	G257	G64	G194	G127
6'h0C	G97	G224	G193	G128	6'h21	G265	G56	G210	G111
6'h0D	G105	G216	G209	G112	6'h22	G273	G48	G226	G95
6'h0E	G113	G208	G225	G96	6'h23	G281	G40	G242	G79
6'h0F	G121	G200	G241	G80	6'h24	G289	G32	G258	G63
6'h10	G129	G192	G257	G64	6'h25	G297	G24	G274	G47
6'h11	G137	G184	G273	G48	6'h26	G305	G16	G290	G31
6'h12	G145	G176	G289	G32	6'h27	G313	G8	G306	G15
6'h13	G153	G168	G305	G16	6'h28-6'h3F	Setting disabled	Setting disabled	Setting disabled	Setting disabled
6'h14	G161	G160	G2	G319					

Note: Make sure that number of scan start position + number of scan end position is 320 lines or less.

(32) PARTIAL IMAGE 1 DISPLAY POSITION (R80H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTDP0[8:0]								

PTDP0[8:0]: Sets the display position of partial image 1.
PTDP1[8:0]: Sets the display position of partial image 2.

The display areas of the partial images 1 and 2 must not overlap each another. In setting, make sure that Partial image 1 display area < Partial image 2 display area, and

Coordinates of partial image 1 display position: (PTDP0, PTDP0 + (PTEA0 – PTSA0))
Coordinates of partial image 2 display position: (PTDP1, PTDP1 + (PTEA1 – PTSA1))

If PTDP0 = “9’h000”, the partial image 1 is displayed from the first line of the base image.

PTSA0[8:0] and PTEA0[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image 1. In setting, make sure that PTSA0 ≤ PTEA0.

PTSA1[8:0] and PTEA1[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image 2. In setting, make sure that PTSA1 ≤ PTEA1.

(33) PARTIAL IMAGE 1 START RAM ADDRESS (R81H)

(34) PARTIAL IMAGE 1 END RAM ADDRESS (R82H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTSA0[8:0]								
W	1	0	0	0	0	0	0	0	PTEA0[8:0]								

(35) PARTIAL IMAGE 2 DISPLAY POSITION (R83H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTDP1[8:0]								

(36) PARTIAL IMAGE 2 START RAM ADDRESS (R84H)

(37) PARTIAL IMAGE 2 END RAM ADDRESS (R85H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTSA1[8:0]								
W	1	0	0	0	0	0	0	0	PTEA1[8:0]								

(38) PANEL INTERFACE CONTROL 1 ~ 6 (R90H , R92H, R93H, R95, R97H, R98H)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FSEL	0	DIVI[1:0]		0	0	0	RTNI[4:0]				
W	1	0	0	0	0	0	NOWI[2:0]			0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI[2:0]		
W	1	0	0	0	0	0	0	DIVE[1:0]		0	0	RTNE[5:0]					
W	1	0	0	0	0	NOWE[3:0]				0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE[2:0]		

RTNI[4:0]: Sets 1H (line) period. This setting is enabled while the UC8230s' display operation is synchronized with internal clock.

DIVI[1:0]: Sets the division ratio of the internal clock frequency. The UC8230s' internal operation is synchronized with the frequency divided internal clock. When DIVI[1:0] setting is changed, the width of the reference clock for liquid crystal panel control signals is changed.

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too. For details, see "Frame-Frequency Adjustment Function". The setting in DIVI[1:0] is disabled in RGB interface operation.

Frame Frequency Calculation

$$\text{Frame frequency} = \frac{fosc}{\text{Clocks per line x division ratio x (line} + \text{BP} + \text{FP)}} \quad [\text{Hz}]$$

where, fosc : RC oscillation frequency
Line: Number of lines to drive the LCD (NL bits)
Division ratio: DIVI
Clocks per line: RTNI

Table 31 clocks per line (internal clock operation: 1 clock = 1 OSC)

RTNI[4:0]	Clocks per Line	RTNI[4:0]	Clocks per Line	RTNI[4:0]	Clocks per Line
5'h00-5'h0F	Setting inhibited	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

Table 32 Division ratio of the internal clock

DIVI[1:0]	Division Ratio	Internal operation clock unit
2'h0	1/1	1 OSC
2'h1	1/2	2 OSC
2'h2	1/4	4 OSC
2'h3	1/8	8 OSC

FSEL: Sets OSC Frequency.
0 : OSC = 376 kHz 1 : OSC = 600 kHz

NOWI[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation synchronizing with the internal clock.

Table 33

NOWI[2:0]	Non-overlap period	NOWI[2:0]	Non-overlap period
3'h0	0 (internal clock *see note)	3'h4	4 (internal clock *see note)
3'h1	1	3'h5	5
3'h2	2	3'h6	6
3'h3	3	3'h7	7

Note: The internal clock is the frequency divided clock, which is set by DIVI[[1:0] bits.

MCPI[2:0]: Sets the source output timing by the number of internal clock from the reference point. The setting is enabled in display operation synchronizing with the internal clock.

Table 34

MCPI[2:0]	Source output position	MCPI[2:0]	Source output position
3'h0	0 (internal clock *see note)	3'h4	4 (internal clock)
3'h1	1	3'h5	5
3'h2	2	3'h6	6
3'h3	3	3'h7	7

Note: The internal clock is the frequency divided clock, which is set by DIVI[[1:0] bits. The source output position is measured from the reference point by the number of internal clock cycle.

RTNE[5:0]: Sets RTNE[5:0] and DIVE[1:0] bits so that the number of DOTCLK calculated from the following formula becomes the number of DOTCLK which should be inputted in 1H period. The RTNE[5:0] setting is enabled in display operation via RGB interface.

DIVE[1:0] (division ratio) *x RTNE[5:0]* (Number of DOTCLK) ≤ *Number of DOTCLK in 1H period*

DIVE[1:0]: Sets the division ratio of DOTCLK frequency. The R61505U's internal operation is synchronized with the frequency divided DOTCLK. The setting in DIVE[1:0] is enabled in RGB interface operation.

Table 35 Division ratio of DOTCLK

DIVE [1:0]	Division Ratio	Internal operation clock unit (DOTCLK)			
		18-bit, 1 transfer RGB interface	DOTCLK = 5 MHz	8-bit, 3 transfers RGB interface	DOTCLK = 15 MHz
2'h0	Setting disabled	Setting disabled	-	Setting disabled	-
2'h1	1/4	4 DOTCLKs	0.8µs	12 DOTCLKs	0.8µs
2'h2	1/8	8 DOTCLKs	1.6µs	24 DOTCLKs	1.6µs
2'h3	1/16	16 DOTCLKs	3.2µs	48 DOTCLKs	3.2µs

Table 36 DOTCLK per line (1H period)

RTNE[5:0]	DOTCLK per line (1H)	RTNE[5:0]	DOTCLK per line (1H)
6'h00	Setting disabled	6'h20	32 clocks
6'h01	Setting disabled	6'h21	33 clocks
6'h02	Setting disabled	6'h22	34 clocks
6'h03	Setting disabled	6'h23	35 clocks
6'h04	Setting disabled	6'h24	36 clocks
6'h05	Setting disabled	6'h25	37 clocks
6'h06	Setting disabled	6'h26	38 clocks
6'h07	Setting disabled	6'h27	39 clocks
6'h08	Setting disabled	6'h28	40 clocks
6'h09	Setting disabled	6'h29	41 clocks
6'h0A	Setting disabled	6'h2A	42 clocks
6'h0B	Setting disabled	6'h2B	43 clocks
6'h0C	Setting disabled	6'h2C	44 clocks
6'h0D	Setting disabled	6'h2D	45 clocks
6'h0E	Setting disabled	6'h2E	46 clocks
6'h0F	Setting disabled	6'h2F	47 clocks
6'h10	16 clocks	6'h30	48 clocks
6'h11	17 clocks	6'h31	49 clocks
6'h12	18 clocks	6'h32	50 clocks
6'h13	19 clocks	6'h33	51 clocks
6'h14	20 clocks	6'h34	52 clocks
6'h15	21 clocks	6'h35	53 clocks
6'h16	22 clocks	6'h36	54 clocks
6'h17	23 clocks	6'h37	55 clocks
6'h18	24 clocks	6'h38	56 clocks
6'h19	25 clocks	6'h39	57 clocks
6'h1A	26 clocks	6'h3A	58 clocks
6'h1B	27 clocks	6'h3B	59 clocks
6'h1C	28 clocks	6'h3C	60 clocks
6'h1D	29 clocks	6'h3D	61 clocks
6'h1E	30 clocks	6'h3E	62 clocks
6'h1F	31 clocks	6'h3F	63 clocks

NOWE[3:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.

Table 37

NOWE[3:0]	Non-overlap period	NOWE[3:0]	Non-overlap period
4'h0	0 (clock *see note)	4'h8	8 (clocks *see note)
4'h1	1	4'h9	9
4'h2	2	4'hA	10
4'h3	3	4'hB	11
4'h4	4	4'hC	12
4'h5	5	4'hD	13
4'h6	6	4'hE	14
4'h7	7	4'hF	15

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) [DOTCLK].

MCPE[2:0]: Sets the source output timing by the number of internal clock from the reference point. The setting is enabled in display operation via RGB interface.

Table 38

MCPE[2:0]	Source output position	MCPE[2:0]	Source output position
3'h0	Setting Disabled	3'h4	4 (clocks *see note)
3'h1	1 clock	3'h5	5
3'h2	2	3'h6	6
3'h3	3	3'h7	7

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) [DOTCLK].

(39) MTP REGISTER (R46H)

(40) MTP TIMER (RC9H)

(41) MTP CELL (RCAH)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	–	–	–	–	–	–	–	MATCH	–	–	MP1	MP0	–	–	MTPign	MTP_EN
W	1	WR TIMER	WR TIMER	WR TIMER	WR TIMER	WR TIMER	WR TIMER	WR TIMER	WR TIMER	RD TIMER	RD TIMER	RD TIMER	RD TIMER	RD TIMER	RD TIMER	RD TIMER	RD TIMER
W	1	MTP ID1	MTP ID0	MVDV 5	MVDV 4	MVDV 3	MVDV 2	MVDV 1	MVDV 0	–	–	MVCM 5	MVCM 4	MVCM 3	MVCM 2	MVCM 1	MVCM 0

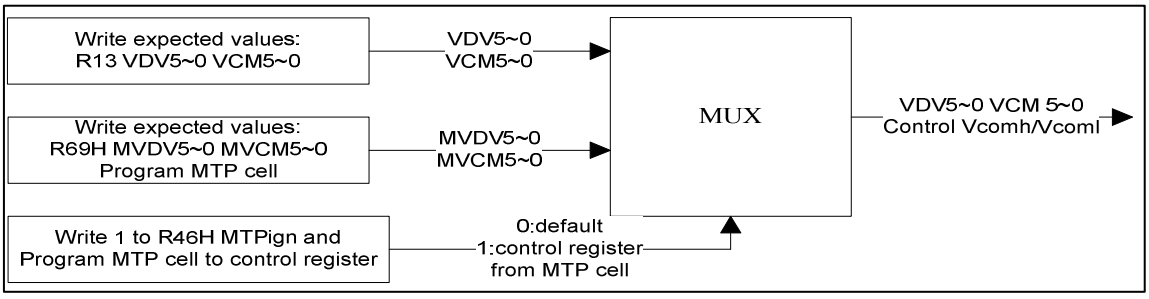
MTP_EN : MTP Write Control
0 : Data-write End 1 : Data-write Start

MTPign
0 : Disable MTP Function 1 : Enable MTP Function

MP [1:0] : will be cleared to 0 by the display driver after MTP operation
00 : Halt 01 : Data write
10 : Erase data 11 : Read MTP Cell

MATCH
0 : Read-out data do not match Program data 1 : Read-out data match Program data

RD_TIMER : Set MTP Read timing
WR_TIMER : Set MTP write timing
MVCM [5:0] : Set VCM
MVDV [5:0] : Set VDV
MTPID [1:0] : Set MTP ID



HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

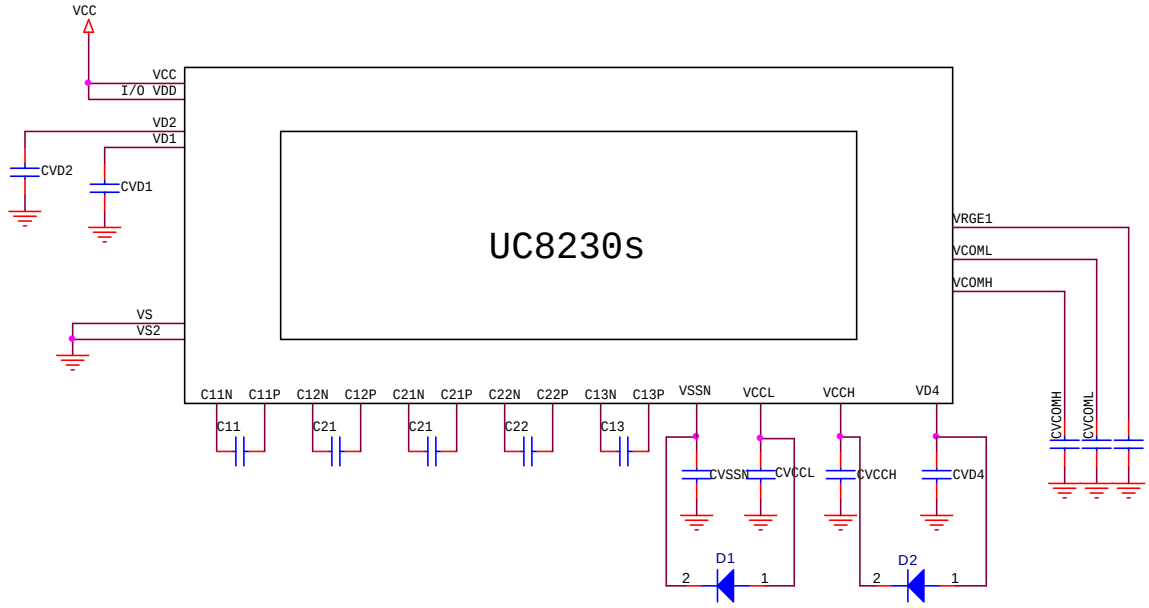


FIGURE 6: Sample circuit using internal Hi-V generator circuit

NOTE:
Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

1 µF/25V : CVD1, CVD2, C11, C21, C21, C22, C13, CVD4, CVSSN, CVCCL, CVCCH, CVOMH, CVOMH, CVREG1

Schottky diode (VF<0.4V/20mA at 25℃, VR ≥30V) : D1, D2

INTERFACES

INTERFACE SPECIFICATION

The UC8230s incorporates a system interface, which is used to set instructions, and an external display interface, which is used to display motion pictures. Selecting these interfaces to match the screen data (motion picture or still picture) enables efficient transfer of data for display.

The external display interface includes RGB interface and VSYNC interface. This allows flicker-free screen update.

When RGB interface is selected, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for use in operating the display. The data for display (DB17-0) is written according to the values of the data enable signal (ENABLE) and data valid signal (VLD), in synchronization with the VSYNC, HSYNC, and DOTCLK signals. In addition, using the window address function enables rewriting only to the internal RAM area to display motion pictures. Using this function also enables simultaneously display of the motion picture area and the RAM data that was written.

While displaying motion pictures, the data for display should be written in high-speed write mode, which achieves both low power consumption and high-speed access via RGB interface or VSYNC interface.

The internal display operation is synchronized with the frame synchronization signal (VSYNC) in VSYNC interface mode. When writing to the internal RAM is done within the required time after the falling edge of VSYNC, motion pictures can be displayed via the conventional interface. There are some limitations on the timing and methods of writing to RAM. See the section on the external display interface.

The UC8230s has four operation modes for each display state. These settings are specified by control instructions for external display interface. Transitions between modes should follow the transition flow.

RAM Access Selection and Display Operation Mode

Operation Mode	RAM Access Selection (RM)	Display Operation Mode (DM1-0)
Internal Clock Operation (Displaying still picture)	System interface (RM=0)	internal clock operation (DM1-0=00)
RGB interface(1) - (Display motion picture)	RGB interface (RM=1)	RGB interface (DM1-0=01)
RGB interface(2) - (Rewriting still picture while display motion picture)	System interface (RM=0)	RGB interface (DM1-0=01)
VSYNC interface (Displaying motion pictures)	System interface (RM=0)	VSYNC interface (DM1-0=10)

Note: 1) Set instruction registers only via system interface.

2) Do not use RGB interface and VSYNC interface at the same time.

3) Do not set RGB interface mode during operation.

4) For mode transitions, see the section on the external display interface.

HOST INTERFACE

As summarized in the table below, UC8230s supports two parallel bus protocols, in any of 18/16/9/8-bit bus width, and bus protocols.

Designers can either use parallel buses to achieve high data transfer rate, or use serial buses to create compact LCD modules.

		Bus Type				
		8080				**SPI**
Width		18-bit	16-bit	9-bit	8-bit	Serial
Access		Read / Write				
Control & Data Pins	IM[3:0]	1010	0010	1011	0011	010[ID]
	CS	Chip Select				
	RS	Index / Register				
	WR0	$\overline{WR}$				—
	WR1	$\overline{RD}$				—
	DATA	DB[17:0]	DB[17:10], [8:1]	DB[17:9]	DB[17:10]	SDI, SDO

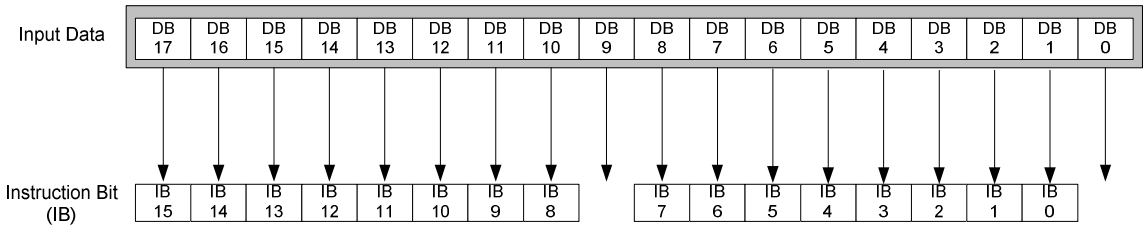
* Connect unused control pins and data bus pins to V_{D1} or V_{SS}

Table 39: Host interfaces Summary

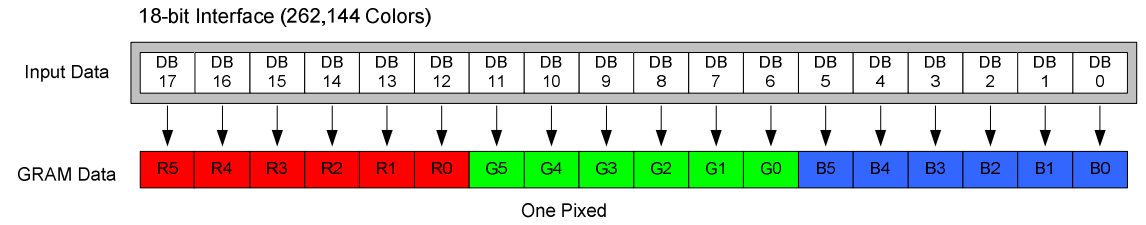
Parallel Interface

8080 18-BIT BUS INTERFACE

Setting the IM3/2/1/0 to the IOV_{CC}/GND/IOV_{CC}/GND level allows 80-system 18-bit parallel data transfer.



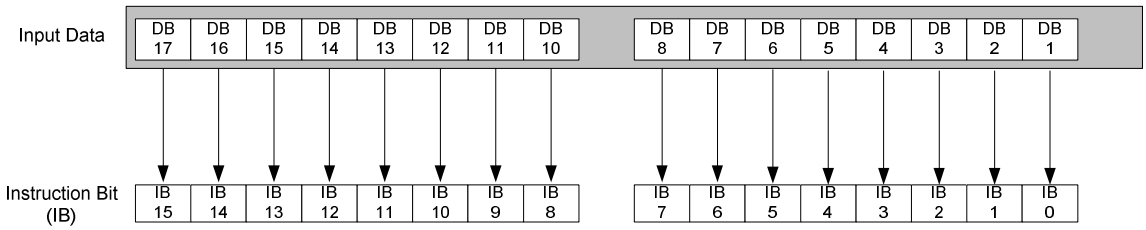
Instruction format for 18-bit



RAM Data Write format for 18-bit interface

8080 16-BIT BUS INTERFACE

Setting the IM3/2/1/0 to the V_{SS}/V_{SS}/IOV_{CC}/V_{SS} level allows 80-system 16-bit parallel data transfer.



Instruction format for 16-bit

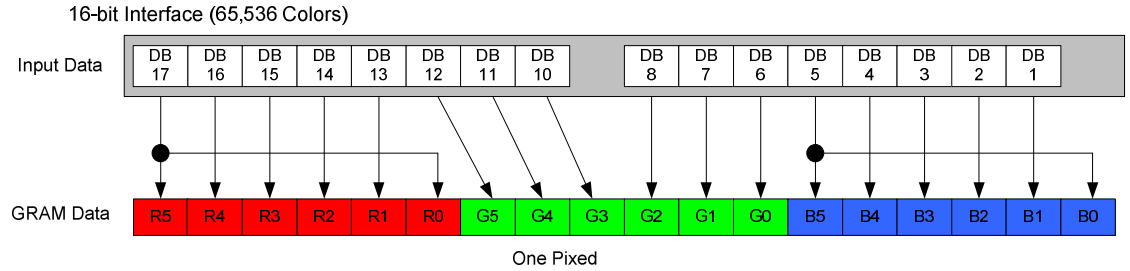
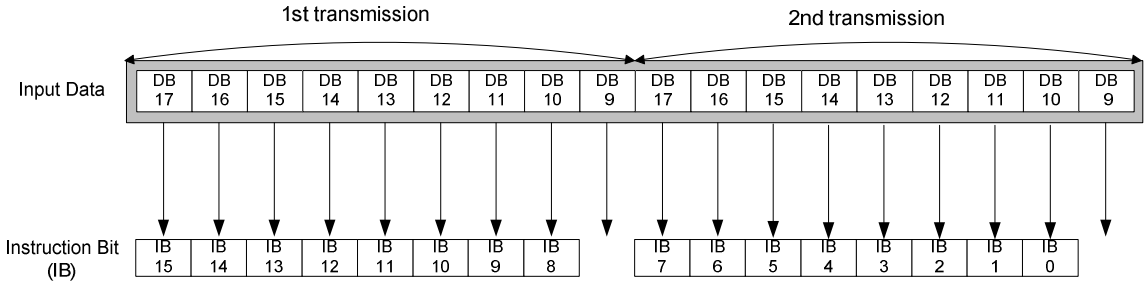


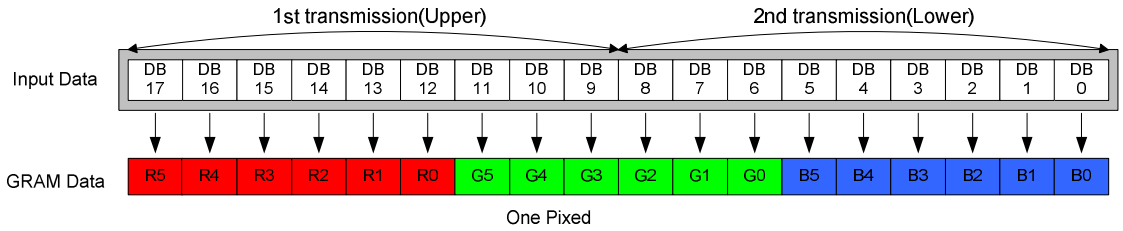
Figure 7. RAM Data Write format for 16-bit interface

8080 9-BIT BUS INTERFACE

Setting the IM3/2/1/0 to be $IOV_{CC}/V_{SS}/IOV_{CC}/IOV_{CC}$ level allows 80-system 9-bit parallel data transfer. The 16-bit instructions and RAM data are divided into nine upper/lower bits and the transfer starts from the upper nine bits. Fix unused pins DB8–DB0 to the IOV_{CC} or V_{SS} level. Note that the upper bytes must also be written when the index register is written.



Instruction format for 9-bit

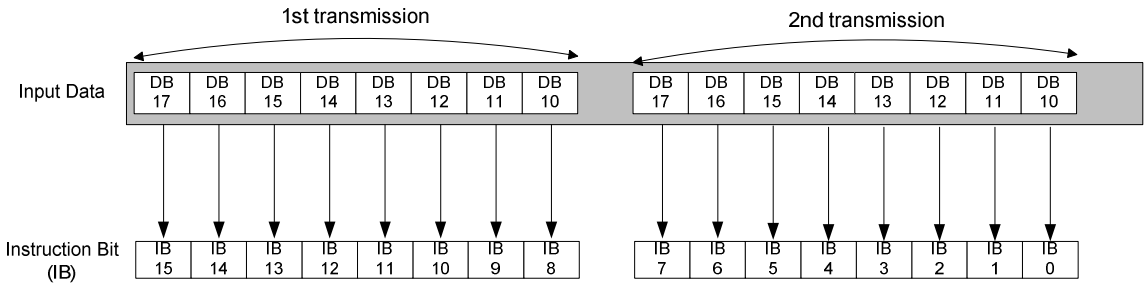


RAM Data Write format for 9-bit interface

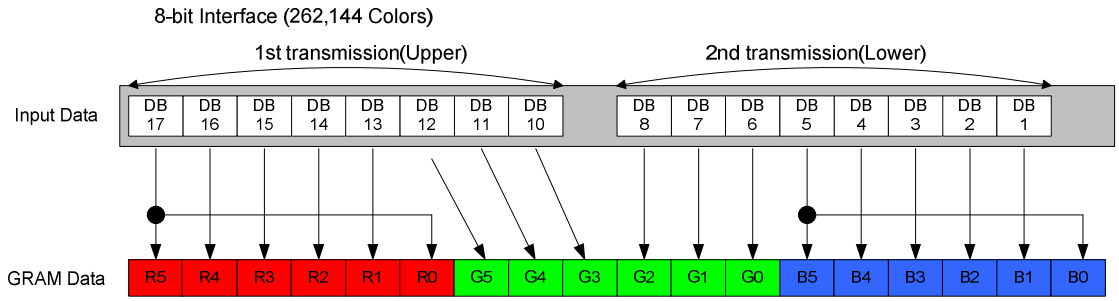
The UC8230s supports the transfer synchronization function, which resets the upper/lower counter to count upper/lower 9-bit data transfer in the 9-bit bus interface. Noise causing transfer mismatch between the nine upper and lower bits can be corrected by a reset triggered by consecutively writing a “00”H instruction four times. The next transfer starts from the upper nine bits. Executing synchronization function periodically can recover any runaway in the display system.

8080 8-BIT BUS INTERFACE

Setting the IM3/2/1/0 to the V_{SS}/V_{SS}/IOV_{CC}/IOV_{CC} level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB9–DB0 to the IOV_{CC} or V_{SS} level. Note that the upper bytes must also be written when the index register is written.



Instruction format for 8-bit



RAM Data Write format for 8-bit interface

The UC8230s supports the transfer synchronization function, which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a “00”H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system

Serial Interface

Setting the IM3 pin to the V_{SS} level allows serial peripheral interface (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB17-2 pins that are not used must be fixed at IOV_{CC} or V_{SS}.

The UC8230s initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input. The UC8230s is selected when the 6-bit chip address in the start byte matches the 6-bit device identification code that is assigned to the UC8230s. When selected, the UC8230s receives the subsequent data string. The LSB of the identification code can be determined by the ID pin. The five upper bits must be 01110.

Two different chip addresses must be assigned to a single UC8230s because the seventh bit of the start byte is used as a register select bit (RS):

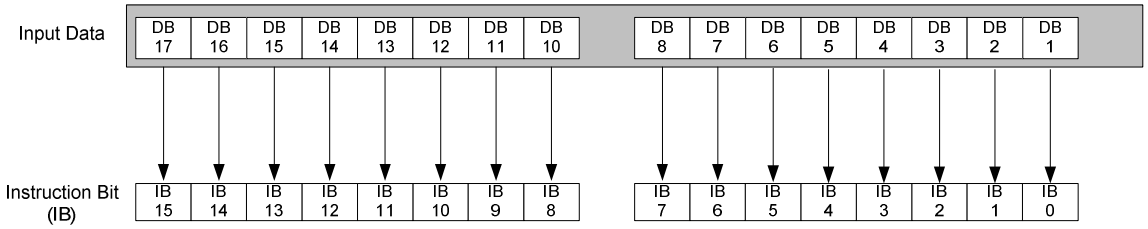
that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1. After receiving the start byte, the UC8230s receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first.

All UC8230s instructions are of 16 bits. Two bytes are received with the MSB first (DB17 to 0), then the instructions are internally executed. After the start byte has been received, the first byte is fetched as the upper eight bits of the instruction and the second byte is fetched as the lower eight bits of the instruction. Four bytes of RAM read data after the start byte are invalid. The UC8230s starts to read correct RAM data from the fifth byte.

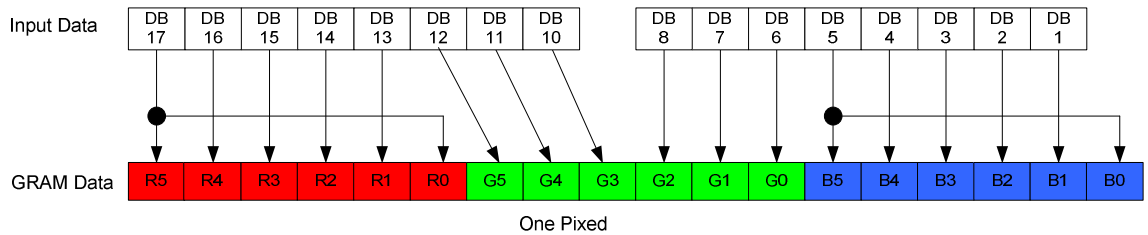
Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

RS	RW	Function
0	0	Set Index Register
0	1	Read status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

Table 40 RS and R/W Bit Function

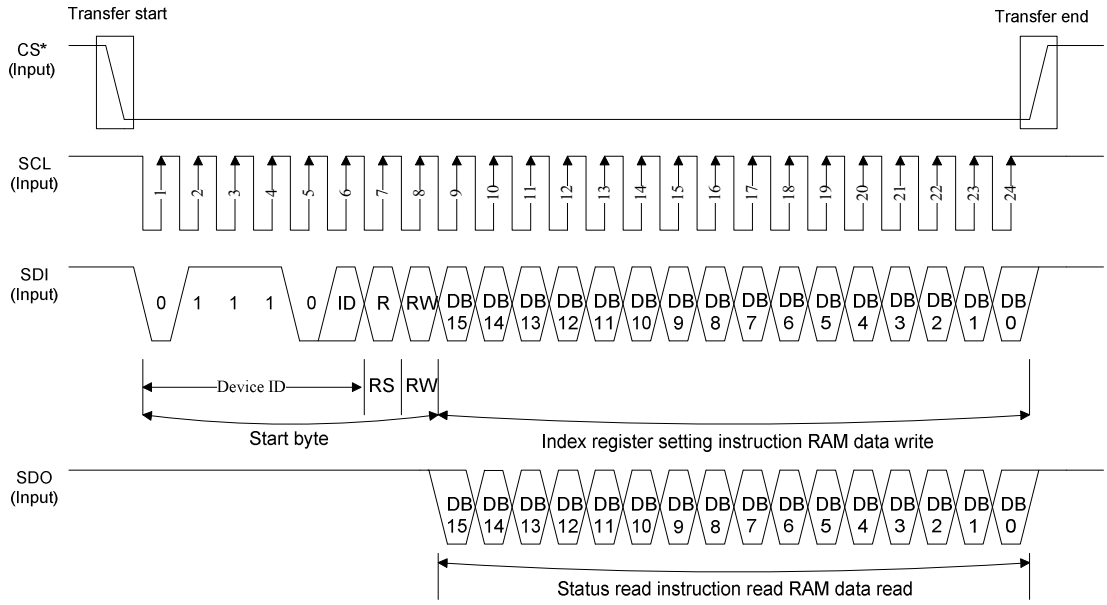


Instruction format for serial data Transfer

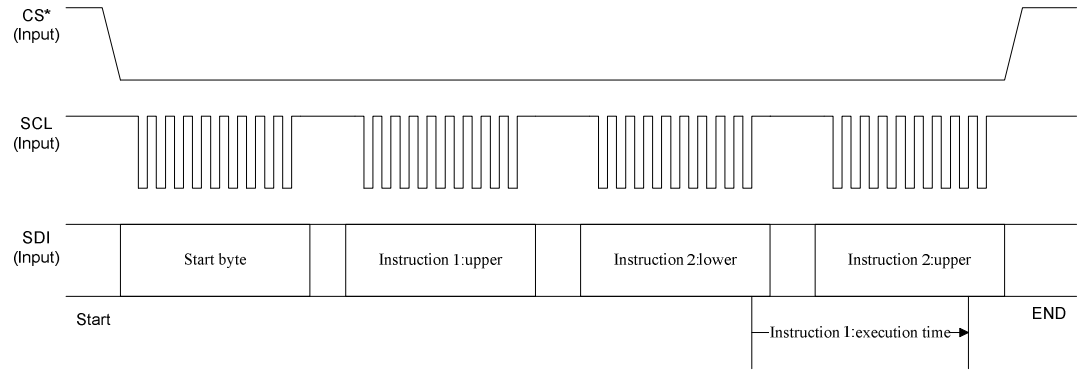


RAM Data Write format for Serial Data Transfer

(A) Timing Data Transfar through Clock Synchronized Serial Bus Interface



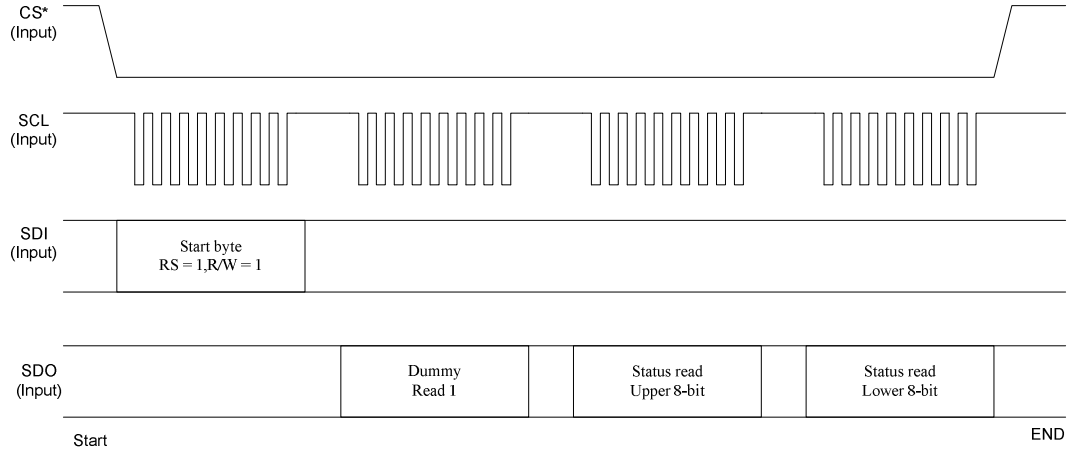
(B) Timing of Consecutive Data-Transfar through Clock Synchronized Serial Bus Interface



Note:

1. The first byte after the start byte is always the upper eight bits.
2. One byte of RAM data read after the start byte are invalid.

(D) Timing of Consecutive Data-Transfar through Clock Synchronized Serial Bus Interface



Note: Two bytes of the RAM data read after the start byte are invalid.

HOST INTERFACE REFERENCE CIRCUIT

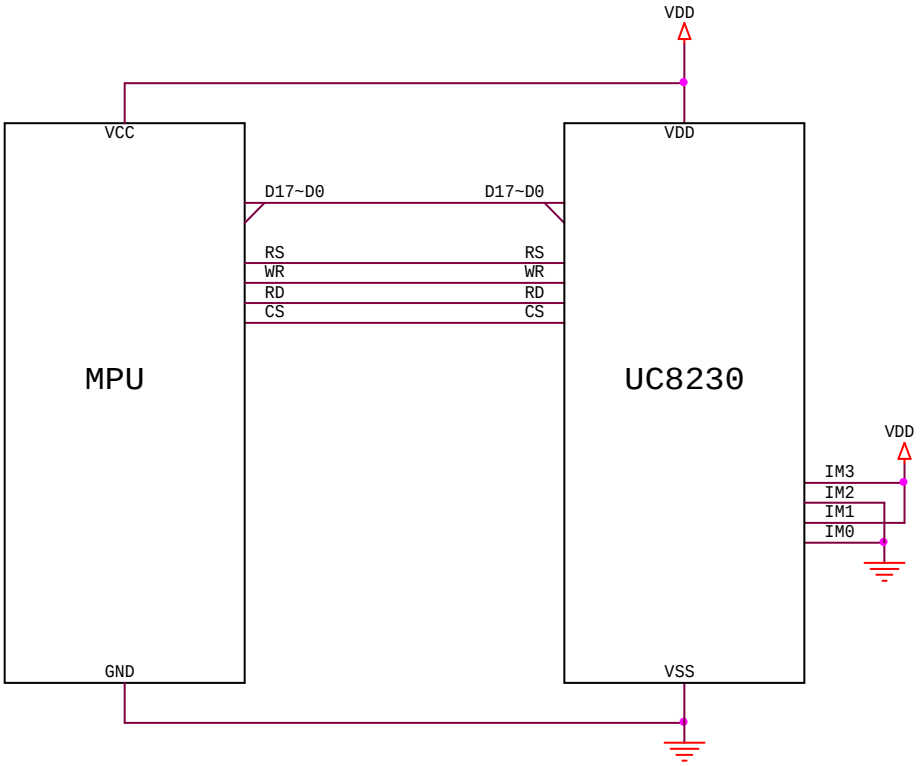


FIGURE 8: 8080/18-bit parallel mode example

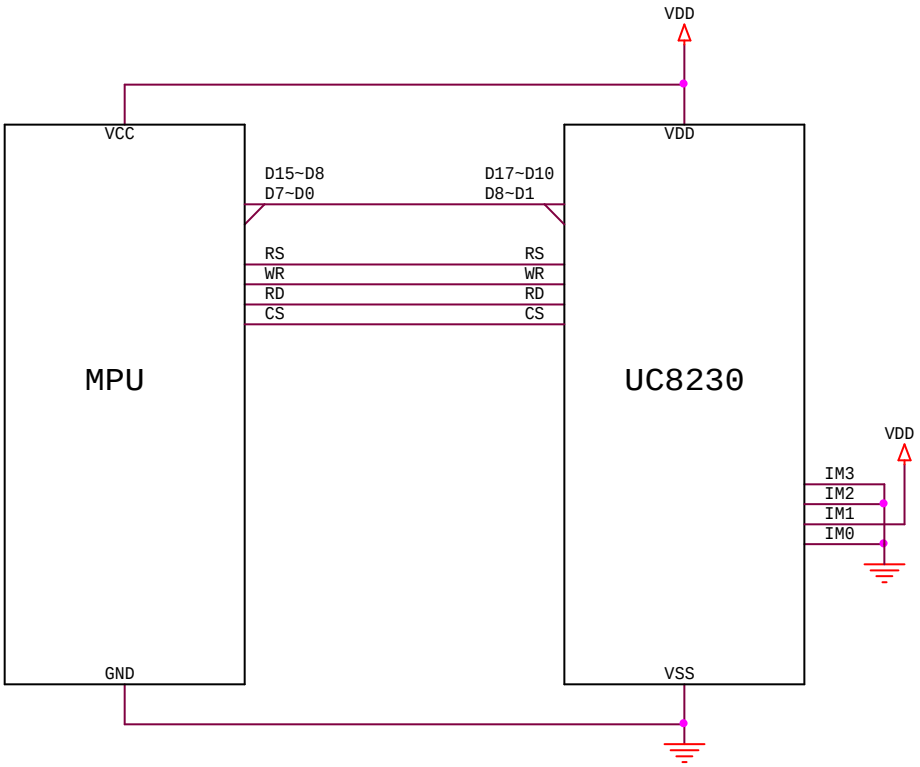


FIGURE 9: 8080/16-bit parallel mode example

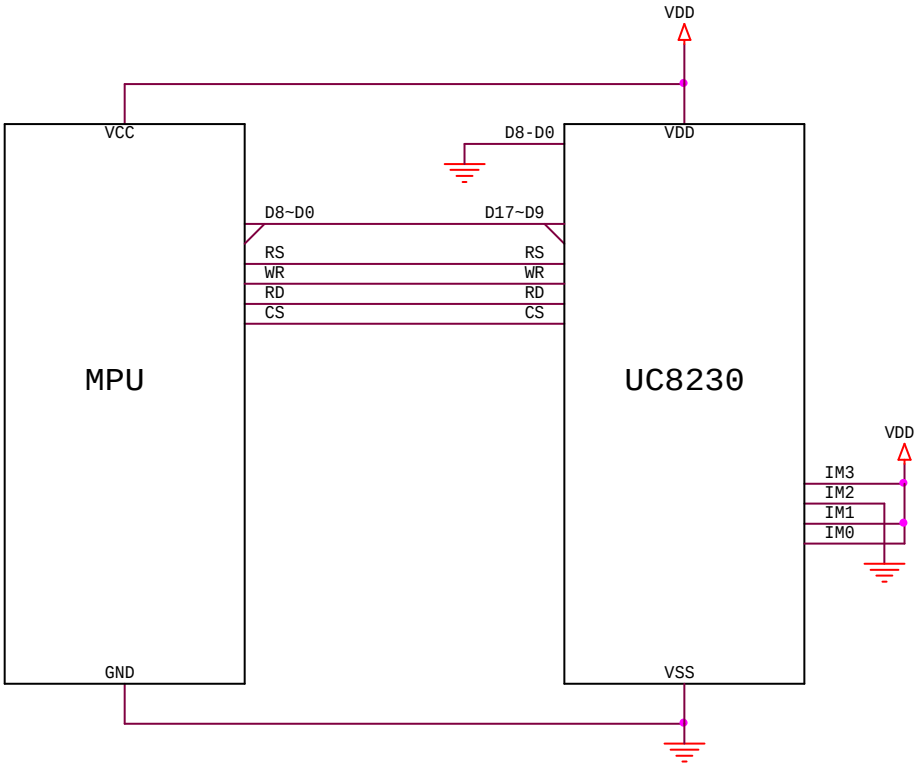


FIGURE 10: 8080/9-bit parallel mode example

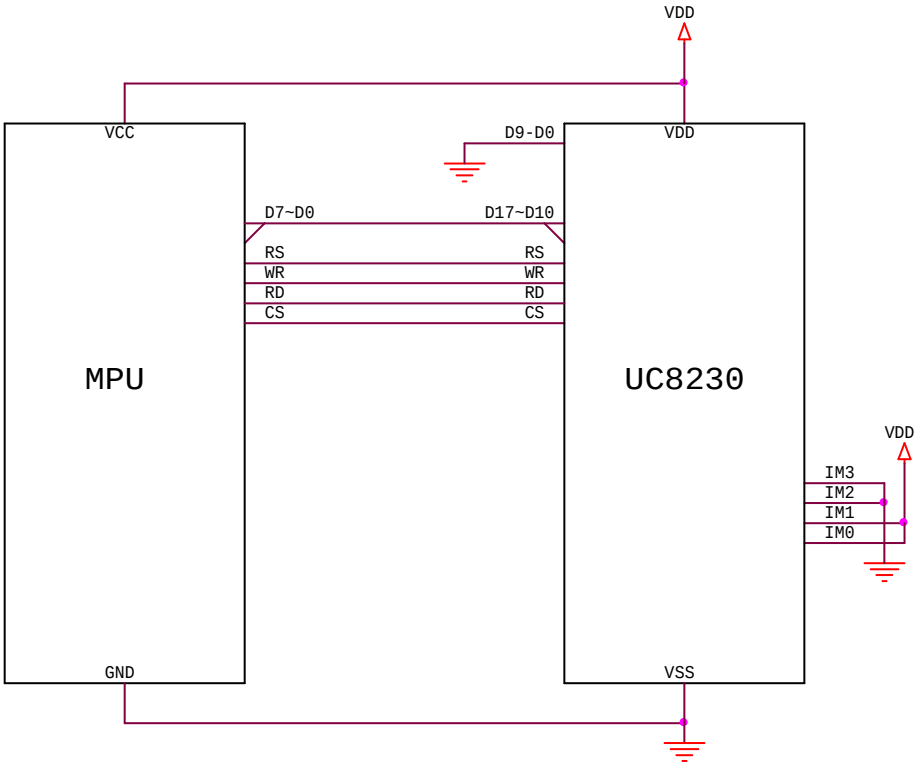


FIGURE 11: 8080/8-bit parallel mode example

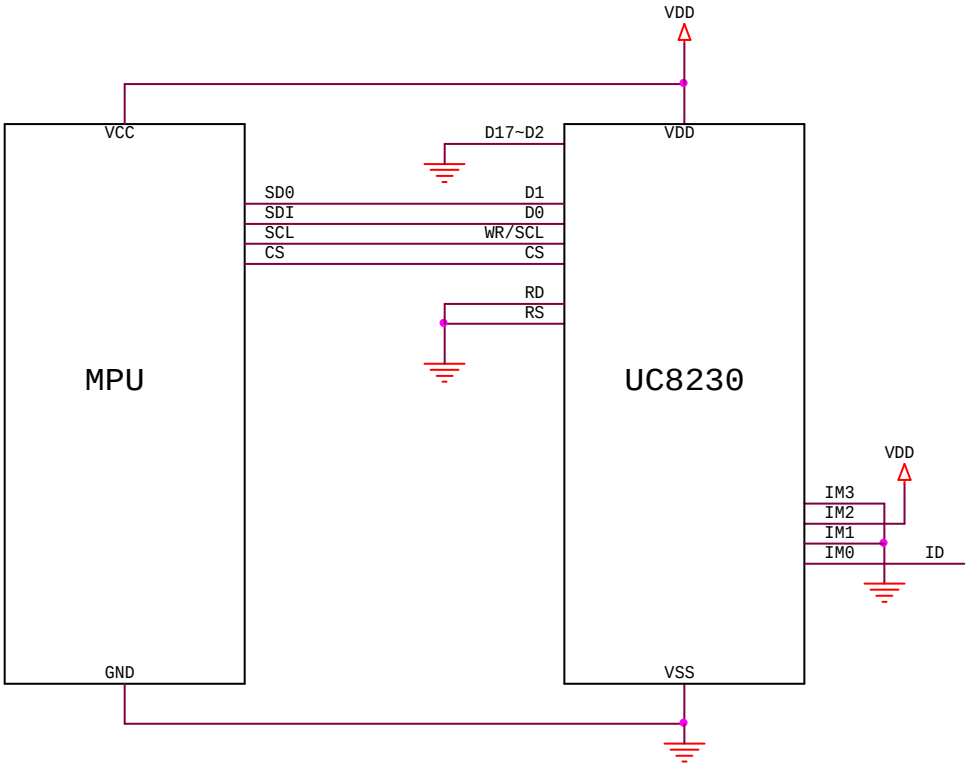


FIGURE 12: 4-Wires SPI serial mode example

EXTERNAL DISPLAY INTERFACE

The following interfaces are available as external display interface. It is determined by bit setting of RIM1-0. RAM accesses can be performed via the RGB interface.

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17 to 0
0	1	16-bit RGB interface	DB17 to 13, 11 to 1
1	0	6-bit RGB interface	DB17 to 12
1	1	Setting disabled	

1. RGB INTERFACE

The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK. Combining the function of the high-speed write mode and the window address enables transfer only the screen to be updated and reduce the power consumption.

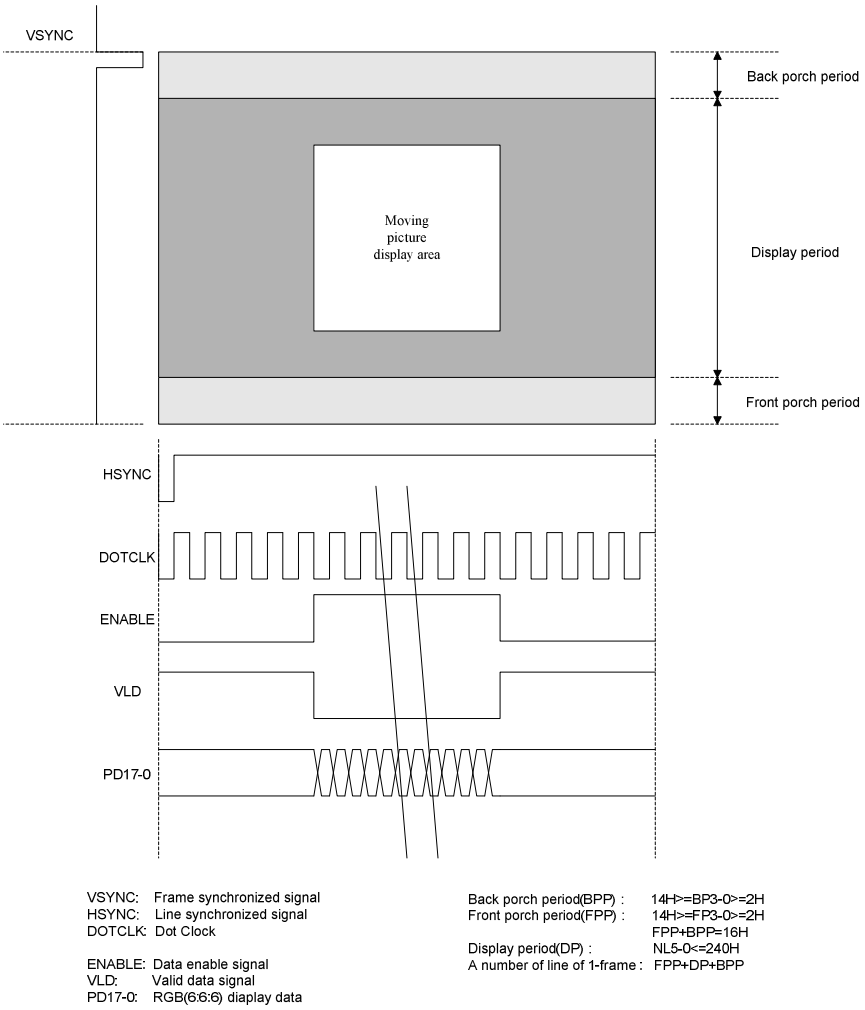
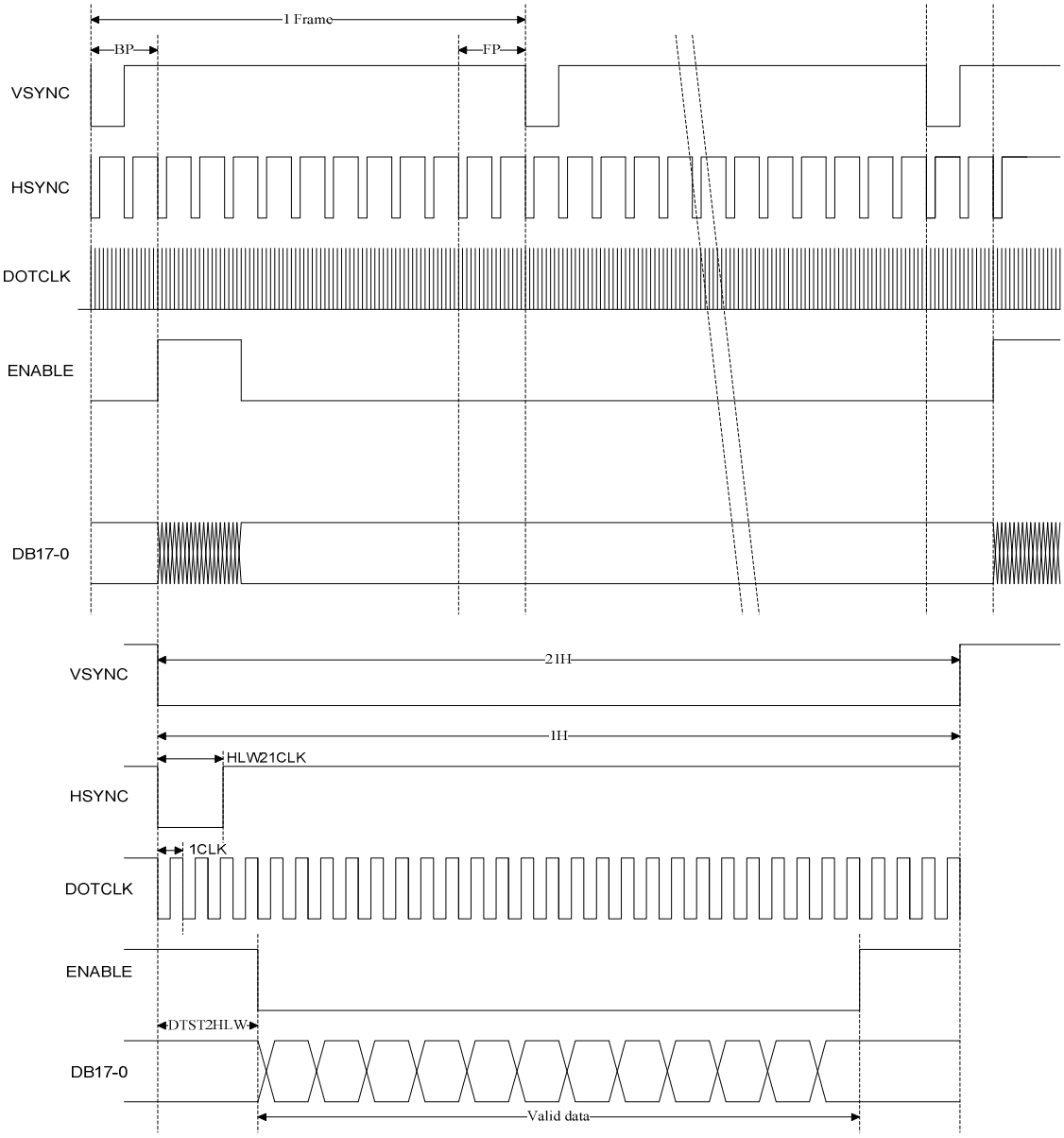


Figure 13 : RGB Interface

RGB INTERFACE TIMING

Time chart for RGB interface is shown below.



VLW: The period in which VSYNC is “Low” level
HLW: The period in which HSYNC is “Low” level
DTST: Set up time of data transfer

NOTE: Data for display should be written in the high-speed write mode (HWM=”1”) in VSYNC is in use.

DISPLAY OF MOVING PICTURE

The UC8230s incorporates RGB interface to display motion pictures and RAM to store data for display. For displaying motion pictures, the UC8230s has the following features.

- Motion picture area can only be transferred by the window address function.
- The high-speed write mode achieves both low power consumption and high-speed access.
- Motion picture area to be rewritten can only be transferred.
- Reducing the amount of data transferred enables reduce the power consumption to the whole system.
- Still picture area, such as an icon, can be updated while displaying motion pictures combining with the system interface.

RAM ACCESS VIA RGB INTERFACE AND SYSTEM INTERFACE

RAM can be accessed via the system interface when RGB interface is in use. When data is written to RAM during RGB interface mode, the ENABLE bit should be low to stop data writing via RGB interface, because RAM writing is always performed in synchronization with the DOTCLK input when ENABLE is high. After this RAM access via the system interface, a waiting time is needed for a write/read bus cycle before the next RAM access starts via RGB interface. When a RAM write conflict occurs, data writing is not guaranteed. Example of display motion picture via RGB-I/F and updating still picture via the system interface are shown below.

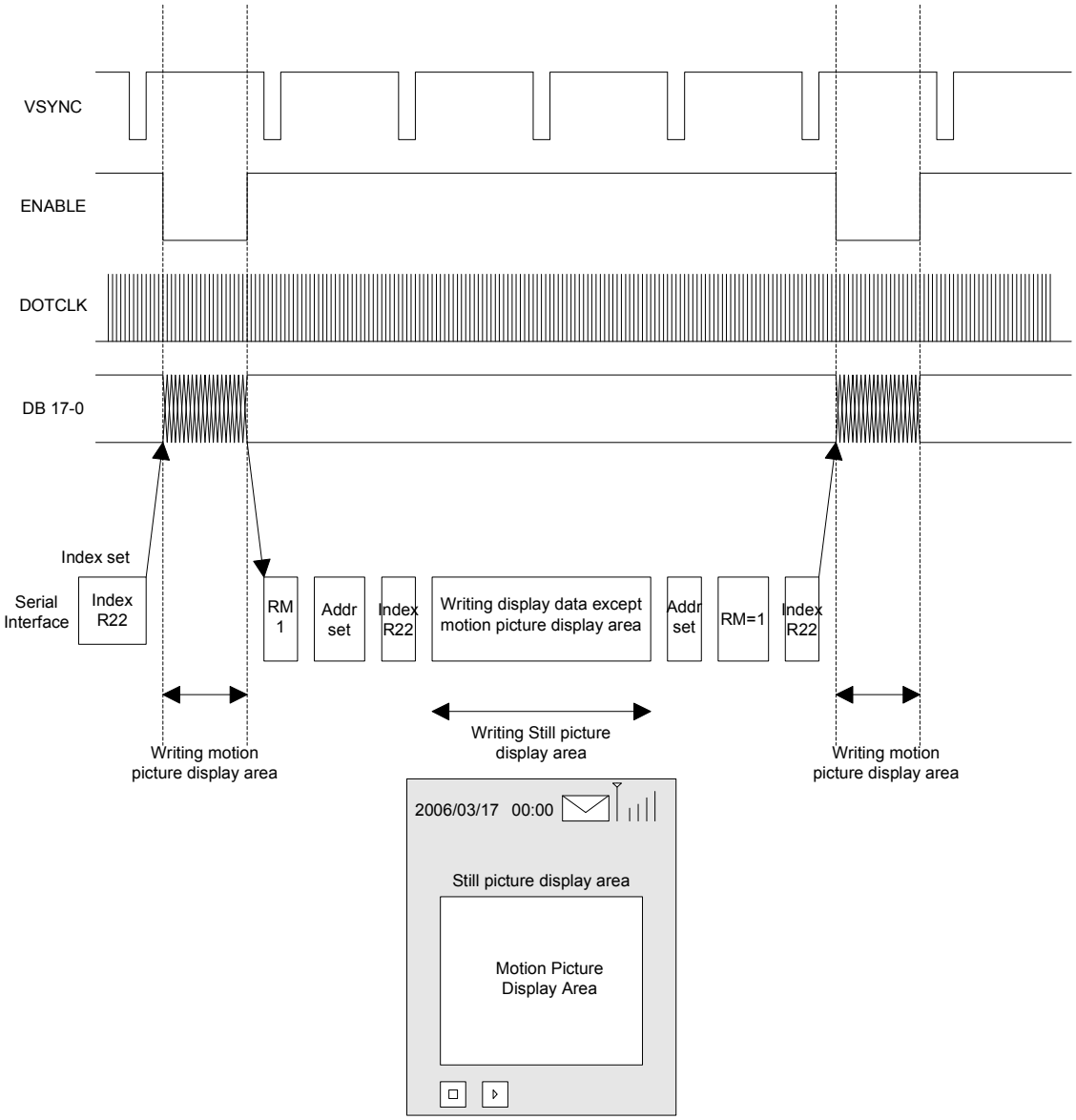


Figure 14 : Example of Updating Still Picture Area During Display Motion Picture

18-BIT RGB INTERFACE

18-bit RGB interface can be used by setting MIF1-0 pins to 01. Display operation is synchronized with VSYNC,HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM via 6-bit RGB data bus (DB17-0).

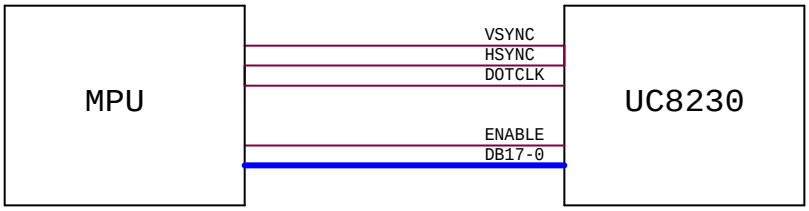
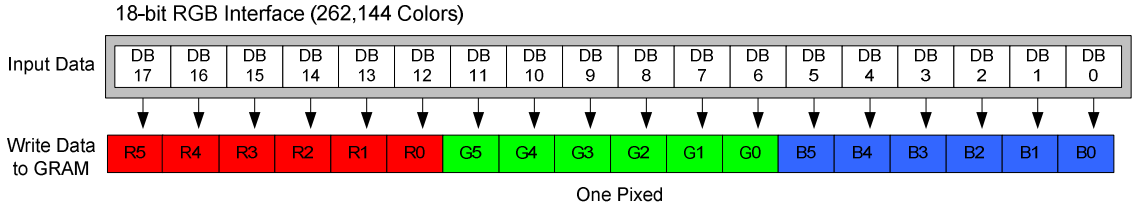


Figure 15. 18-bit interface



GRAM Write Data format for 18-bit RGB Interface

16-BIT RGB INTERFACE

16-bit RGB interface can be used by setting RIM1-0 pins to 01. Display operation is synchronized with VSYNC,HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM via 6-bit RGB data bus (DB17-13 and 11-1). Instruction should be set via the system interface.

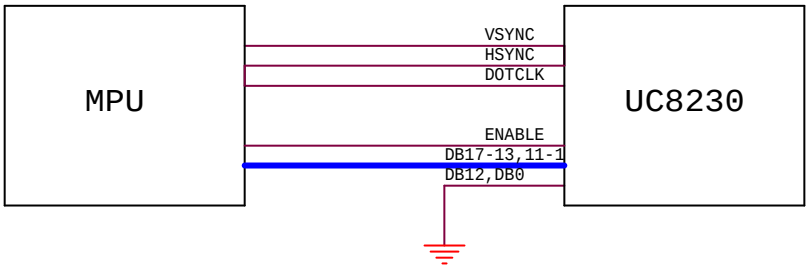
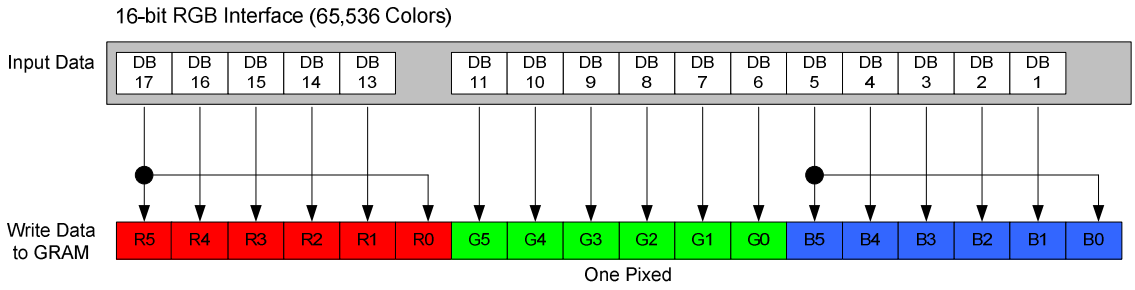


Figure 16 : 16-bit interface



GRAM Write Data format for 16-bit RGB Interface

6-BIT RGB INTERFACE

6-bit RGB interface can be used by setting RIM1-0 pins to “00”. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM via 6-bit RGB data bus (DB17 to 12), and the data enable signal (ENABLE). Unused pins must be fixed to the IOV_{CC} or GND level.

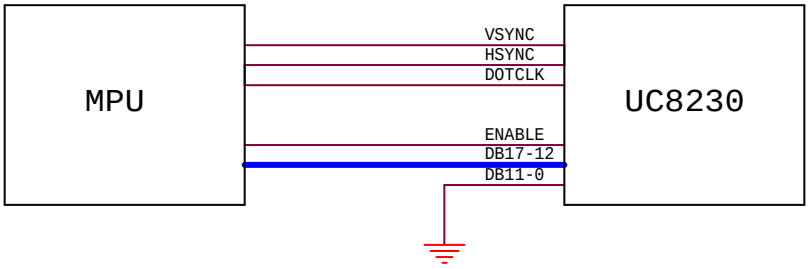
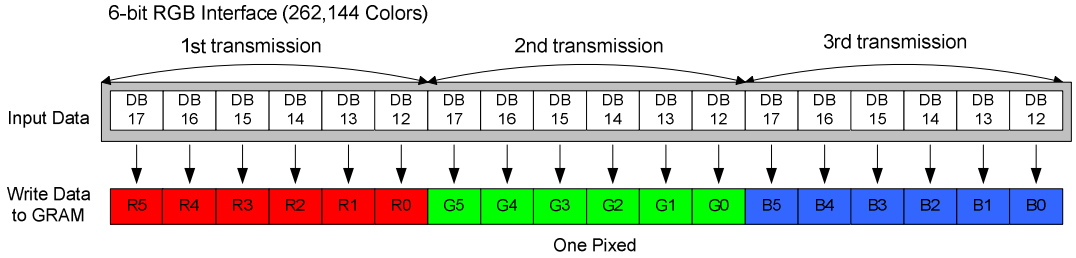


Figure 17. 6-bit interface



GRAM Write Data format for 6-bit RGB Interface

NOTE: Transfer synchronization function for an 6-bit bus interface. The UC8230s has the transfer counter to count 1st, 2nd and 3rd data transfer in the 6-bit bus interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected transfer restarts correctly. In this method, when data is consecutively transferred such as displaying motion pictures, the effect of transfer mismatch will be reduced and recover normal operation.

NOTE: The internal display is operated in units of three DOTCLK. When the DOTCLK is not input in units of pixels, click mismatch occurs and the frame, which is operated, and the next frame are not display correctly.

GRAM ADDRESS AND DISPLAY PANEL POSITION (SS ="0")

SG pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	……	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS =0	GS =1	DB17 ~DB0			DB17 ~DB0			DB17 ~DB0			DB17 ~DB0				DB17 ~DB0			DB17 ~DB0			DB17 ~DB0			DB17 ~DB0		
G1	G320	"0000"H			"0001"H			"0002"H			"0003"H			……	"00AC"H			"00AD"H			"00AE"H			"00AF"H		
G2	G319	"0100"H			"0101"H			"0102"H			"0103"H			……	"01AC"H			"01AD"H			"01AE"H			"01AF"H		
G3	G318	"0200"H			"0201"H			"0202"H			"0203"H			……	"02AC"H			"02AD"H			"02AE"H			"02AF"H		
G4	G317	"0300"H			"0301"H			"0302"H			"0303"H			……	"03AC"H			"03AD"H			"03AE"H			"03AF"H		
G5	G316	"0400"H			"0401"H			"0402"H			"0403"H			……	"04AC"H			"04AD"H			"04AE"H			"04AF"H		
G6	G315	"0500"H			"0501"H			"0502"H			"0503"H			……	"05AC"H			"05AD"H			"05AE"H			"05AF"H		
G7	G314	"0600"H			"0601"H			"0602"H			"0603"H			……	"06AC"H			"06AD"H			"06AE"H			"06AF"H		
G8	G313	"0700"H			"0701"H			"0702"H			"0703"H			……	"07AC"H			"07AD"H			"07AE"H			"07AF"H		
G9	G312	"0800"H			"0801"H			"0802"H			"0803"H			……	"08AC"H			"08AD"H			"08AE"H			"08AF"H		
G10	G311	"0900"H			"0901"H			"0902"H			"0903"H			……	"09AC"H			"09AD"H			"09AE"H			"09AF"H		
G11	G310	"0A00"H			"0A01"H			"0A02"H			"0A03"H			……	"0AAC"H			"0AAD"H			"0AAE"H			"0AAF"H		
G12	G309	"0B00"H			"0B01"H			"0B02"H			"0B03"H			……	"0BAC"H			"0BAD"H			"0BAE"H			"0BAF"H		
G13	G308	"0C00"H			"0C01"H			"0C02"H			"0C03"H			……	"0CAC"H			"0CAD"H			"0CAE"H			"0CAF"H		
G14	G307	"0D00"H			"0D01"H			"0D02"H			"0D03"H			……	"0DAC"H			"0DAD"H			"0DAE"H			"0DAF"H		
G15	G306	"0E00"H			"0E01"H			"0E02"H			"0E03"H			……	"0EAC"H			"0EAD"H			"0EAE"H			"0EAF"H		
G16	G305	"0F00"H			"0F01"H			"0F02"H			"0F03"H			……	"0FAC"H			"0FAD"H			"0FAE"H			"0FAF"H		
G17	G304	"1000"H			"1001"H			"1002"H			"1003"H			……	"10AC"H			"10AD"H			"10AE"H			"10AF"H		
G18	G303	"1100"H			"1101"H			"1102"H			"1103"H			……	"11AC"H			"11AD"H			"11AE"H			"11AF"H		
G19	G302	"1200"H			"1201"H			"1202"H			"1203"H			……	"12AC"H			"12AD"H			"12AE"H			"12AF"H		
G20	G301	"1300"H			"1301"H			"1302"H			"1303"H			……	"13AC"H			"13AD"H			"13AE"H			"13AF"H		
……	……	……			……			……			……			……	……			……			……			……		
G313	G8	"0800"H			"0801"H			"0802"H			"0803"H			……	"E8AC"H			"E8AD"H			"E8AE"H			"E8AF"H		
G314	G7	"0900"H			"0901"H			"0902"H			"0903"H			……	"E9AC"H			"E9AD"H			"E9AE"H			"E9AF"H		
G315	G6	"EA00"H			"EA01"H			"EA02"H			"EA03"H			……	"EAAC"H			"EAAD"H			"EAAE"H			"EAAF"H		
G316	G5	"EB00"H			"EB01"H			"EB02"H			"EB03"H			……	"EBAC"H			"EBAD"H			"EBAE"H			"EBAF"H		
G317	G4	"EC00"H			"EC01"H			"EC02"H			"EC03"H			……	"ECAC"H			"ECAD"H			"ECAE"H			"ECAF"H		
G318	G3	"ED00"H			"ED01"H			"ED02"H			"ED03"H			……	"EDAC"H			"EDAD"H			"EDAE"H			"EDAF"H		
G319	G2	"EE00"H			"EE01"H			"EE02"H			"EE03"H			……	"EEAC"H			"EEAD"H			"EEAE"H			"EEAF"H		
G320	G1	"EF00"H			"EF01"H			"EF02"H			"EF03"H			……	"EFAC"H			"EFAD"H			"EFAE"H			"EFAF"H		

Example for memory mapping: let MX = 0, MY = 0, SL = 0, LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color), according to the data shown in the above table (R: 11111b, G: 111111b, B: 11111b):

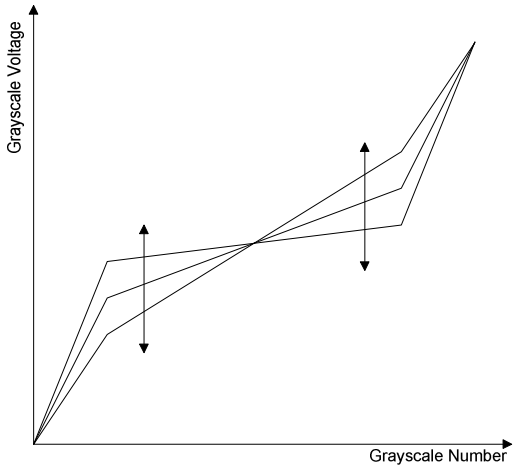
⇒ 1st byte of Write data: 11111111b

⇒ 2nd byte of Write data: 11111111b

Gamma-Correction Register

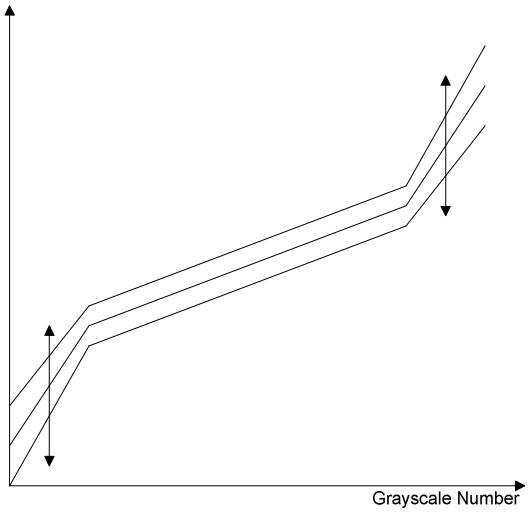
The Gamma-adjustment register is a group of registers to set an appropriate gray scale voltage for the gamma-characteristics of a liquid crystal panel. The register group is categorized into the ones adjusting gradient, amplitude, and fine-tuning in relation to grayscale number and grayscale voltage characteristics. Each register can make an independent setting for the positive/negative polarity. The reference value and RGB are common to both polarities.

1. Gradient adjustment registers
The gradient adjustment registers are used to adjust the gradient around the middle of the grayscale number and voltage characteristics without changing a dynamic range. To adjust a gradient, the values of the variable resistors (VRHP (N)/VRLP (N)) in the middle of the ladder resistor block for grayscale voltage generation are controlled. The registers incorporate separate registers for positive and negative polarities to be compatible with asymmetric drive.



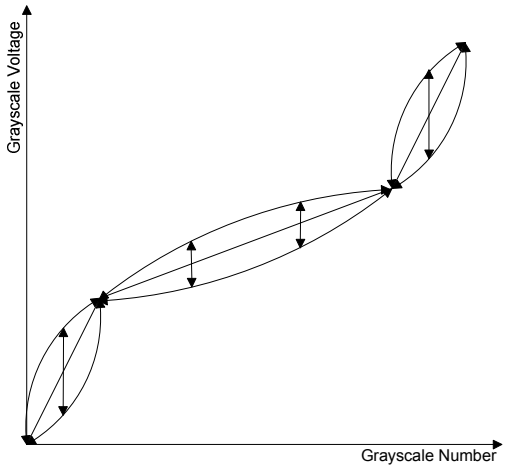
1. Gradient adjustment resister

2. Amplitude adjustment registers
The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage. To adjust the amplitude, the values of the variable resistors (VRP(N)1/0) in the bottom of the ladder resistor block for grayscale voltage generation are adjusted. Same with the gradient registers, the amplitude adjustment registers also incorporate separate registers for positive and negative polarities.



2. Amplitude adjustment

3. Fine adjustment registers
The fine adjustment register is to fine-adjust the grayscale voltage level. To fine-adjust the grayscale voltage level, each level of 8-level reference voltages generated from the ladder registers is controlled by 8- to -1 selector. Same with the other registers, the fine-adjustment registers also incorporate separate registers for positive and negative polarities.



3. Micro- adjustment

Gamma Correction registers

Register	Positive Polarity	Negative Polarity	set-up Contents
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRLP(N)
Reference adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VRP(N)0
Amplitude adjustment	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Micro adjustment	PKP0[2:0]	PKN0[2:0]	The Voltage of grayscale number 1 is selected by the 8 to 1 select
	PKP1[2:0]	PKN1[2:0]	The Voltage of grayscale number 8 is selected by the 8 to 1 select
	PKP2[2:0]	PKN2[2:0]	The Voltage of grayscale number 20 is selected by the 8 to 1 select
	PKP3[2:0]	PKN3[2:0]	The Voltage of grayscale number 43 is selected by the 8 to 1 select
	PKP4[2:0]	PKN4[2:0]	The Voltage of grayscale number 55 is selected by the 8 to 1 select
	PKP5[2:0]	PKN5[2:0]	The Voltage of grayscale number 62 is selected by the 8 to 1 select

Variable resistor

There are three kinds of variable resistors for the gradient adjustment (VRHP(N)/VRLP(N)), the amplitude adjustment (1) (VRP(N)0), and the amplitude adjustment (2) (VRP(N)1). The resistance is determined by the gradient adjustment and amplitude adjustment registers as is shown below.

Gradient Adjustment(1)	
Register Value PRP(N)0 [2:0]	Resistance value VRHP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R
Gradient Adjustment(2)	
Register Value PRP(N)1 [2:0]	Resistance value VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Reference Adjustment	
Reference value VRP(N)0 [4:0]	Resistance value VRP(N)0
00000	0R
00001	2R
00010	4R
…	…
…	…
11101	58R
11110	60R
11111	62R
Amplitude Adjustment	
Reference value VRP(N)1 [4:0]	Resistance value VRP(N)1
00000	0R
00001	1R
00010	2R
…	…
…	…
11101	29R
11110	30R
11111	31R

8-to-1 Selector

The 8-to-1 selectors select a voltage level generated by the ladder resistors according to the fine adjustment registers, and output six kinds of reference voltage, VIN1 to VIN 6. The relationship between the fine adjustment register and the selected voltage is as follows.

Relationship between Micro-adjustment Register and selected Voltage

Register value PKP(N) [2:0]	Selected voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

Shade #	Shade Voltage (V)	Formula
V0	3.000	VIN0
V1	2.471	VIN1
V2	2.447	VIN2+(VIN1-VIN2)*(19/24)
V3	2.428	VIN2+(VIN1-VIN2)*(15/24)
V4	2.414	VIN2+(VIN1-VIN2)*(12/24)
V5	2.400	VIN2+(VIN1-VIN2)*(9/24)
V6	2.386	VIN2+(VIN1-VIN2)*(6/24)
V7	2.372	VIN2+(VIN1-VIN2)*(3/24)
V8	2.358	VIN2
V9	2.342	VIN3+(VIN2-VIN3)*(22/24)
V10	2.326	VIN3+(VIN2-VIN3)*(20/24)
V11	2.310	VIN3+(VIN2-VIN3)*(18/24)
V12	2.294	VIN3+(VIN2-VIN3)*(16/24)
V13	2.278	VIN3+(VIN2-VIN3)*(14/24)
V14	2.262	VIN3+(VIN2-VIN3)*(12/24)
V15	2.246	VIN3+(VIN2-VIN3)*(10/24)
V16	2.230	VIN3+(VIN2-VIN3)*(8/24)
V17	2.214	VIN3+(VIN2-VIN3)*(6/24)
V18	2.198	VIN3+(VIN2-VIN3)*(4/24)
V19	2.182	VIN3+(VIN2-VIN3)*(2/24)
V20	2.166	VIN3
V21	2.155	VIN4+(VIN3-VIN4)*(22/23)
V22	2.143	VIN4+(VIN3-VIN4)*(21/23)
V23	2.132	VIN4+(VIN3-VIN4)*(20/23)
V24	2.121	VIN4+(VIN3-VIN4)*(19/23)
V25	2.110	VIN4+(VIN3-VIN4)*(18/23)
V26	2.099	VIN4+(VIN3-VIN4)*(17/23)
V27	2.088	VIN4+(VIN3-VIN4)*(16/23)
V28	2.076	VIN4+(VIN3-VIN4)*(15/23)
V29	2.065	VIN4+(VIN3-VIN4)*(14/23)
V30	2.054	VIN4+(VIN3-VIN4)*(13/23)
V31	2.043	VIN4+(VIN3-VIN4)*(12/23)

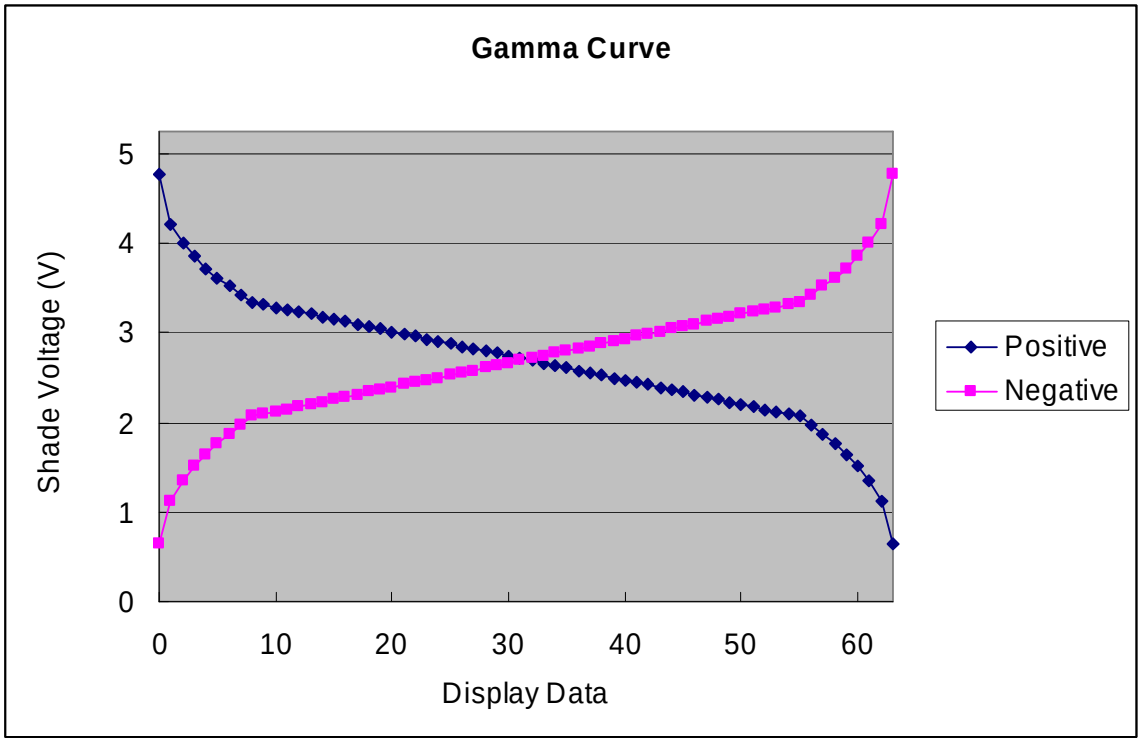
Shade #	Shade Voltage (V)	Formula
V32	2.032	VIN4+(VIN3-VIN4)*(11/23)
V33	2.021	VIN4+(VIN3-VIN4)*(10/23)
V34	2.010	VIN4+(VIN3-VIN4)*(9/23)
V35	1.998	VIN4+(VIN3-VIN4)*(8/23)
V36	1.987	VIN4+(VIN3-VIN4)*(7/23)
V37	1.976	VIN4+(VIN3-VIN4)*(6/23)
V38	1.965	VIN4+(VIN3-VIN4)*(5/23)
V39	1.954	VIN4+(VIN3-VIN4)*(4/23)
V40	1.943	VIN4+(VIN3-VIN4)*(3/23)
V41	1.931	VIN4+(VIN3-VIN4)*(2/23)
V42	1.920	VIN4+(VIN3-VIN4)*(1/23)
V43	1.909	VIN4
V44	1.893	VIN5+(VIN4-VIN5)*(22/24)
V45	1.877	VIN5+(VIN4-VIN5)*(20/24)
V46	1.861	VIN5+(VIN4-VIN5)*(18/24)
V47	1.845	VIN5+(VIN4-VIN5)*(16/24)
V48	1.829	VIN5+(VIN4-VIN5)*(14/24)
V49	1.813	VIN5+(VIN4-VIN5)*(12/24)
V50	1.797	VIN5+(VIN4-VIN5)*(10/24)
V51	1.781	VIN5+(VIN4-VIN5)*(8/24)
V52	1.765	VIN5+(VIN4-VIN5)*(6/24)
V53	1.749	VIN5+(VIN4-VIN5)*(4/24)
V54	1.733	VIN5+(VIN4-VIN5)*(2/24)
V55	1.717	VIN5
V56	1.646	VIN6+(VIN5-VIN6)*(21/24)
V57	1.576	VIN6+(VIN5-VIN6)*(18/24)
V58	1.506	VIN6+(VIN5-VIN6)*(15/24)
V59	1.436	VIN6+(VIN5-VIN6)*(12/24)
V60	1.366	VIN6+(VIN5-VIN6)*(9/24)
V61	1.272	VIN6+(VIN5-VIN6)*(5/24)
V62	1.155	VIN6
V63	0.626	VIN7

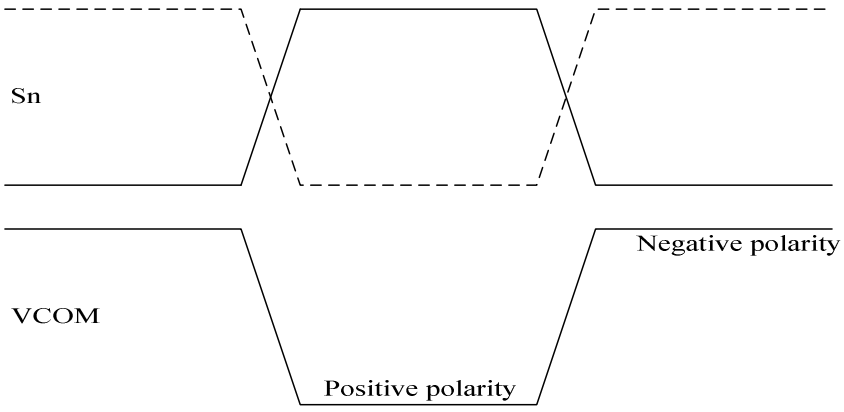
Gamma Voltage Formula

Display data	Grayscale			
	Negative polarity		Positive polarity	
	Formula	Effective Voltage	Formula	Effective Voltage
0	V0	4.783	V63	0.652
1	V1	4.212	V62	1.114
2	V2	3.995	V61	1.352
3	V3	3.850	V60	1.510
4	V4	3.723	V59	1.649
5	V5	3.614	V58	1.768
6	V6	3.524	V57	1.867
7	V7	3.433	V56	1.966
8	V8	3.342	V55	2.065
9	V9	3.315	V54	2.092
10	V10	3.288	V53	2.120
11	V11	3.261	V52	2.147
12	V12	3.234	V51	2.174
13	V13	3.207	V50	2.201
14	V14	3.179	V49	2.228
15	V15	3.152	V48	2.255
16	V16	3.125	V47	2.283
17	V17	3.098	V46	2.310
18	V18	3.071	V45	2.337
19	V19	3.043	V44	2.364
20	V20	3.016	V43	2.391
21	V21	2.989	V42	2.418
22	V22	2.962	V41	2.446
23	V23	2.935	V40	2.473
24	V24	2.908	V39	2.500
25	V25	2.880	V38	2.527
26	V26	2.853	V37	2.554
27	V27	2.826	V36	2.582
28	V28	2.799	V35	2.609
29	V29	2.772	V34	2.636
30	V30	2.745	V33	2.663
31	V31	2.717	V32	2.690
32	V32	2.690	V31	2.717

Display data	Grayscale			
	Negative polarity		Positive polarity	
	Formula	Effective Voltage	Formula	Effective Voltage
33	V33	2.663	V30	2.745
34	V34	2.636	V29	2.772
35	V35	2.609	V28	2.799
36	V36	2.582	V27	2.826
37	V37	2.554	V26	2.853
38	V38	2.527	V25	2.880
39	V39	2.500	V24	2.908
40	V40	2.473	V23	2.935
41	V41	2.446	V22	2.962
42	V42	2.418	V21	2.989
43	V43	2.391	V20	3.016
44	V44	2.364	V19	3.043
45	V45	2.337	V18	3.071
46	V46	2.310	V17	3.098
47	V47	2.283	V16	3.125
48	V48	2.255	V15	3.152
49	V49	2.228	V14	3.179
50	V50	2.201	V13	3.207
51	V51	2.174	V12	3.234
52	V52	2.147	V11	3.261
53	V53	2.120	V10	3.288
54	V54	2.092	V9	3.315
55	V55	2.065	V8	3.342
56	V56	1.966	V7	3.433
57	V57	1.867	V6	3.524
58	V58	1.768	V5	3.614
59	V59	1.649	V4	3.723
60	V60	1.510	V3	3.850
61	V61	1.352	V2	3.995
62	V62	1.114	V1	4.212
63	V63	0.652	V0	4.783

Relationship between RAM data and out voltage

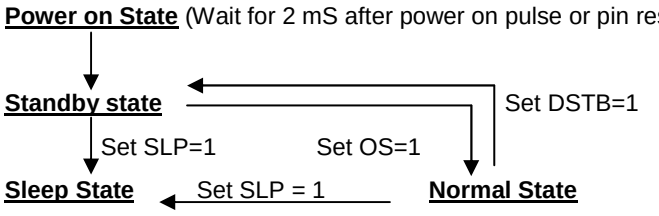




Relationship between source output and VCOM

POWER MANAGEMENT

IC Control State



MAN – 0 : automatic power-display setup 1 : manual power-display setup
This command is for programming register DE

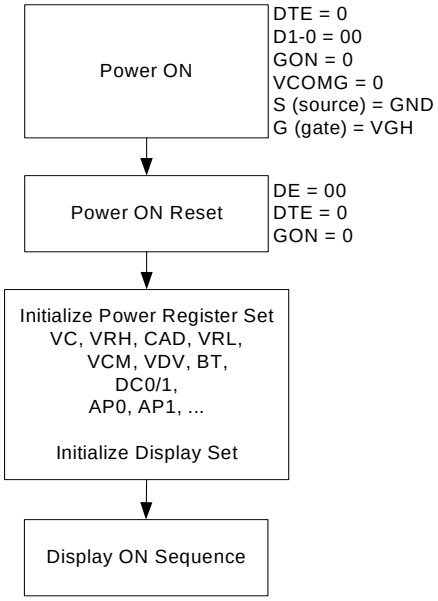
DE –

	DSTB	SLP	OS
State	Standby state	Sleep State (for temporary display turns off)	Normal State
Function	Standby	Sleep	Display On
Bus Interface	Active	Active	Active
Register	Normal	Normal	Normal
Display operation	Off	Off	Active
Clock	Off	Active	Active
Power setup	Off / drain	On	On

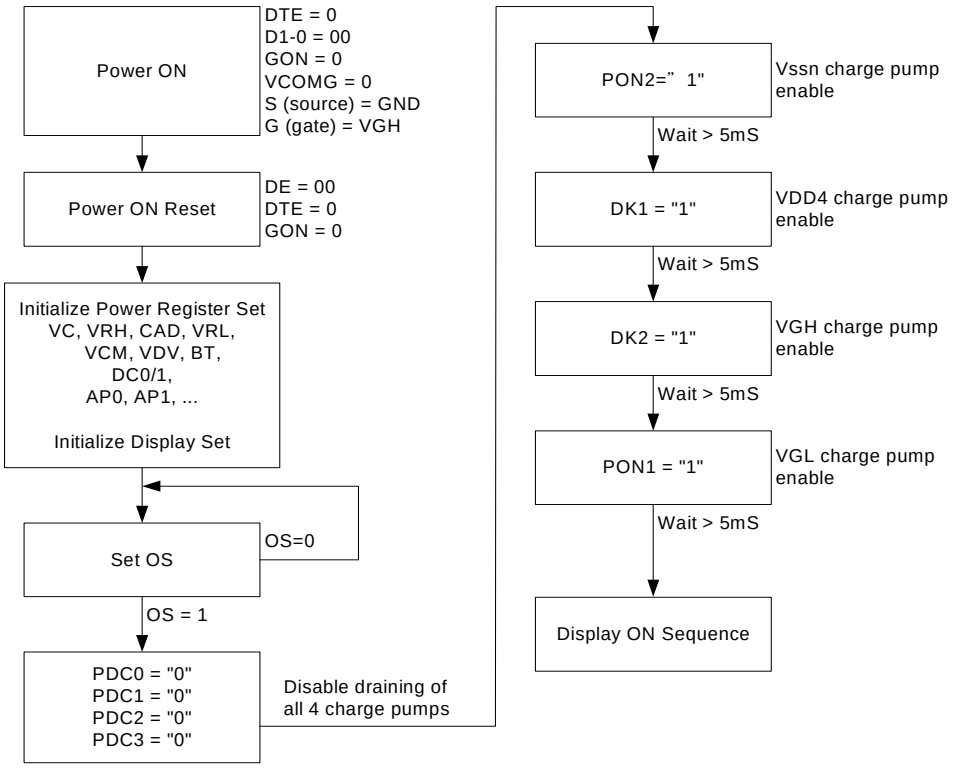
For manual power-up sequence, please refer to Command `Display Control 1/2.`

Power-On Sequence

Power-On Sequence (Auto mode setting)



Power-On Sequence (manual setting)

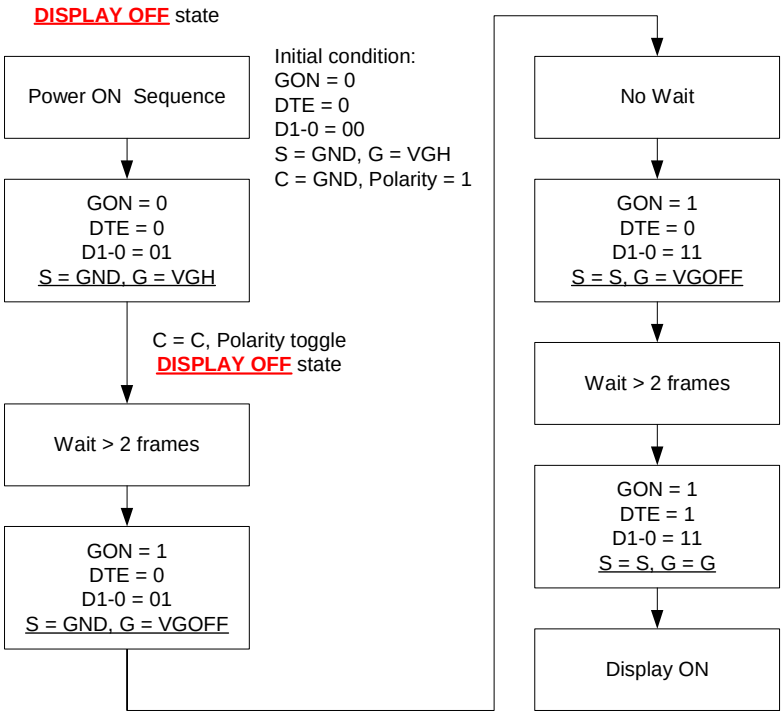


V_{D4}/VGH power set up sequence –

AUTO mode – V_{D4} is up first, then VGH
MANUAL mode – V_{D4} & VGH are set up at the same time

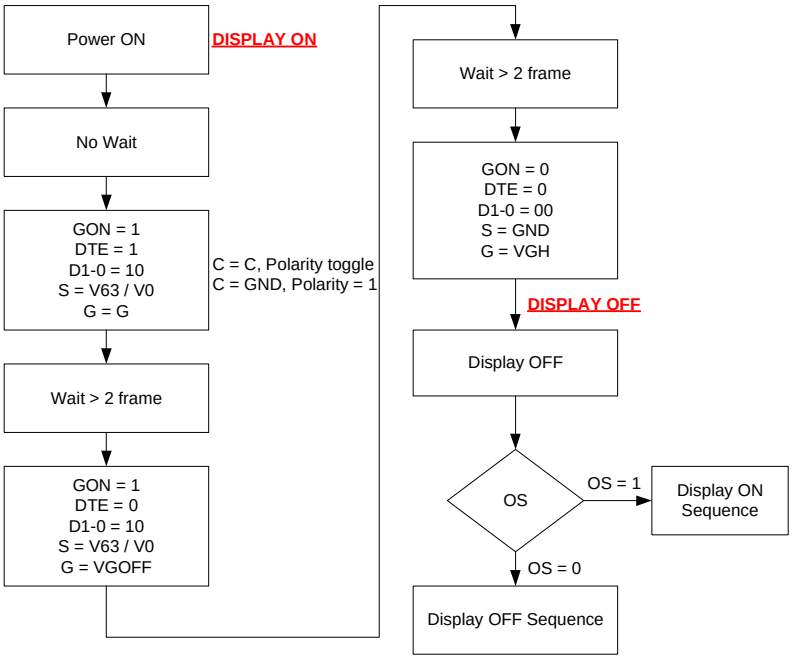
Display ON Flow

Display On Flow (S: Source, G: Gate, C: Com)



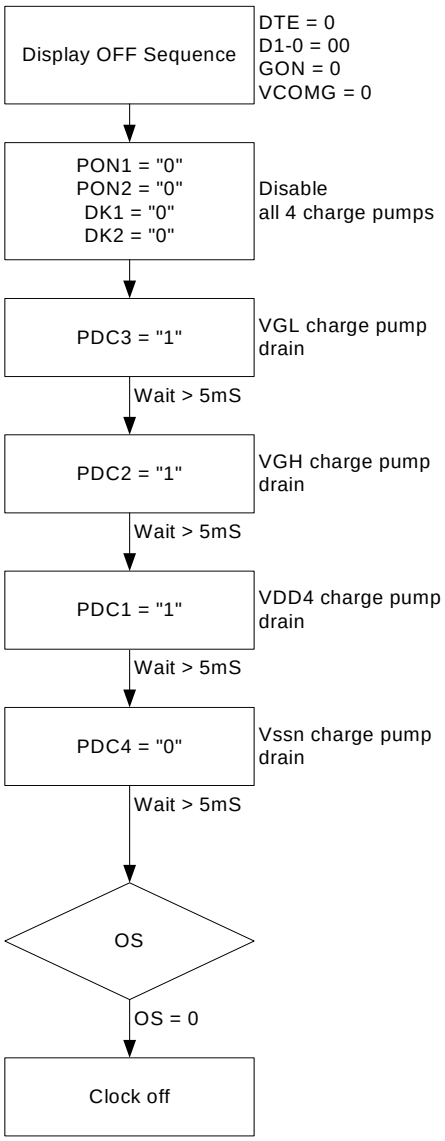
Power-OFF Flow

Power-OFF Flow
(S: Source, G: Gate, C: Com)

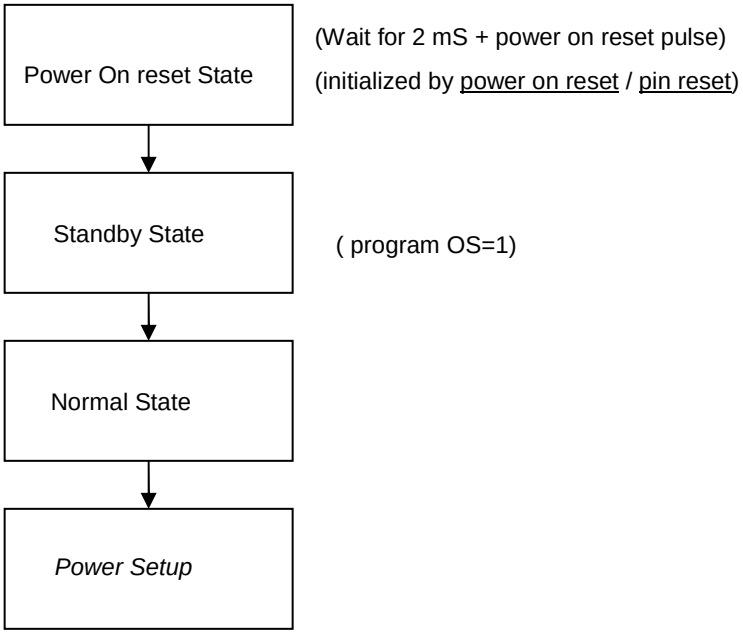


Power-OFF Sequence

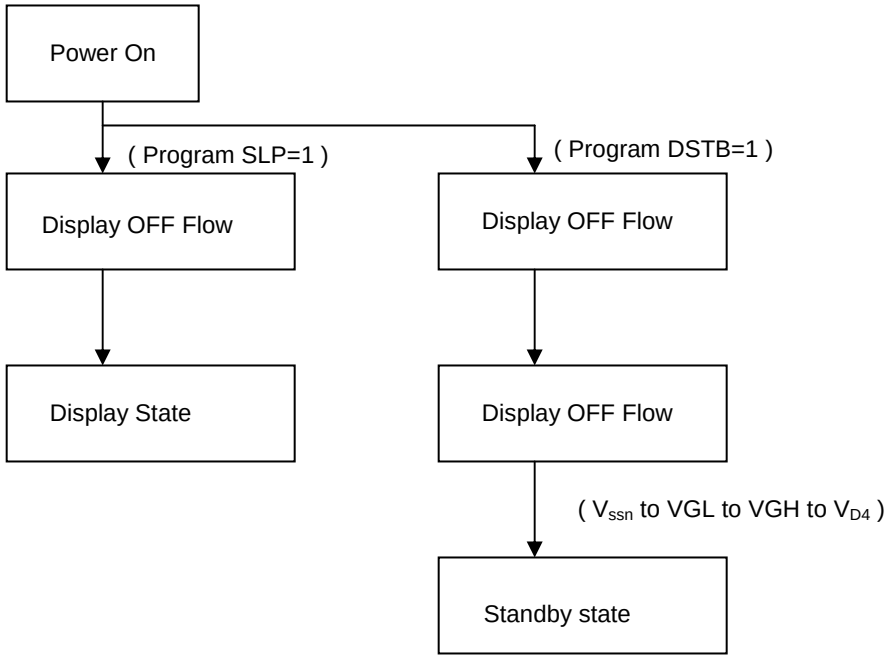
Power-OFF Sequence



Auto Display On/Off Flow



Display On-OFF Flow



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	LCD Generator Supply voltage	-0.3	+4.0	V
IOV_{CC}	Interface pin power supply	-0.3	+4.0	V
V_{D4}	Analog Circuit Supply voltage	-0.3	+6.0	V
$\mid V_{CC}H - V_{CC}L \mid$	LCD Gate Driving voltage	-0.3	+27	V
V_{IN}	Digital input signal	-0.4	V_{D1} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

NOTE:

1. V_{D1} is based on V_{SS} = 0V.
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	LCD Generator Supply voltage		2.5		3.3	V
IOV_{CC}	Interface pin power supply		1.65		3.3	V
V_{D4}	V_{D4} pumpout		4		5.5	V
$V_{CC}H$	$V_{CC}H$ pumpout		10		15	V
V_SN	V_SN pumpout		-2.75			V
$V_{CC}L$	$V_{CC}L$ pumpout		-12		-8	V
V_{IL_H}	Input logic LOW	IOVCC=2.5V~3.3V			0.15xIOVcc	V
V_{IH_H}	Input logic HIGH	IOVCC=2.5V~3.3V	0.85xIOVcc			V
V_{IL_L}	Input logic LOW	IOVCC=1.65V~2.5V			0xIOVcc	V
V_{IH_L}	Input logic HIGH	IOVCC=1.65V~2.5V	1xIOVcc			V
V_{OL}	Output logic LOW				0.2 IOVcc	V
V_{OH}	Output logic HIGH		0.8 IOVcc			V
I_{IL}	Input leakage current				1.5	µA
C_{IN}	Input capacitance			5	10	PF

Note : Voltages exceeding the Max. value may still keep the IC operating properly, yet might shorten its lifetime.

POWER CONSUMPTION

IOVcc=3.3V, Vcc=3.3V, Line Inverted=1

Display Pattern	Conditions	Typ. (µA)	Max. (µA)
Black	Bus = idle	3500	5250
1-pixel checker	Bus = idle	3100	4650
Sleep mode	Into Sleep mode	<50	100

AC CHARACTERISTICS

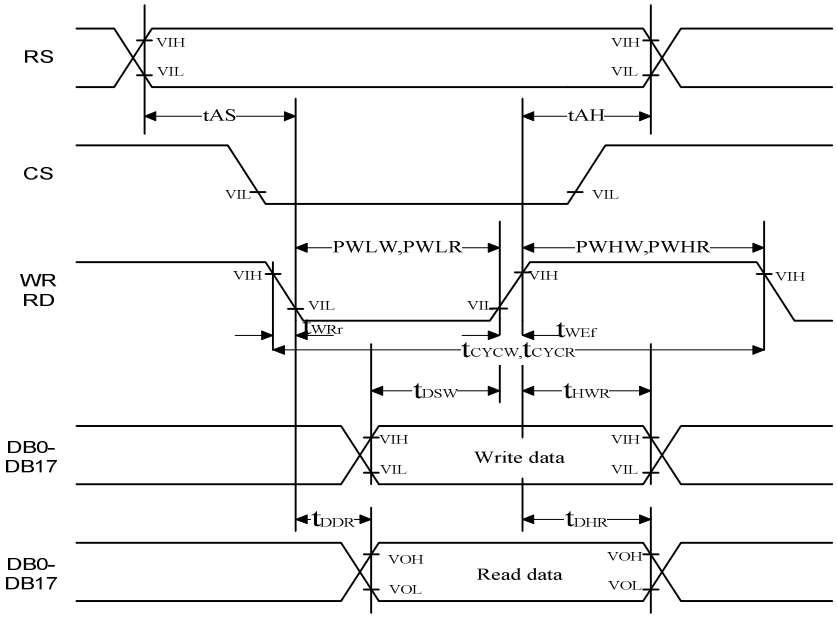


FIGURE 18: Parallel Bus Timing Characteristics (for 8080 MCU)

(1.65V ≤ IOVCC < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Min.	Max.	Units
t_{AS}	RS to CS,WR,RD	Address Setup Time	10	–	nS
t_{AH}		Hold Time	10		nS
PW_{LW}	WR	Pulse Width (low-level) Write	65	–	nS
PW_{LR}	RD	Read	150	–	nS
PW_{HW}	WR	Pulse Width (high-level) Write	65	–	nS
PW_{HR}	RD	Read	150	–	nS
t_{WRr}, t_{WRf}	WR, RD	Write/Read Rise/Fall Time		25	nS
t_{CYCW}	WR	Bus Cycle Time Write	130	–	nS
t_{CYCR}	RD	Read	300		
t_{DSW}	WR	Write Data Setup Time	10		nS
t_{HWR}		Hold Time	10		nS
t_{DDR}	RD	Read Data Delay Time		150	nS
t_{DHR}		Hold Hime	55		nS

(2.5V ≤ V_{D1} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Min.	Max.	Units
t_{AS}	RS to CS,WR,RD	Address Setup Time	10	–	nS
t_{AH}		Hold Time	10		nS
PW_{LW}	WR	Pulse Width (low-level) Write	60	–	nS
PW_{LR}	RD	Read	150	–	nS
PW_{HW}	WR	Pulse Width (high-level) Write	60	–	nS
PW_{HR}	RD	Read	150	–	nS
t_{WRr}, t_{WRf}	WR, RD	Write/Read Rise/Fall Time		25	nS
t_{CYCW}	WR	Bus Cycle Time Write	120	–	nS
t_{CYCR}	RD	Read	300		
t_{DSW}	DB0-DB17 WR	Write Data Setup Time	10		nS
t_{HWR}		Hold Time	10		nS
t_{DDR}	DB0-DB17 RD	Read Data Delay Time		150	nS
t_{DHR}		Hold Time	55		nS

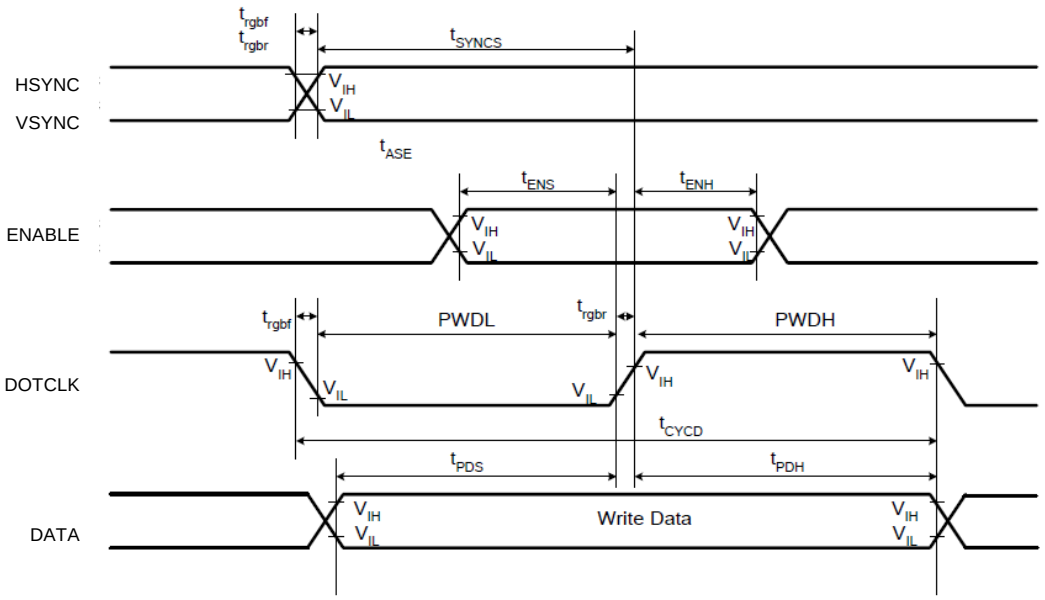


FIGURE 19: Parallel Bus Timing Characteristics (for RGB Interface Mode)

(1.65V ⩽ IOVcc < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Min.	Max.	Units
t_{SYNCS}	HSYNC/ VSYNC	Hsync/Vsync Setup Time	0	–	nS
t_{ENS}	ENABLE	ENABLE Setup Time	10	–	nS
t_{ENH}		ENABLE Hold Time	10	–	nS
PWDH	DOTCLK	Pulse Width DOTCLK (high-level)	50	–	nS
PWDL		(low-level)	50	–	nS
t_{RGBR}, t_{RGBF}		DOTCLK Hsync/Vsync Rise/Fall Time	–	25	nS
t_{CYCD}		DOTCLK Cycle Time	100	–	nS
t_{PDS}	DATA	DATA Setup Time	10	–	nS
t_{PDH}		DATA Hold Time	40	–	nS

(2.5V ⩽ IOVcc < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Min.	Max.	Units
t_{SYNCS}	VSYNC/ HSYNC	Hsync/Vsync Setup Time	5	–	nS
t_{ENS}	ENABLE	ENABLE Setup Time	10	–	nS
t_{ENH}	ENABLE	ENABLE Hold Time	15	–	nS
PWDH	DOTCLK	Pulse Width DOTCLK (high-level)	50	–	nS
PWDL		(low-level)	50	–	nS
t_{RGBR}, t_{RGBF}		DOTCLK Hsync/Vsync Rise/Rall Time	–	25	nS
t_{CYCD}		DOTCLK Cycle Time	100	–	nS
t_{PDS}	DATA	DATA Setup Time	15	–	nS
t_{PDH}		DATA Hold Time	40	–	nS

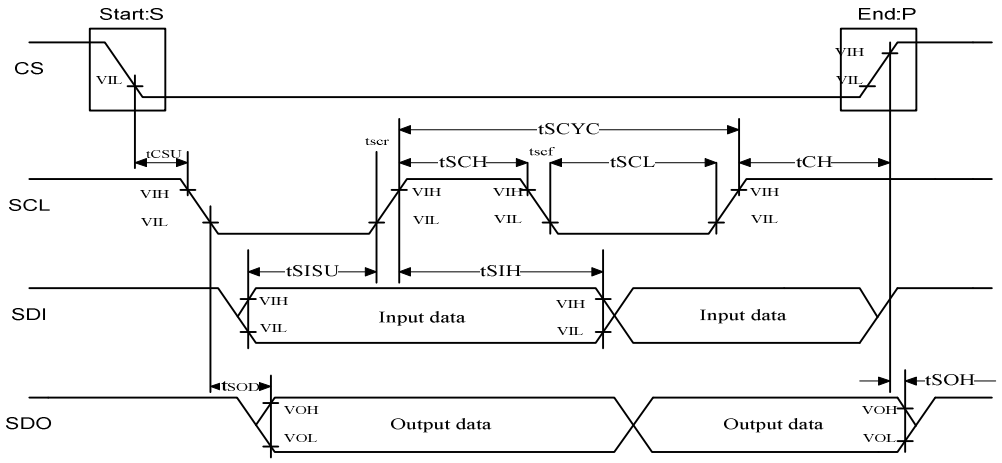


FIGURE 20: Serial Bus Timing Characteristics

Normal Mode :

(1.65V ≤ IOVcc < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Min.	Max.	Units
t_{SCYC}	SCL	Serial Clock Cycle Time Write (received)	200	–	nS
		Read (transmitted)	250		
t_{SCH}		Serial Clock High-level Pulse Width Write (received)	100	–	nS
		Read (transmitted)	125		
t_{SCL}		Serial Clock Low-level Pulse Width Write (received)	100	–	nS
		Read (transmitted)	125		
t_{SCR}, t_{SCF}		Serial Clock Rising/Falling Time		25	nS
t_{CSU}	CS, SCL	Chip Select Setup Time	5	–	nS
t_{CH}		Hole Time	5		nS
t_{SISU}	SDI	Serial Input Data Setup Time	10		nS
t_{SIH}		Hold Time	5		nS
t_{SOD}	SDO	Serial Output Data Delay Time		130	nS
t_{SOH}		Hold Time	60		nS

(2.5V ≤ IOVcc < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Min.	Max.	Units
t_{SCYC}	SCL	Serial Clock Cycle Time Write(received)	200	–	nS
		Read(transmitted)	250		
t_{SCH}		Serial Clock High-level Pulse Width Write(received)	100	–	nS
		Read(transmitted)	125		
t_{SCL}		Serial Clock Low-level Pulse Width Write(received)	100	–	nS
		Read(transmitted)	125		
t_{SCR}, t_{SCF}		Serial Clock Rising/Falling time		25	nS
t_{CSU}	CS, SCL	Chip Select Setup Time	5	–	nS
t_{CH}		Hold Time	5		nS
t_{SISU}	SDI	Serial Input Data Setup Time	10		nS
t_{SIH}		Hold Time	5		nS
t_{SOD}	SDO	Serial Output Data Delay Time		130	nS
t_{SOH}		Hold Time	60		nS

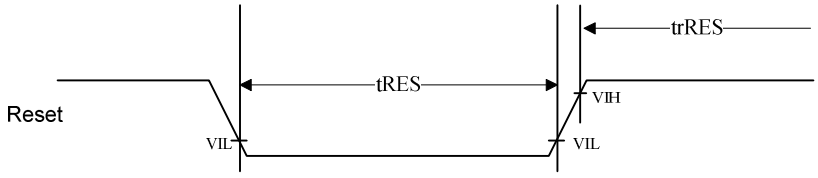


FIGURE 21: Reset Characteristics

(1.65V ≤ IOVcc < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Min.	Max.	Units
t_{RES}	RST	Reset Low Pulse Width	1	–	mS
t_{rRES}		Reset Rise Time	–	10	µS

PHYSICAL DIMENSIONS

PAD COORDINATES

DIE SIZE :
17820 µM x 790 µM ± 40 µM

DIE THICKNESS :
400 µM ± 20 µM

DIE TTV :
(Dmax – Dmin) ⩽ 20 µM

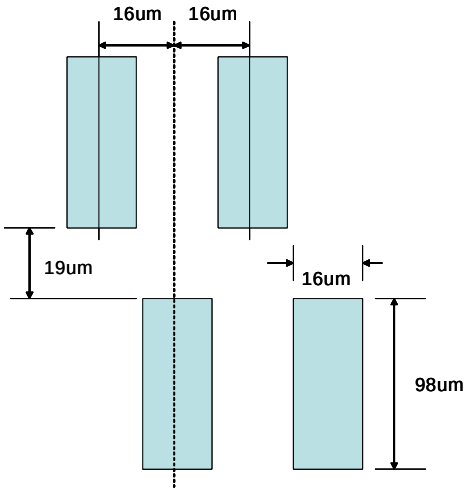
HARDNESS :
60Hv ± 15Hv

BUMP AREA :
1568 μM^2

BUMP SIZE :
16 x 98 μM^2 ± 2 µM

BUMP HEIGHT :
15 µM ± 3 µM

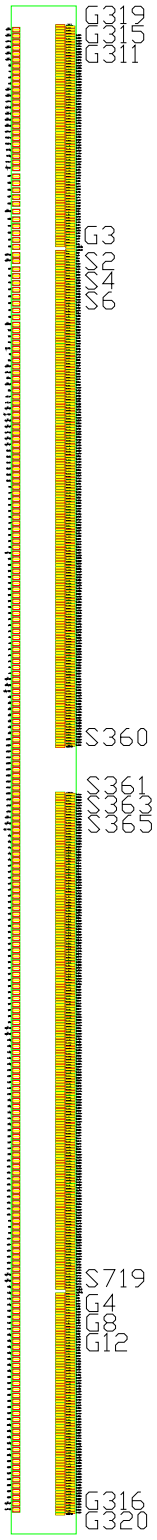
BUMP PITCH :
32 µM



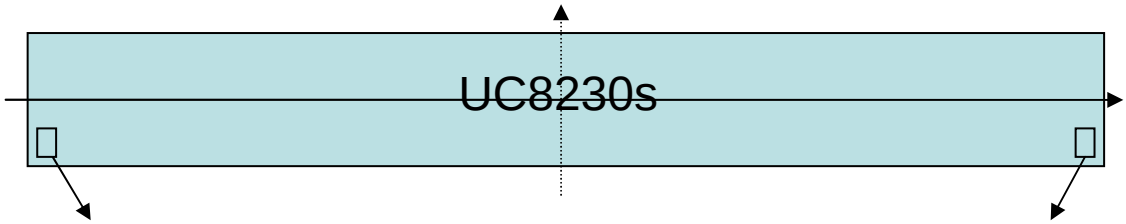
COORDINATE ORIGIN :
Chip center

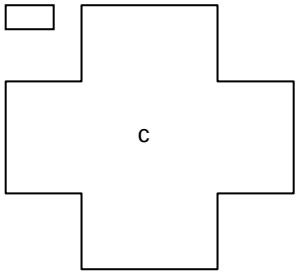
PAD REFERENCE :
Pad center

(Drawing and coordinates are for the Circuit/Bump view.)



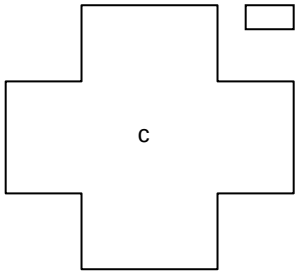
ALIGNMENT MARK INFORMATION





NOTE:

1. Alignment mark is on Metal4 (or top metal).
2. Each mark itself is symmetric both horizontally and vertically.



COORDINATES:

	Down Left Spider Mark (+)		Down Right Spider Mark (+)	
	X	Y	X	Y
C	-8751	269	8751	269

PAD COORDINATES

#	Pad	X	Y	W	H
1	DUMMY	-8610	-307.5	50	80
2	DUMMY	-8540	-307.5	50	80
3	DUMMY	-8470	-307.5	50	80
4	DUMMY	-8400	-307.5	50	80
5	DUMMY	-8330	-307.5	50	80
6	DUMMY	-8260	-307.5	50	80
7	IM0	-8190	-307.5	50	80
8	IM1	-8120	-307.5	50	80
9	IM2	-8050	-307.5	50	80
10	IM3	-7980	-307.5	50	80
11	DUMMY	-7910	-307.5	50	80
12	DUMMY	-7840	-307.5	50	80
13	DUMMY	-7770	-307.5	50	80
14	DUMMY	-7700	-307.5	50	80
15	DUMMY	-7630	-307.5	50	80
16	DUMMY	-7560	-307.5	50	80
17	DUMMY	-7490	-307.5	50	80
18	DUMMY	-7420	-307.5	50	80
19	RESETb	-7350	-307.5	50	80
20	RESETb	-7280	-307.5	50	80
21	VSYNC	-7210	-307.5	50	80
22	HSYNC	-7140	-307.5	50	80
23	DOTCLK	-7070	-307.5	50	80
24	ENABLE	-7000	-307.5	50	80
25	DB17	-6905	-307.5	50	80
26	DB16	-6825	-307.5	50	80
27	DB15	-6745	-307.5	50	80
28	DB14	-6665	-307.5	50	80
29	DB13	-6585	-307.5	50	80
30	DUMMY	-6495	-307.5	50	80
31	DB12	-6405	-307.5	50	80
32	DB11	-6325	-307.5	50	80
33	DB10	-6245	-307.5	50	80
34	DB9	-6165	-307.5	50	80
35	DB8	-6085	-307.5	50	80
36	DUMMY	-5990	-307.5	50	80
37	DUMMY	-5920	-307.5	50	80
38	DB7	-5825	-307.5	50	80
39	DB6	-5745	-307.5	50	80
40	DB5	-5665	-307.5	50	80
41	DB4	-5585	-307.5	50	80
42	DB3	-5505	-307.5	50	80
43	DB2	-5425	-307.5	50	80
44	DB1	-5345	-307.5	50	80
45	DB0	-5265	-307.5	50	80
46	DUMMY	-5180	-307.5	50	80
47	SDO	-5110	-307.5	50	80
48	SDI	-5040	-307.5	50	80
49	RDb	-4970	-307.5	50	80
50	WR_SCL	-4900	-307.5	50	80
51	RS	-4830	-307.5	50	80
52	CSb	-4760	-307.5	50	80
53	DUMMY	-4690	-307.5	50	80
54	DUMMY	-4620	-307.5	50	80
55	FMARK	-4550	-307.5	50	80
56	DUMMY	-4480	-307.5	50	80
57	OSC	-4410	-307.5	50	80
58	VD1_on	-4340	-307.5	50	80
59	VD2_on	-4270	-307.5	50	80
60	DUMMY	-4200	-307.5	50	80
61	INIT_TEST	-4130	-307.5	50	80
62	DUMMY	-4060	-307.5	50	80
63	DUMMY	-3990	-307.5	50	80
64	DUMMY	-3920	-307.5	50	80
65	DUMMY	-3850	-307.5	50	80
66	DUMMY	-3780	-307.5	50	80
67	IOVCC	-3710	-307.5	50	80
68	IOVCC	-3640	-307.5	50	80
69	IOVCC	-3570	-307.5	50	80
70	IOVCC	-3500	-307.5	50	80
71	IOVCC	-3430	-307.5	50	80
72	IOVCC	-3360	-307.5	50	80
73	VD1	-3290	-307.5	50	80
74	VD1	-3220	-307.5	50	80
75	VD1	-3150	-307.5	50	80
76	VD1	-3080	-307.5	50	80
77	VD1	-3010	-307.5	50	80
78	VD1	-2940	-307.5	50	80
79	VD1	-2870	-307.5	50	80
80	VD1	-2800	-307.5	50	80
81	VD1	-2730	-307.5	50	80
82	VD1	-2660	-307.5	50	80
83	VD1	-2590	-307.5	50	80
84	DUMMY	-2520	-307.5	50	80
85	VS2	-2450	-307.5	50	80
86	VS2	-2380	-307.5	50	80
87	VS2	-2310	-307.5	50	80
88	VS2	-2240	-307.5	50	80
89	VS2	-2170	-307.5	50	80
90	VS2	-2100	-307.5	50	80
91	VS2	-2030	-307.5	50	80
92	VS2	-1960	-307.5	50	80
93	VGS	-1890	-307.5	50	80
94	VGS	-1820	-307.5	50	80
95	vss	-1750	-307.5	50	80
96	vss	-1680	-307.5	50	80
97	vss	-1610	-307.5	50	80
98	vss	-1540	-307.5	50	80
99	vss	-1470	-307.5	50	80
100	vss	-1400	-307.5	50	80
101	vss	-1330	-307.5	50	80
102	vss	-1260	-307.5	50	80
103	vss	-1190	-307.5	50	80
104	vss	-1120	-307.5	50	80
105	DUMMY	-1050	-307.5	50	80
106	DUMMY	-980	-307.5	50	80
107	COM_TEST	-910	-307.5	50	80
108	COM	-840	-307.5	50	80
109	COM	-770	-307.5	50	80
110	COM	-700	-307.5	50	80
111	COM	-630	-307.5	50	80
112	COM	-560	-307.5	50	80
113	COM	-490	-307.5	50	80
114	COM	-420	-307.5	50	80
115	VCOMH	-350	-307.5	50	80
116	VCOMH	-280	-307.5	50	80
117	VCOMH	-210	-307.5	50	80
118	VCOMH	-140	-307.5	50	80
119	VCOMH	-70	-307.5	50	80
120	VCOMH	0	-307.5	50	80
121	VCOML	70	-307.5	50	80
122	VCOML	140	-307.5	50	80
123	VCOML	210	-307.5	50	80
124	VCOML	280	-307.5	50	80
125	VREG1	350	-307.5	50	80
126	VREG1	420	-307.5	50	80
127	VREG1	490	-307.5	50	80
128	DUMMY	560	-307.5	50	80
129	DUMMY	630	-307.5	50	80
130	SRC_TEST	700	-307.5	50	80
131	VSN	770	-307.5	50	80
132	VSN	840	-307.5	50	80
133	VSN	910	-307.5	50	80
134	VSN	980	-307.5	50	80
135	VSN	1050	-307.5	50	80
136	VD4	1120	-307.5	50	80
137	VD4	1190	-307.5	50	80
138	VD4	1260	-307.5	50	80
139	VD4	1330	-307.5	50	80
140	VD4	1400	-307.5	50	80
141	VD4	1470	-307.5	50	80
142	VD2	1540	-307.5	50	80
143	VD2	1610	-307.5	50	80
144	VD2	1680	-307.5	50	80
145	VCC	1750	-307.5	50	80
146	VCC	1820	-307.5	50	80
147	VCC	1890	-307.5	50	80
148	VCC	1960	-307.5	50	80
149	VCC	2030	-307.5	50	80
150	VCC	2100	-307.5	50	80
151	VCC	2170	-307.5	50	80
152	VCC	2240	-307.5	50	80
153	VCC	2310	-307.5	50	80
154	VCC	2380	-307.5	50	80
155	VCC	2450	-307.5	50	80
156	VCC	2520	-307.5	50	80
157	VCC	2590	-307.5	50	80
158	VCC	2660	-307.5	50	80
159	VCC	2730	-307.5	50	80
160	VCC	2800	-307.5	50	80
161	VCC	2870	-307.5	50	80
162	VCC	2940	-307.5	50	80
163	DUMMY	3010	-307.5	50	80
164	DUMMY	3080	-307.5	50	80
165	C12-	3150	-307.5	50	80
166	C12-	3220	-307.5	50	80
167	C12-	3290	-307.5	50	80
168	C12-	3360	-307.5	50	80
169	C12-	3430	-307.5	50	80
170	C12+	3500	-307.5	50	80
171	C12+	3570	-307.5	50	80
172	C12+	3640	-307.5	50	80
173	C12+	3710	-307.5	50	80
174	C12+	3780	-307.5	50	80
175	C11-	3850	-307.5	50	80
176	C11-	3920	-307.5	50	80
177	C11-	3990	-307.5	50	80
178	C11-	4060	-307.5	50	80
179	C11-	4130	-307.5	50	80
180	C11+	4200	-307.5	50	80
181	C11+	4270	-307.5	50	80
182	C11+	4340	-307.5	50	80
183	C11+	4410	-307.5	50	80
184	C11+	4480	-307.5	50	80
185	VCCL	4550	-307.5	50	80
186	VCCL	4620	-307.5	50	80
187	VCCL	4690	-307.5	50	80
188	VCCL	4760	-307.5	50	80
189	VCCL	4830	-307.5	50	80
190	VCCL	4900	-307.5	50	80
191	VCCL	4970	-307.5	50	80
192	VCCL	5040	-307.5	50	80
193	VCCL	5110	-307.5	50	80
194	VCCL	5180	-307.5	50	80
195	vss	5250	-307.5	50	80
196	vss	5320	-307.5	50	80
197	vss	5390	-307.5	50	80
198	VCCH	5460	-307.5	50	80
199	VCCH	5530	-307.5	50	80
200	VCCH	5600	-307.5	50	80
201	VCCH	5670	-307.5	50	80
202	VCCH	5740	-307.5	50	80
203	VCCH	5810	-307.5	50	80
204	DUMMY	5880	-307.5	50	80
205	DUMMY	5950	-307.5	50	80
206	C13-	6020	-307.5	50	80
207	C13-	6090	-307.5	50	80
208	C13-	6160	-307.5	50	80
209	C13-	6230	-307.5	50	80
210	C13+	6300	-307.5	50	80
211	C13+	6370	-307.5	50	80
212	C13+	6440	-307.5	50	80
213	C13+	6510	-307.5	50	80
214	C21-	6580	-307.5	50	80
215	C21-	6650	-307.5	50	80
216	C21-	6720	-307.5	50	80
217	C21-	6790	-307.5	50	80
218	C21-	6860	-307.5	50	80
219	C21-	6930	-307.5	50	80
220	C21-	7000	-307.5	50	80
221	C21+	7070	-307.5	50	80
222	C21+	7140	-307.5	50	80
223	C21+	7210	-307.5	50	80
224	C21+	7280	-307.5	50	80
225	C21+	7350	-307.5	50	80
226	C21+	7420	-307.5	50	80
227	C21+	7490	-307.5	50	80
228	C22-	7560	-307.5	50	80
229	C22-	7630	-307.5	50	80
230	C22-	7700	-307.5	50	80
231	C22-	7770	-307.5	50	80
232	C22-	7840	-307.5	50	80
233	C22-	7910	-307.5	50	80
234	C22-	7980	-307.5	50	80
235	C22+	8050	-307.5	50	80
236	C22+	8120	-307.5	50	80
237	C22+	8190	-307.5	50	80
238	C22+	8260	-307.5	50	80
239	C22+	8330	-307.5	50	80
240	C22+	8400	-307.5	50	80

#	Pad	X	Y	W	H
241	C22+	8470	-307.5	50	80
242	DUMMY	8540	-307.5	50	80
243	DUMMY	8610	-307.5	50	80
244	DUMMY	8659	202.5	16	98
245	G320	8643	319.5	16	98
246	G318	8627	202.5	16	98
247	G316	8611	319.5	16	98
248	G314	8595	202.5	16	98
249	G312	8579	319.5	16	98
250	G310	8563	202.5	16	98
251	G308	8547	319.5	16	98
252	G306	8531	202.5	16	98
253	G304	8515	319.5	16	98
254	G302	8499	202.5	16	98
255	G300	8483	319.5	16	98
256	G298	8467	202.5	16	98
257	G296	8451	319.5	16	98
258	G294	8435	202.5	16	98
259	G292	8419	319.5	16	98
260	G290	8403	202.5	16	98
261	G288	8387	319.5	16	98
262	G286	8371	202.5	16	98
263	G284	8355	319.5	16	98
264	G282	8339	202.5	16	98
265	G280	8323	319.5	16	98
266	G278	8307	202.5	16	98
267	G276	8291	319.5	16	98
268	G274	8275	202.5	16	98
269	G272	8259	319.5	16	98
270	G270	8243	202.5	16	98
271	G268	8227	319.5	16	98
272	G266	8211	202.5	16	98
273	G264	8195	319.5	16	98
274	G262	8179	202.5	16	98
275	G260	8163	319.5	16	98
276	G258	8147	202.5	16	98
277	G256	8131	319.5	16	98
278	G254	8115	202.5	16	98
279	G252	8099	319.5	16	98
280	G250	8083	202.5	16	98
281	G248	8067	319.5	16	98
282	G246	8051	202.5	16	98
283	G244	8035	319.5	16	98
284	G242	8019	202.5	16	98
285	G240	8003	319.5	16	98
286	G238	7987	202.5	16	98
287	G236	7971	319.5	16	98
288	G234	7955	202.5	16	98
289	G232	7939	319.5	16	98
290	G230	7923	202.5	16	98
291	G228	7907	319.5	16	98
292	G226	7891	202.5	16	98
293	G224	7875	319.5	16	98
294	G222	7859	202.5	16	98
295	G220	7843	319.5	16	98
296	G218	7827	202.5	16	98
297	G216	7811	319.5	16	98
298	G214	7795	202.5	16	98
299	G212	7779	319.5	16	98
300	G210	7763	202.5	16	98
301	G208	7747	319.5	16	98
302	G206	7731	202.5	16	98
303	G204	7715	319.5	16	98
304	G202	7699	202.5	16	98
305	G200	7683	319.5	16	98
306	G198	7667	202.5	16	98
307	G196	7651	319.5	16	98
308	G194	7635	202.5	16	98
309	G192	7619	319.5	16	98
310	G190	7603	202.5	16	98
311	G188	7587	319.5	16	98
312	G186	7571	202.5	16	98
313	G184	7555	319.5	16	98
314	G182	7539	202.5	16	98
315	G180	7523	319.5	16	98
316	G178	7507	202.5	16	98
317	G176	7491	319.5	16	98
318	G174	7475	202.5	16	98
319	G172	7459	319.5	16	98
320	G170	7443	202.5	16	98
321	G168	7427	319.5	16	98
322	G166	7411	202.5	16	98
323	G164	7395	319.5	16	98

#	Pad	X	Y	W	H
324	G162	7379	202.5	16	98
325	G160	7363	319.5	16	98
326	G158	7347	202.5	16	98
327	G156	7331	319.5	16	98
328	G154	7315	202.5	16	98
329	G152	7299	319.5	16	98
330	G150	7283	202.5	16	98
331	G148	7267	319.5	16	98
332	G146	7251	202.5	16	98
333	G144	7235	319.5	16	98
334	G142	7219	202.5	16	98
335	G140	7203	319.5	16	98
336	G138	7187	202.5	16	98
337	G136	7171	319.5	16	98
338	G134	7155	202.5	16	98
339	G132	7139	319.5	16	98
340	G130	7123	202.5	16	98
341	G128	7107	319.5	16	98
342	G126	7091	202.5	16	98
343	G124	7075	319.5	16	98
344	G122	7059	202.5	16	98
345	G120	7043	319.5	16	98
346	G118	7027	202.5	16	98
347	G116	7011	319.5	16	98
348	G114	6995	202.5	16	98
349	G112	6979	319.5	16	98
350	G110	6963	202.5	16	98
351	G108	6947	319.5	16	98
352	G106	6931	202.5	16	98
353	G104	6915	319.5	16	98
354	G102	6899	202.5	16	98
355	G100	6883	319.5	16	98
356	G98	6867	202.5	16	98
357	G96	6851	319.5	16	98
358	G94	6835	202.5	16	98
359	G92	6819	319.5	16	98
360	G90	6803	202.5	16	98
361	G88	6787	319.5	16	98
362	G86	6771	202.5	16	98
363	G84	6755	319.5	16	98
364	G82	6739	202.5	16	98
365	G80	6723	319.5	16	98
366	G78	6707	202.5	16	98
367	G76	6691	319.5	16	98
368	G74	6675	202.5	16	98
369	G72	6659	319.5	16	98
370	G70	6643	202.5	16	98
371	G68	6627	319.5	16	98
372	G66	6611	202.5	16	98
373	G64	6595	319.5	16	98
374	G62	6579	202.5	16	98
375	G60	6563	319.5	16	98
376	G58	6547	202.5	16	98
377	G56	6531	319.5	16	98
378	G54	6515	202.5	16	98
379	G52	6499	319.5	16	98
380	G50	6483	202.5	16	98
381	G48	6467	319.5	16	98
382	G46	6451	202.5	16	98
383	G44	6435	319.5	16	98
384	G42	6419	202.5	16	98
385	G40	6403	319.5	16	98
386	G38	6387	202.5	16	98
387	G36	6371	319.5	16	98
388	G34	6355	202.5	16	98
389	G32	6339	319.5	16	98
390	G30	6323	202.5	16	98
391	G28	6307	319.5	16	98
392	G26	6291	202.5	16	98
393	G24	6275	319.5	16	98
394	G22	6259	202.5	16	98
395	G20	6243	319.5	16	98
396	G18	6227	202.5	16	98
397	G16	6211	319.5	16	98
398	G14	6195	202.5	16	98
399	G12	6179	319.5	16	98
400	G10	6163	202.5	16	98
401	G8	6147	319.5	16	98
402	G6	6131	202.5	16	98
403	G4	6115	319.5	16	98
404	G2	6099	202.5	16	98
405	DUMMY	6083	319.5	16	98
406	DUMMY	6047	319.5	16	98

#	Pad	X	Y	W	H
407	S720	6031	202.5	16	98
408	S719	6015	319.5	16	98
409	S718	5999	202.5	16	98
410	S717	5983	319.5	16	98
411	S716	5967	202.5	16	98
412	S715	5951	319.5	16	98
413	S714	5935	202.5	16	98
414	S713	5919	319.5	16	98
415	S712	5903	202.5	16	98
416	S711	5887	319.5	16	98
417	S710	5871	202.5	16	98
418	S709	5855	319.5	16	98
419	S708	5839	202.5	16	98
420	S707	5823	319.5	16	98
421	S706	5807	202.5	16	98
422	S705	5791	319.5	16	98
423	S704	5775	202.5	16	98
424	S703	5759	319.5	16	98
425	S702	5743	202.5	16	98
426	S701	5727	319.5	16	98
427	S700	5711	202.5	16	98
428	S699	5695	319.5	16	98
429	S698	5679	202.5	16	98
430	S697	5663	319.5	16	98
431	S696	5647	202.5	16	98
432	S695	5631	319.5	16	98
433	S694	5615	202.5	16	98
434	S693	5599	319.5	16	98
435	S692	5583	202.5	16	98
436	S691	5567	319.5	16	98
437	S690	5551	202.5	16	98
438	S689	5535	319.5	16	98
439	S688	5519	202.5	16	98
440	S687	5503	319.5	16	98
441	S686	5487	202.5	16	98
442	S685	5471	319.5	16	98
443	S684	5455	202.5	16	98
444	S683	5439	319.5	16	98
445	S682	5423	202.5	16	98
446	S681	5407	319.5	16	98
447	S680	5391	202.5	16	98
448	S679	5375	319.5	16	98
449	S678	5359	202.5	16	98
450	S677	5343	319.5	16	98
451	S676	5327	202.5	16	98
452	S675	5311	319.5	16	98
453	S674	5295	202.5	16	98
454	S673	5279	319.5	16	98
455	S672	5263	202.5	16	98
456	S671	5247	319.5	16	98
457	S670	5231	202.5	16	98
458	S669	5215	319.5	16	98
459	S668	5199	202.5	16	98
460	S667	5183	319.5	16	98
461	S666	5167	202.5	16	98
462	S665	5151	319.5	16	98
463	S664	5135	202.5	16	98
464	S663	5119	319.5	16	98
465	S662	5103	202.5	16	98
466	S661	5087	319.5	16	98
467	S660	5071	202.5	16	98
468	S659	5055	319.5	16	98
469	S658	5039	202.5	16	98
470	S657	5023	319.5	16	98
471	S656	5007	202.5	16	98
472	S655	4991	319.5	16	98
473	S654	4975	202.5	16	98
474	S653	4959	319.5	16	98
475	S652	4943	202.5	16	98
476	S651	4927	319.5	16	98
477	S650	4911	202.5	16	98
478	S649	4895	319.5	16	98
479	S648	4879	202.5	16	98
480	S647	4863	319.5	16	98
481	S646	4847	202.5	16	98
482	S645	4831	319.5	16	98
483	S644	4815	202.5	16	98
484	S643	4799	319.5	16	98
485	S642	4783	202.5	16	98
486	S641	4767	319.5	16	98
487	S640	4751	202.5	16	98
488	S639	4735	319.5	16	98
489	S638	4719	202.5	16	98

#	Pad	X	Y	W	H
490	S637	4703	319.5	16	98
491	S636	4687	202.5	16	98
492	S635	4671	319.5	16	98
493	S634	4655	202.5	16	98
494	S633	4639	319.5	16	98
495	S632	4623	202.5	16	98
496	S631	4607	319.5	16	98
497	S630	4591	202.5	16	98
498	S629	4575	319.5	16	98
499	S628	4559	202.5	16	98
500	S627	4543	319.5	16	98
501	S626	4527	202.5	16	98
502	S625	4511	319.5	16	98
503	S624	4495	202.5	16	98
504	S623	4479	319.5	16	98
505	S622	4463	202.5	16	98
506	S621	4447	319.5	16	98
507	S620	4431	202.5	16	98
508	S619	4415	319.5	16	98
509	S618	4399	202.5	16	98
510	S617	4383	319.5	16	98
511	S616	4367	202.5	16	98
512	S615	4351	319.5	16	98
513	S614	4335	202.5	16	98
514	S613	4319	319.5	16	98
515	S612	4303	202.5	16	98
516	S611	4287	319.5	16	98
517	S610	4271	202.5	16	98
518	S609	4255	319.5	16	98
519	S608	4239	202.5	16	98
520	S607	4223	319.5	16	98
521	S606	4207	202.5	16	98
522	S605	4191	319.5	16	98
523	S604	4175	202.5	16	98
524	S603	4159	319.5	16	98
525	S602	4143	202.5	16	98
526	S601	4127	319.5	16	98
527	S600	4111	202.5	16	98
528	S599	4095	319.5	16	98
529	S598	4079	202.5	16	98
530	S597	4063	319.5	16	98
531	S596	4047	202.5	16	98
532	S595	4031	319.5	16	98
533	S594	4015	202.5	16	98
534	S593	3999	319.5	16	98
535	S592	3983	202.5	16	98
536	S591	3967	319.5	16	98
537	S590	3951	202.5	16	98
538	S589	3935	319.5	16	98
539	S588	3919	202.5	16	98
540	S587	3903	319.5	16	98
541	S586	3887	202.5	16	98
542	S585	3871	319.5	16	98
543	S584	3855	202.5	16	98
544	S583	3839	319.5	16	98
545	S582	3823	202.5	16	98
546	S581	3807	319.5	16	98
547	S580	3791	202.5	16	98
548	S579	3775	319.5	16	98
549	S578	3759	202.5	16	98
550	S577	3743	319.5	16	98
551	S576	3727	202.5	16	98
552	S575	3711	319.5	16	98
553	S574	3695	202.5	16	98
554	S573	3679	319.5	16	98
555	S572	3663	202.5	16	98
556	S571	3647	319.5	16	98
557	S570	3631	202.5	16	98
558	S569	3615	319.5	16	98
559	S568	3599	202.5	16	98
560	S567	3583	319.5	16	98
561	S566	3567	202.5	16	98
562	S565	3551	319.5	16	98
563	S564	3535	202.5	16	98
564	S563	3519	319.5	16	98
565	S562	3503	202.5	16	98
566	S561	3487	319.5	16	98
567	S560	3471	202.5	16	98
568	S559	3455	319.5	16	98
569	S558	3439	202.5	16	98
570	S557	3423	319.5	16	98
571	S556	3407	202.5	16	98
572	S555	3391	319.5	16	98
573	S554	3375	202.5	16	98
574	S553	3359	319.5	16	98
575	S552	3343	202.5	16	98
576	S551	3327	319.5	16	98
577	S550	3311	202.5	16	98
578	S549	3295	319.5	16	98
579	S548	3279	202.5	16	98
580	S547	3263	319.5	16	98
581	S546	3247	202.5	16	98
582	S545	3231	319.5	16	98
583	S544	3215	202.5	16	98
584	S543	3199	319.5	16	98
585	S542	3183	202.5	16	98
586	S541	3167	319.5	16	98
587	S540	3151	202.5	16	98
588	S539	3135	319.5	16	98
589	S538	3119	202.5	16	98
590	S537	3103	319.5	16	98
591	S536	3087	202.5	16	98
592	S535	3071	319.5	16	98
593	S534	3055	202.5	16	98
594	S533	3039	319.5	16	98
595	S532	3023	202.5	16	98
596	S531	3007	319.5	16	98
597	S530	2991	202.5	16	98
598	S529	2975	319.5	16	98
599	S528	2959	202.5	16	98
600	S527	2943	319.5	16	98
601	S526	2927	202.5	16	98
602	S525	2911	319.5	16	98
603	S524	2895	202.5	16	98
604	S523	2879	319.5	16	98
605	S522	2863	202.5	16	98
606	S521	2847	319.5	16	98
607	S520	2831	202.5	16	98
608	S519	2815	319.5	16	98
609	S518	2799	202.5	16	98
610	S517	2783	319.5	16	98
611	S516	2767	202.5	16	98
612	S515	2751	319.5	16	98
613	S514	2735	202.5	16	98
614	S513	2719	319.5	16	98
615	S512	2703	202.5	16	98
616	S511	2687	319.5	16	98
617	S510	2671	202.5	16	98
618	S509	2655	319.5	16	98
619	S508	2639	202.5	16	98
620	S507	2623	319.5	16	98
621	S506	2607	202.5	16	98
622	S505	2591	319.5	16	98
623	S504	2575	202.5	16	98
624	S503	2559	319.5	16	98
625	S502	2543	202.5	16	98
626	S501	2527	319.5	16	98
627	S500	2511	202.5	16	98
628	S499	2495	319.5	16	98
629	S498	2479	202.5	16	98
630	S497	2463	319.5	16	98
631	S496	2447	202.5	16	98
632	S495	2431	319.5	16	98
633	S494	2415	202.5	16	98
634	S493	2399	319.5	16	98
635	S492	2383	202.5	16	98
636	S491	2367	319.5	16	98
637	S490	2351	202.5	16	98
638	S489	2335	319.5	16	98
639	S488	2319	202.5	16	98
640	S487	2303	319.5	16	98
641	S486	2287	202.5	16	98
642	S485	2271	319.5	16	98
643	S484	2255	202.5	16	98
644	S483	2239	319.5	16	98
645	S482	2223	202.5	16	98
646	S481	2207	319.5	16	98
647	S480	2191	202.5	16	98
648	S479	2175	319.5	16	98
649	S478	2159	202.5	16	98
650	S477	2143	319.5	16	98
651	S476	2127	202.5	16	98
652	S475	2111	319.5	16	98
653	S474	2095	202.5	16	98
654	S473	2079	319.5	16	98
655	S472	2063	202.5	16	98
656	S471	2047	319.5	16	98
657	S470	2031	202.5	16	98
658	S469	2015	319.5	16	98
659	S468	1999	202.5	16	98
660	S467	1983	319.5	16	98
661	S466	1967	202.5	16	98
662	S465	1951	319.5	16	98
663	S464	1935	202.5	16	98
664	S463	1919	319.5	16	98
665	S462	1903	202.5	16	98
666	S461	1887	319.5	16	98
667	S460	1871	202.5	16	98
668	S459	1855	319.5	16	98
669	S458	1839	202.5	16	98
670	S457	1823	319.5	16	98
671	S456	1807	202.5	16	98
672	S455	1791	319.5	16	98
673	S454	1775	202.5	16	98
674	S453	1759	319.5	16	98
675	S452	1743	202.5	16	98
676	S451	1727	319.5	16	98
677	S450	1711	202.5	16	98
678	S449	1695	319.5	16	98
679	S448	1679	202.5	16	98
680	S447	1663	319.5	16	98
681	S446	1647	202.5	16	98
682	S445	1631	319.5	16	98
683	S444	1615	202.5	16	98
684	S443	1599	319.5	16	98
685	S442	1583	202.5	16	98
686	S441	1567	319.5	16	98
687	S440	1551	202.5	16	98
688	S439	1535	319.5	16	98
689	S438	1519	202.5	16	98
690	S437	1503	319.5	16	98
691	S436	1487	202.5	16	98
692	S435	1471	319.5	16	98
693	S434	1455	202.5	16	98
694	S433	1439	319.5	16	98
695	S432	1423	202.5	16	98
696	S431	1407	319.5	16	98
697	S430	1391	202.5	16	98
698	S429	1375	319.5	16	98
699	S428	1359	202.5	16	98
700	S427	1343	319.5	16	98
701	S426	1327	202.5	16	98
702	S425	1311	319.5	16	98
703	S424	1295	202.5	16	98
704	S423	1279	319.5	16	98
705	S422	1263	202.5	16	98
706	S421	1247	319.5	16	98
707	S420	1231	202.5	16	98
708	S419	1215	319.5	16	98
709	S418	1199	202.5	16	98
710	S417	1183	319.5	16	98
711	S416	1167	202.5	16	98
712	S415	1151	319.5	16	98
713	S414	1135	202.5	16	98
714	S413	1119	319.5	16	98
715	S412	1103	202.5	16	98
716	S411	1087	319.5	16	98
717	S410	1071	202.5	16	98
718	S409	1055	319.5	16	98
719	S408	1039	202.5	16	98
720	S407	1023	319.5	16	98
721	S406	1007	202.5	16	98
722	S405	991	319.5	16	98
723	S404	975	202.5	16	98
724	S403	959	319.5	16	98
725	S402	943	202.5	16	98
726	S401	927	319.5	16	98
727	S400	911	202.5	16	98
728	S399	895	319.5	16	98
729	S398	879	202.5	16	98
730	S397	863	319.5	16	98
731	S396	847	202.5	16	98
732	S395	831	319.5	16	98
733	S394	815	202.5	16	98
734	S393	799	319.5	16	98
735	S392	783	202.5	16	98
736	S391	767	319.5	16	98
737	S390	751	202.5	16	98
738	S389	735	319.5	16	98

#	Pad	X	Y	W	H
739	S388	719	202.5	16	98
740	S387	703	319.5	16	98
741	S386	687	202.5	16	98
742	S385	671	319.5	16	98
743	S384	655	202.5	16	98
744	S383	639	319.5	16	98
745	S382	623	202.5	16	98
746	S381	607	319.5	16	98
747	S380	591	202.5	16	98
748	S379	575	319.5	16	98
749	S378	559	202.5	16	98
750	S377	543	319.5	16	98
751	S376	527	202.5	16	98
752	S375	511	319.5	16	98
753	S374	495	202.5	16	98
754	S373	479	319.5	16	98
755	S372	463	202.5	16	98
756	S371	447	319.5	16	98
757	S370	431	202.5	16	98
758	S369	415	319.5	16	98
759	S368	399	202.5	16	98
760	S367	383	319.5	16	98
761	S366	367	202.5	16	98
762	S365	351	319.5	16	98
763	S364	335	202.5	16	98
764	S363	319	319.5	16	98
765	S362	303	202.5	16	98
766	S361	287	319.5	16	98
767	DUMMY	271	202.5	16	98
768	DUMMY	-271	202.5	16	98
769	S360	-287	319.5	16	98
770	S359	-303	202.5	16	98
771	S358	-319	319.5	16	98
772	S357	-335	202.5	16	98
773	S356	-351	319.5	16	98
774	S355	-367	202.5	16	98
775	S354	-383	319.5	16	98
776	S353	-399	202.5	16	98
777	S352	-415	319.5	16	98
778	S351	-431	202.5	16	98
779	S350	-447	319.5	16	98
780	S349	-463	202.5	16	98
781	S348	-479	319.5	16	98
782	S347	-495	202.5	16	98
783	S346	-511	319.5	16	98
784	S345	-527	202.5	16	98
785	S344	-543	319.5	16	98
786	S343	-559	202.5	16	98
787	S342	-575	319.5	16	98
788	S341	-591	202.5	16	98
789	S340	-607	319.5	16	98
790	S339	-623	202.5	16	98
791	S338	-639	319.5	16	98
792	S337	-655	202.5	16	98
793	S336	-671	319.5	16	98
794	S335	-687	202.5	16	98
795	S334	-703	319.5	16	98
796	S333	-719	202.5	16	98
797	S332	-735	319.5	16	98
798	S331	-751	202.5	16	98
799	S330	-767	319.5	16	98
800	S329	-783	202.5	16	98
801	S328	-799	319.5	16	98
802	S327	-815	202.5	16	98
803	S326	-831	319.5	16	98
804	S325	-847	202.5	16	98
805	S324	-863	319.5	16	98
806	S323	-879	202.5	16	98
807	S322	-895	319.5	16	98
808	S321	-911	202.5	16	98
809	S320	-927	319.5	16	98
810	S319	-943	202.5	16	98
811	S318	-959	319.5	16	98
812	S317	-975	202.5	16	98
813	S316	-991	319.5	16	98
814	S315	-1007	202.5	16	98
815	S314	-1023	319.5	16	98
816	S313	-1039	202.5	16	98
817	S312	-1055	319.5	16	98
818	S311	-1071	202.5	16	98
819	S310	-1087	319.5	16	98
820	S309	-1103	202.5	16	98
821	S308	-1119	319.5	16	98
822	S307	-1135	202.5	16	98
823	S306	-1151	319.5	16	98
824	S305	-1167	202.5	16	98
825	S304	-1183	319.5	16	98
826	S303	-1199	202.5	16	98
827	S302	-1215	319.5	16	98
828	S301	-1231	202.5	16	98
829	S300	-1247	319.5	16	98
830	S299	-1263	202.5	16	98
831	S298	-1279	319.5	16	98
832	S297	-1295	202.5	16	98
833	S296	-1311	319.5	16	98
834	S295	-1327	202.5	16	98
835	S294	-1343	319.5	16	98
836	S293	-1359	202.5	16	98
837	S292	-1375	319.5	16	98
838	S291	-1391	202.5	16	98
839	S290	-1407	319.5	16	98
840	S289	-1423	202.5	16	98
841	S288	-1439	319.5	16	98
842	S287	-1455	202.5	16	98
843	S286	-1471	319.5	16	98
844	S285	-1487	202.5	16	98
845	S284	-1503	319.5	16	98
846	S283	-1519	202.5	16	98
847	S282	-1535	319.5	16	98
848	S281	-1551	202.5	16	98
849	S280	-1567	319.5	16	98
850	S279	-1583	202.5	16	98
851	S278	-1599	319.5	16	98
852	S277	-1615	202.5	16	98
853	S276	-1631	319.5	16	98
854	S275	-1647	202.5	16	98
855	S274	-1663	319.5	16	98
856	S273	-1679	202.5	16	98
857	S272	-1695	319.5	16	98
858	S271	-1711	202.5	16	98
859	S270	-1727	319.5	16	98
860	S269	-1743	202.5	16	98
861	S268	-1759	319.5	16	98
862	S267	-1775	202.5	16	98
863	S266	-1791	319.5	16	98
864	S265	-1807	202.5	16	98
865	S264	-1823	319.5	16	98
866	S263	-1839	202.5	16	98
867	S262	-1855	319.5	16	98
868	S261	-1871	202.5	16	98
869	S260	-1887	319.5	16	98
870	S259	-1903	202.5	16	98
871	S258	-1919	319.5	16	98
872	S257	-1935	202.5	16	98
873	S256	-1951	319.5	16	98
874	S255	-1967	202.5	16	98
875	S254	-1983	319.5	16	98
876	S253	-1999	202.5	16	98
877	S252	-2015	319.5	16	98
878	S251	-2031	202.5	16	98
879	S250	-2047	319.5	16	98
880	S249	-2063	202.5	16	98
881	S248	-2079	319.5	16	98
882	S247	-2095	202.5	16	98
883	S246	-2111	319.5	16	98
884	S245	-2127	202.5	16	98
885	S244	-2143	319.5	16	98
886	S243	-2159	202.5	16	98
887	S242	-2175	319.5	16	98
888	S241	-2191	202.5	16	98
889	S240	-2207	319.5	16	98
890	S239	-2223	202.5	16	98
891	S238	-2239	319.5	16	98
892	S237	-2255	202.5	16	98
893	S236	-2271	319.5	16	98
894	S235	-2287	202.5	16	98
895	S234	-2303	319.5	16	98
896	S233	-2319	202.5	16	98
897	S232	-2335	319.5	16	98
898	S231	-2351	202.5	16	98
899	S230	-2367	319.5	16	98
900	S229	-2383	202.5	16	98
901	S228	-2399	319.5	16	98
902	S227	-2415	202.5	16	98
903	S226	-2431	319.5	16	98
904	S225	-2447	202.5	16	98
905	S224	-2463	319.5	16	98
906	S223	-2479	202.5	16	98
907	S222	-2495	319.5	16	98
908	S221	-2511	202.5	16	98
909	S220	-2527	319.5	16	98
910	S219	-2543	202.5	16	98
911	S218	-2559	319.5	16	98
912	S217	-2575	202.5	16	98
913	S216	-2591	319.5	16	98
914	S215	-2607	202.5	16	98
915	S214	-2623	319.5	16	98
916	S213	-2639	202.5	16	98
917	S212	-2655	319.5	16	98
918	S211	-2671	202.5	16	98
919	S210	-2687	319.5	16	98
920	S209	-2703	202.5	16	98
921	S208	-2719	319.5	16	98
922	S207	-2735	202.5	16	98
923	S206	-2751	319.5	16	98
924	S205	-2767	202.5	16	98
925	S204	-2783	319.5	16	98
926	S203	-2799	202.5	16	98
927	S202	-2815	319.5	16	98
928	S201	-2831	202.5	16	98
929	S200	-2847	319.5	16	98
930	S199	-2863	202.5	16	98
931	S198	-2879	319.5	16	98
932	S197	-2895	202.5	16	98
933	S196	-2911	319.5	16	98
934	S195	-2927	202.5	16	98
935	S194	-2943	319.5	16	98
936	S193	-2959	202.5	16	98
937	S192	-2975	319.5	16	98
938	S191	-2991	202.5	16	98
939	S190	-3007	319.5	16	98
940	S189	-3023	202.5	16	98
941	S188	-3039	319.5	16	98
942	S187	-3055	202.5	16	98
943	S186	-3071	319.5	16	98
944	S185	-3087	202.5	16	98
945	S184	-3103	319.5	16	98
946	S183	-3119	202.5	16	98
947	S182	-3135	319.5	16	98
948	S181	-3151	202.5	16	98
949	S180	-3167	319.5	16	98
950	S179	-3183	202.5	16	98
951	S178	-3199	319.5	16	98
952	S177	-3215	202.5	16	98
953	S176	-3231	319.5	16	98
954	S175	-3247	202.5	16	98
955	S174	-3263	319.5	16	98
956	S173	-3279	202.5	16	98
957	S172	-3295	319.5	16	98
958	S171	-3311	202.5	16	98
959	S170	-3327	319.5	16	98
960	S169	-3343	202.5	16	98
961	S168	-3359	319.5	16	98
962	S167	-3375	202.5	16	98
963	S166	-3391	319.5	16	98
964	S165	-3407	202.5	16	98
965	S164	-3423	319.5	16	98
966	S163	-3439	202.5	16	98
967	S162	-3455	319.5	16	98
968	S161	-3471	202.5	16	98
969	S160	-3487	319.5	16	98
970	S159	-3503	202.5	16	98
971	S158	-3519	319.5	16	98
972	S157	-3535	202.5	16	98
973	S156	-3551	319.5	16	98
974	S155	-3567	202.5	16	98
975	S154	-3583	319.5	16	98
976	S153	-3599	202.5	16	98
977	S152	-3615	319.5	16	98
978	S151	-3631	202.5	16	98
979	S150	-3647	319.5	16	98
980	S149	-3663	202.5	16	98
981	S148	-3679	319.5	16	98
982	S147	-3695	202.5	16	98
983	S146	-3711	319.5	16	98
984	S145	-3727	202.5	16	98
985	S144	-3743	319.5	16	98
986	S143	-3759	202.5	16	98
987	S142	-3775	319.5	16	98

#	Pad	X	Y	W	H
988	S141	-3791	202.5	16	98
989	S140	-3807	319.5	16	98
990	S139	-3823	202.5	16	98
991	S138	-3839	319.5	16	98
992	S137	-3855	202.5	16	98
993	S136	-3871	319.5	16	98
994	S135	-3887	202.5	16	98
995	S134	-3903	319.5	16	98
996	S133	-3919	202.5	16	98
997	S132	-3935	319.5	16	98
998	S131	-3951	202.5	16	98
999	S130	-3967	319.5	16	98
1000	S129	-3983	202.5	16	98
1001	S128	-3999	319.5	16	98
1002	S127	-4015	202.5	16	98
1003	S126	-4031	319.5	16	98
1004	S125	-4047	202.5	16	98
1005	S124	-4063	319.5	16	98
1006	S123	-4079	202.5	16	98
1007	S122	-4095	319.5	16	98
1008	S121	-4111	202.5	16	98
1009	S120	-4127	319.5	16	98
1010	S119	-4143	202.5	16	98
1011	S118	-4159	319.5	16	98
1012	S117	-4175	202.5	16	98
1013	S116	-4191	319.5	16	98
1014	S115	-4207	202.5	16	98
1015	S114	-4223	319.5	16	98
1016	S113	-4239	202.5	16	98
1017	S112	-4255	319.5	16	98
1018	S111	-4271	202.5	16	98
1019	S110	-4287	319.5	16	98
1020	S109	-4303	202.5	16	98
1021	S108	-4319	319.5	16	98
1022	S107	-4335	202.5	16	98
1023	S106	-4351	319.5	16	98
1024	S105	-4367	202.5	16	98
1025	S104	-4383	319.5	16	98
1026	S103	-4399	202.5	16	98
1027	S102	-4415	319.5	16	98
1028	S101	-4431	202.5	16	98
1029	S100	-4447	319.5	16	98
1030	S99	-4463	202.5	16	98
1031	S98	-4479	319.5	16	98
1032	S97	-4495	202.5	16	98
1033	S96	-4511	319.5	16	98
1034	S95	-4527	202.5	16	98
1035	S94	-4543	319.5	16	98
1036	S93	-4559	202.5	16	98
1037	S92	-4575	319.5	16	98
1038	S91	-4591	202.5	16	98
1039	S90	-4607	319.5	16	98
1040	S89	-4623	202.5	16	98
1041	S88	-4639	319.5	16	98
1042	S87	-4655	202.5	16	98
1043	S86	-4671	319.5	16	98
1044	S85	-4687	202.5	16	98
1045	S84	-4703	319.5	16	98
1046	S83	-4719	202.5	16	98
1047	S82	-4735	319.5	16	98
1048	S81	-4751	202.5	16	98
1049	S80	-4767	319.5	16	98
1050	S79	-4783	202.5	16	98
1051	S78	-4799	319.5	16	98
1052	S77	-4815	202.5	16	98
1053	S76	-4831	319.5	16	98
1054	S75	-4847	202.5	16	98
1055	S74	-4863	319.5	16	98
1056	S73	-4879	202.5	16	98
1057	S72	-4895	319.5	16	98
1058	S71	-4911	202.5	16	98
1059	S70	-4927	319.5	16	98
1060	S69	-4943	202.5	16	98
1061	S68	-4959	319.5	16	98
1062	S67	-4975	202.5	16	98
1063	S66	-4991	319.5	16	98
1064	S65	-5007	202.5	16	98
1065	S64	-5023	319.5	16	98
1066	S63	-5039	202.5	16	98
1067	S62	-5055	319.5	16	98
1068	S61	-5071	202.5	16	98
1069	S60	-5087	319.5	16	98
1070	S59	-5103	202.5	16	98

#	Pad	X	Y	W	H
1071	S58	-5119	319.5	16	98
1072	S57	-5135	202.5	16	98
1073	S56	-5151	319.5	16	98
1074	S55	-5167	202.5	16	98
1075	S54	-5183	319.5	16	98
1076	S53	-5199	202.5	16	98
1077	S52	-5215	319.5	16	98
1078	S51	-5231	202.5	16	98
1079	S50	-5247	319.5	16	98
1080	S49	-5263	202.5	16	98
1081	S48	-5279	319.5	16	98
1082	S47	-5295	202.5	16	98
1083	S46	-5311	319.5	16	98
1084	S45	-5327	202.5	16	98
1085	S44	-5343	319.5	16	98
1086	S43	-5359	202.5	16	98
1087	S42	-5375	319.5	16	98
1088	S41	-5391	202.5	16	98
1089	S40	-5407	319.5	16	98
1090	S39	-5423	202.5	16	98
1091	S38	-5439	319.5	16	98
1092	S37	-5455	202.5	16	98
1093	S36	-5471	319.5	16	98
1094	S35	-5487	202.5	16	98
1095	S34	-5503	319.5	16	98
1096	S33	-5519	202.5	16	98
1097	S32	-5535	319.5	16	98
1098	S31	-5551	202.5	16	98
1099	S30	-5567	319.5	16	98
1100	S29	-5583	202.5	16	98
1101	S28	-5599	319.5	16	98
1102	S27	-5615	202.5	16	98
1103	S26	-5631	319.5	16	98
1104	S25	-5647	202.5	16	98
1105	S24	-5663	319.5	16	98
1106	S23	-5679	202.5	16	98
1107	S22	-5695	319.5	16	98
1108	S21	-5711	202.5	16	98
1109	S20	-5727	319.5	16	98
1110	S19	-5743	202.5	16	98
1111	S18	-5759	319.5	16	98
1112	S17	-5775	202.5	16	98
1113	S16	-5791	319.5	16	98
1114	S15	-5807	202.5	16	98
1115	S14	-5823	319.5	16	98
1116	S13	-5839	202.5	16	98
1117	S12	-5855	319.5	16	98
1118	S11	-5871	202.5	16	98
1119	S10	-5887	319.5	16	98
1120	S9	-5903	202.5	16	98
1121	S8	-5919	319.5	16	98
1122	S7	-5935	202.5	16	98
1123	S6	-5951	319.5	16	98
1124	S5	-5967	202.5	16	98
1125	S4	-5983	319.5	16	98
1126	S3	-5999	202.5	16	98
1127	S2	-6015	319.5	16	98
1128	S1	-6031	202.5	16	98
1129	DUMMY	-6047	319.5	16	98
1130	DUMMY	-6083	319.5	16	98
1131	G1	-6099	202.5	16	98
1132	G3	-6115	319.5	16	98
1133	G5	-6131	202.5	16	98
1134	G7	-6147	319.5	16	98
1135	G9	-6163	202.5	16	98
1136	G11	-6179	319.5	16	98
1137	G13	-6195	202.5	16	98
1138	G15	-6211	319.5	16	98
1139	G17	-6227	202.5	16	98
1140	G19	-6243	319.5	16	98
1141	G21	-6259	202.5	16	98
1142	G23	-6275	319.5	16	98
1143	G25	-6291	202.5	16	98
1144	G27	-6307	319.5	16	98
1145	G29	-6323	202.5	16	98
1146	G31	-6339	319.5	16	98
1147	G33	-6355	202.5	16	98
1148	G35	-6371	319.5	16	98
1149	G37	-6387	202.5	16	98
1150	G39	-6403	319.5	16	98
1151	G41	-6419	202.5	16	98
1152	G43	-6435	319.5	16	98
1153	G45	-6451	202.5	16	98

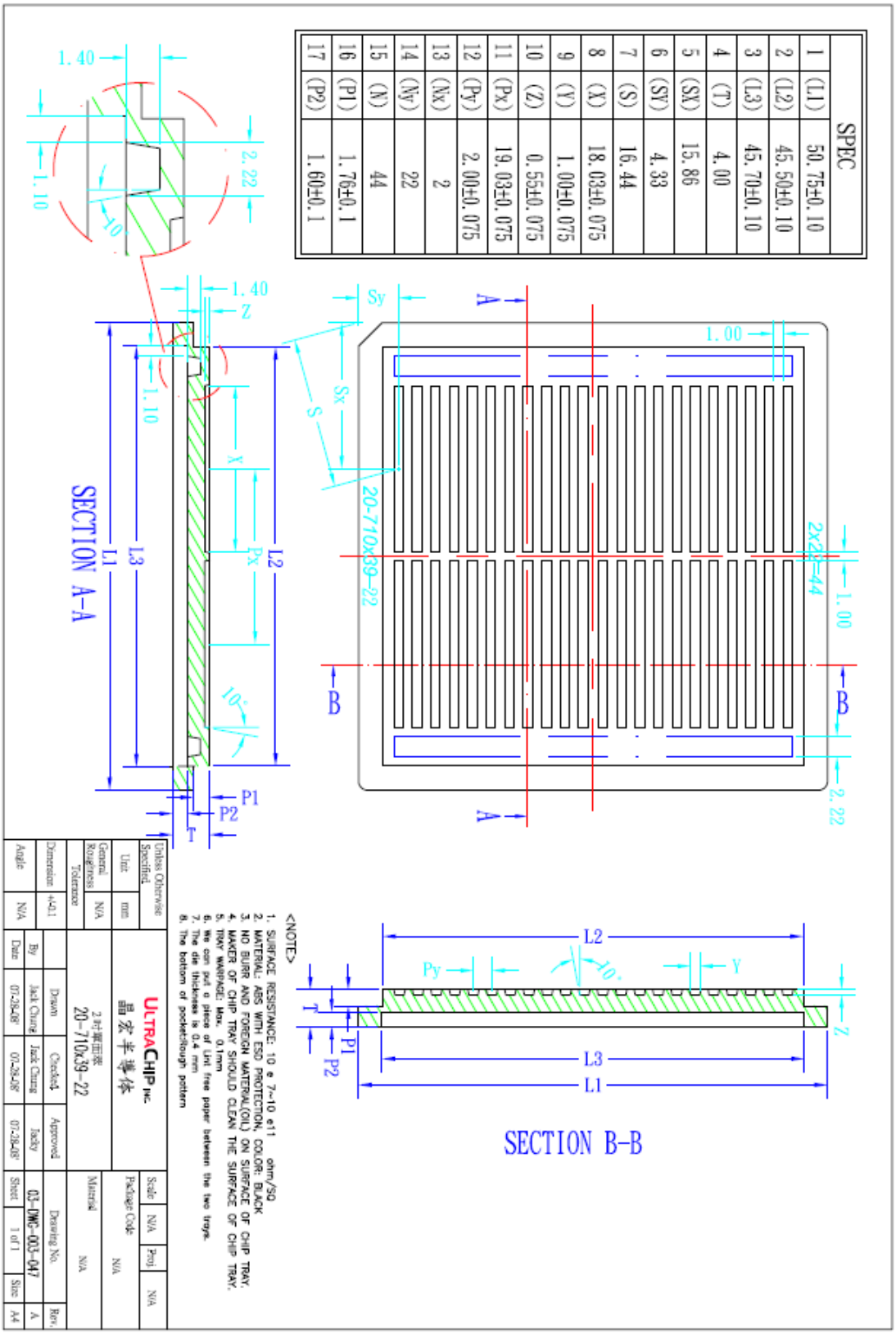
#	Pad	X	Y	W	H
1154	G47	-6467	319.5	16	98
1155	G49	-6483	202.5	16	98
1156	G51	-6499	319.5	16	98
1157	G53	-6515	202.5	16	98
1158	G55	-6531	319.5	16	98
1159	G57	-6547	202.5	16	98
1160	G59	-6563	319.5	16	98
1161	G61	-6579	202.5	16	98
1162	G63	-6595	319.5	16	98
1163	G65	-6611	202.5	16	98
1164	G67	-6627	319.5	16	98
1165	G69	-6643	202.5	16	98
1166	G71	-6659	319.5	16	98
1167	G73	-6675	202.5	16	98
1168	G75	-6691	319.5	16	98
1169	G77	-6707	202.5	16	98
1170	G79	-6723	319.5	16	98
1171	G81	-6739	202.5	16	98
1172	G83	-6755	319.5	16	98
1173	G85	-6771	202.5	16	98
1174	G87	-6787	319.5	16	98
1175	G89	-6803	202.5	16	98
1176	G91	-6819	319.5	16	98
1177	G93	-6835	202.5	16	98
1178	G95	-6851	319.5	16	98
1179	G97	-6867	202.5	16	98
1180	G99	-6883	319.5	16	98
1181	G101	-6899	202.5	16	98
1182	G103	-6915	319.5	16	98
1183	G105	-6931	202.5	16	98
1184	G107	-6947	319.5	16	98
1185	G109	-6963	202.5	16	98
1186	G111	-6979	319.5	16	98
1187	G113	-6995	202.5	16	98
1188	G115	-7011	319.5	16	98
1189	G117	-7027	202.5	16	98
1190	G119	-7043	319.5	16	98
1191	G121	-7059	202.5	16	98
1192	G123	-7075	319.5	16	98
1193	G125	-7091	202.5	16	98
1194	G127	-7107	319.5	16	98
1195	G129	-7123	202.5	16	98
1196	G131	-7139	319.5	16	98
1197	G133	-7155	202.5	16	98
1198	G135	-7171	319.5	16	98
1199	G137	-7187	202.5	16	98
1200	G139	-7203	319.5	16	98
1201	G141	-7219	202.5	16	98
1202	G143	-7235	319.5	16	98
1203	G145	-7251	202.5	16	98
1204	G147	-7267	319.5	16	98
1205	G149	-7283	202.5	16	98
1206	G151	-7299	319.5	16	98
1207	G153	-7315	202.5	16	98
1208	G155	-7331	319.5	16	98
1209	G157	-7347	202.5	16	98
1210	G159	-7363	319.5	16	98
1211	G161	-7379	202.5	16	98
1212	G163	-7395	319.5	16	98
1213	G165	-7411	202.5	16	98
1214	G167	-7427	319.5	16	98
1215	G169	-7443	202.5	16	98
1216	G171	-7459	319.5	16	98
1217	G173	-7475	202.5	16	98
1218	G175	-7491	319.5	16	98
1219	G177	-7507	202.5	16	98
1220	G179	-7523	319.5	16	98
1221	G181	-7539	202.5	16	98
1222	G183	-7555	319.5	16	98
1223	G185	-7571	202.5	16	98
1224	G187	-7587	319.5	16	98
1225	G189	-7603	202.5	16	98
1226	G191	-7619	319.5	16	98
1227	G193	-7635	202.5	16	98
1228	G195	-7651	319.5	16	98
1229	G197	-7667	202.5	16	98
1230	G199	-7683	319.5	16	98
1231	G201	-7699	202.5	16	98
1232	G203	-7715	319.5	16	98
1233	G205	-7731	202.5	16	98
1234	G207	-7747	319.5	16	98
1235	G209	-7763	202.5	16	98
1236	G211	-7779	319.5	16	98

#	Pad	X	Y	W	H
1237	G213	-7795	202.5	16	98
1238	G215	-7811	319.5	16	98
1239	G217	-7827	202.5	16	98
1240	G219	-7843	319.5	16	98
1241	G221	-7859	202.5	16	98
1242	G223	-7875	319.5	16	98
1243	G225	-7891	202.5	16	98
1244	G227	-7907	319.5	16	98
1245	G229	-7923	202.5	16	98
1246	G231	-7939	319.5	16	98
1247	G233	-7955	202.5	16	98
1248	G235	-7971	319.5	16	98
1249	G237	-7987	202.5	16	98
1250	G239	-8003	319.5	16	98
1251	G241	-8019	202.5	16	98
1252	G243	-8035	319.5	16	98
1253	G245	-8051	202.5	16	98
1254	G247	-8067	319.5	16	98
1255	G249	-8083	202.5	16	98

#	Pad	X	Y	W	H
1256	G251	-8099	319.5	16	98
1257	G253	-8115	202.5	16	98
1258	G255	-8131	319.5	16	98
1259	G257	-8147	202.5	16	98
1260	G259	-8163	319.5	16	98
1261	G261	-8179	202.5	16	98
1262	G263	-8195	319.5	16	98
1263	G265	-8211	202.5	16	98
1264	G267	-8227	319.5	16	98
1265	G269	-8243	202.5	16	98
1266	G271	-8259	319.5	16	98
1267	G273	-8275	202.5	16	98
1268	G275	-8291	319.5	16	98
1269	G277	-8307	202.5	16	98
1270	G279	-8323	319.5	16	98
1271	G281	-8339	202.5	16	98
1272	G283	-8355	319.5	16	98
1273	G285	-8371	202.5	16	98
1274	G287	-8387	319.5	16	98

#	Pad	X	Y	W	H
1275	G289	-8403	202.5	16	98
1276	G291	-8419	319.5	16	98
1277	G293	-8435	202.5	16	98
1278	G295	-8451	319.5	16	98
1279	G297	-8467	202.5	16	98
1280	G299	-8483	319.5	16	98
1281	G301	-8499	202.5	16	98
1282	G303	-8515	319.5	16	98
1283	G305	-8531	202.5	16	98
1284	G307	-8547	319.5	16	98
1285	G309	-8563	202.5	16	98
1286	G311	-8579	319.5	16	98
1287	G313	-8595	202.5	16	98
1288	G315	-8611	319.5	16	98
1289	G317	-8627	202.5	16	98
1290	G319	-8643	319.5	16	98
1291	DUMMY	-8659	202.5	16	98

TRAY INFORMATION



REVISION HISTORY

Revision	Contents	Date
0.6	First release	Apr. 9, '09
0.8	(1) Reference voltage for interface pin input, I/OVCC, is adjusted. 1.8~3.3V → 1.65~3.3V (Section "Feature Highlights", page 4)	Jun. 30, '09
	(2) The table for register VC[2:0] is extended with a column for VsN. (Section "Command Description" – (16) Power Control 1~4, page 30)	
	Legacy content of 6800 mode are removed: (3) Settings "0000" and "1000" of IM[3:0] are removed. (Section "Pin Description", page 7) (4) The main table and the content are updated accordingly. (Section "Host Interface", Pp 51-54) (5) The drawings are removed. (Section "Host Interface Reference Circuit", page 59~60)	
	(6) VDD is renamed as VD1. VDD3 is renamed as IOVcc. VDD4 is renamed as VD4. (overall)	
	(7) The "Reference Adjustment" table is corrected. (Section "Variable resistor", page 69)	
	(8) The Gamma Curve chart is corrected. (Section "Gamma Voltage Formula", page 72)	
	(9) VsN (Min.) : –2.3 → –2.75 V V_{IL} (Max.) : 0.2 IOVcc → 0.15 IOVcc V V_{IH} (Min.) : 0.8 IOVcc → 0.85 IOVcc V (10) Besides Hi-V (IOVcc=2.5V~3.3V), one more pair of V_{IL} / V_{IH} is added for Low-V (IOVcc=1.65V~2.5V): V_{IL} (Max.) : 0 x IOVcc V V_{IH} (Min.) : 1 x IOVcc V (Section "Specifications" – DC Characteristics, page 79)	
	(11) Power consumption data present. (Section "Specifications" – Power Consumption, page 79)	
	(12) AC timings present. (Section "AC Characteristics", page 80~83)	