CSE 460

VLSI DESIGN

Lab Assignment 6

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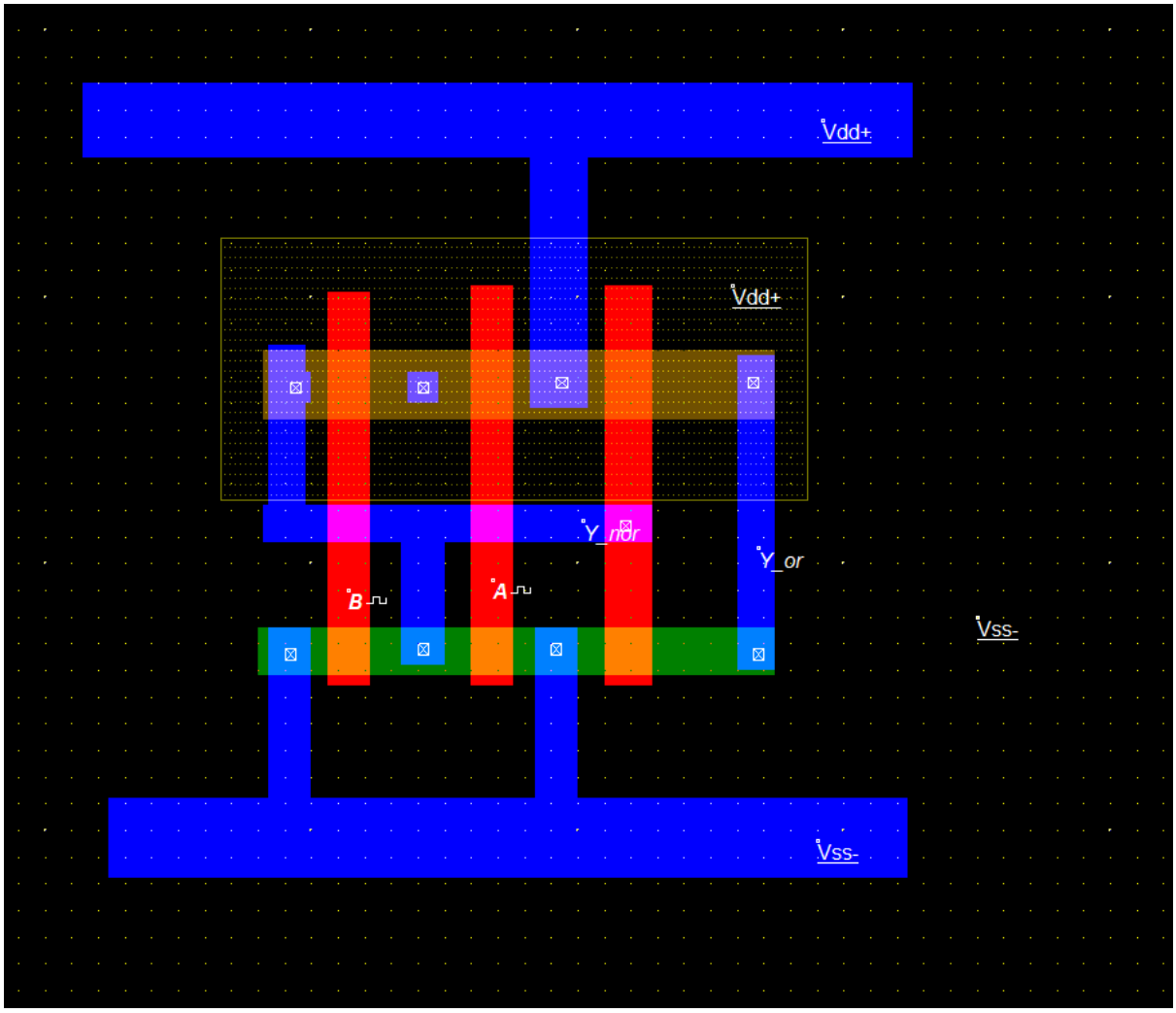
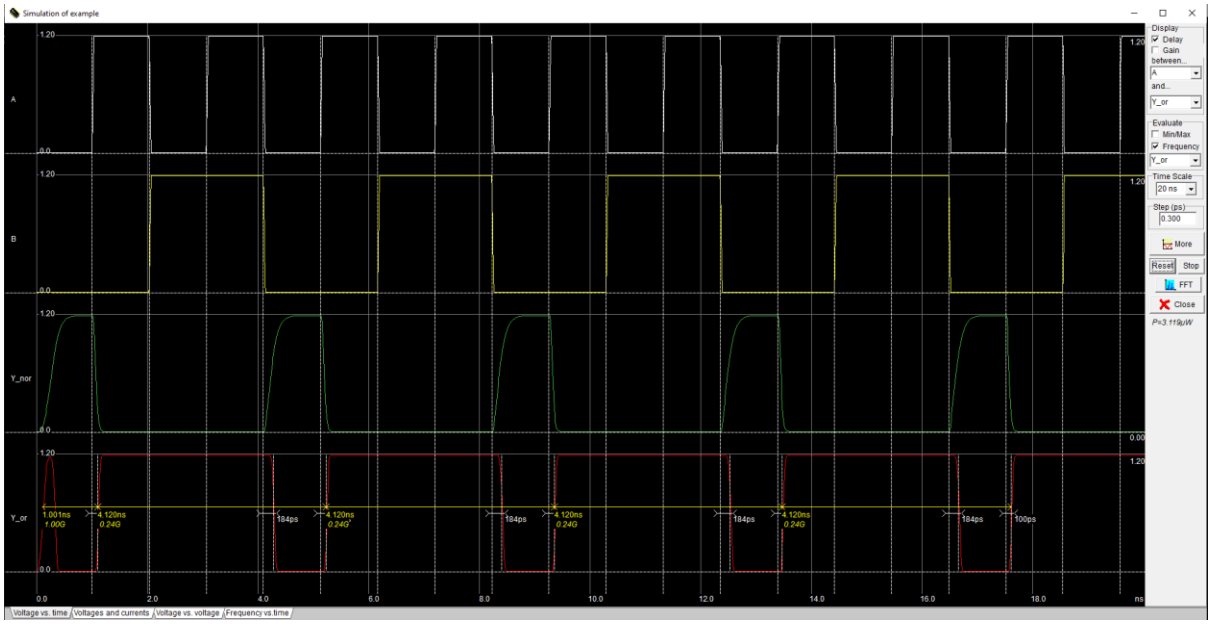
Sec: 09

Problem 1: 2 input OR gate (Design the NOR gate followed by the inverter to create the OR gate)

Layout:



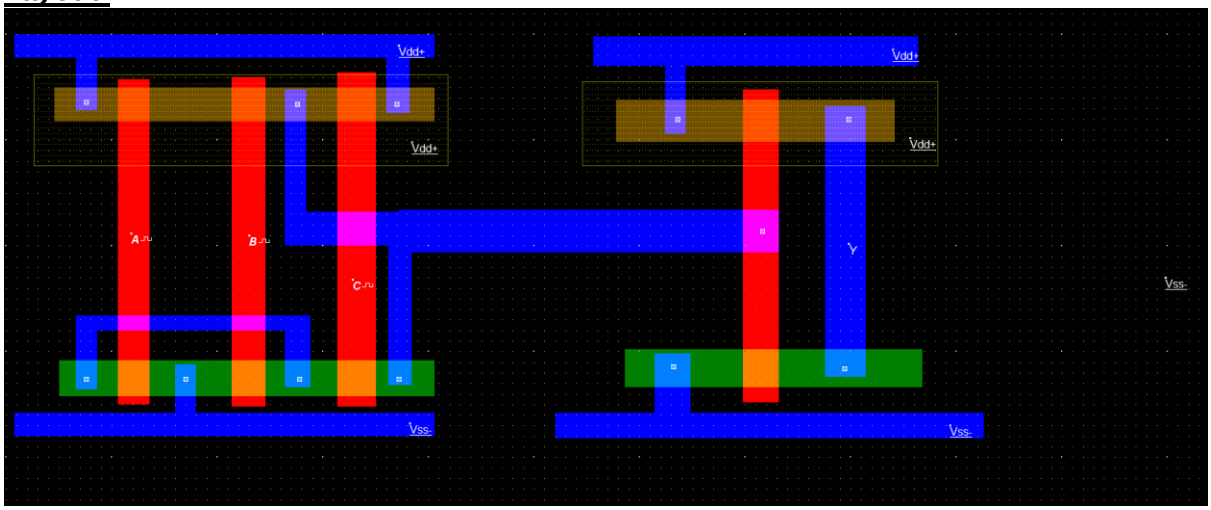
Timing Diagram:



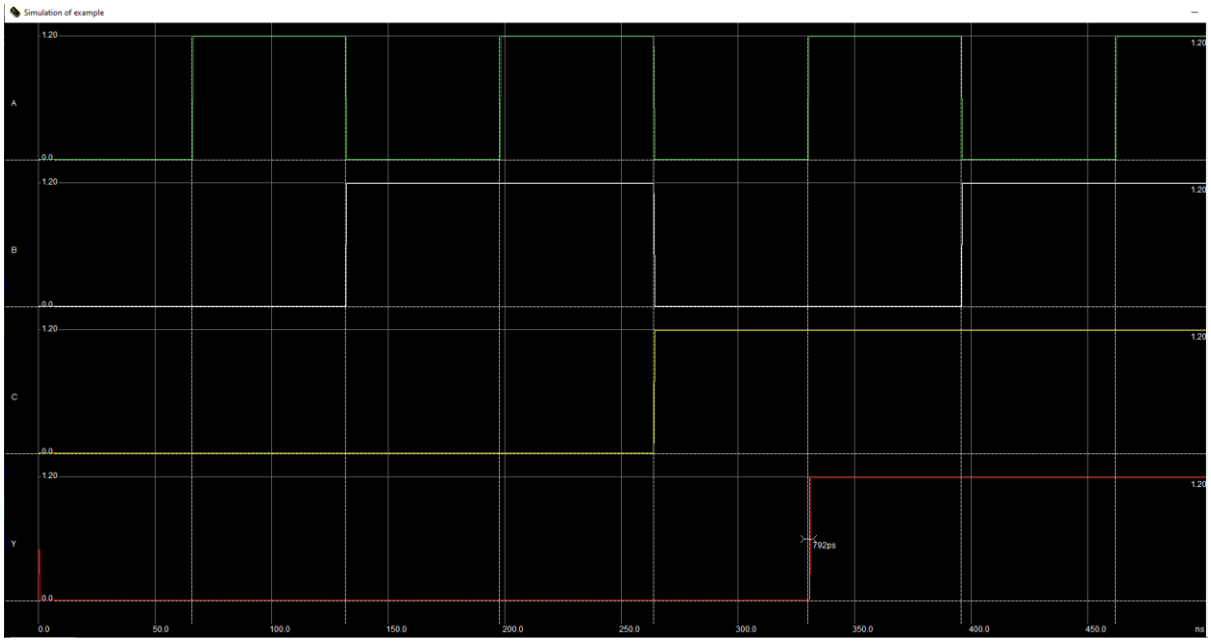
Explanation: In this experiment, we use microwind to implement the CMOS OR Gate. Designing the NOR gate followed by the inverter to create the OR gate. There are two input functions. If we look at the timing diagram we can see that when the A ,B input is low the output is low and when the A,B input is low,low or high,low or low,high the output is high. If we manually calculate the truth table of the given function it will also be the same.

Problem 2: Y= (A+B)C.

Layout:



Timing Diagram:



Explanation:

In this experiment, we use microwind to implement th F=(A+B) C.

There are three input functions. If we look at the timing diagram we can see that when the A ,B,C input is low,high,high the output is high again the input is high,low,high and all inputs are high then the output is high. All other input combination causes output low. If we manually calculate the truth table of the given
function it will also be the same.