CSE 460

VLSI DESIGN

Lab Assignment 3

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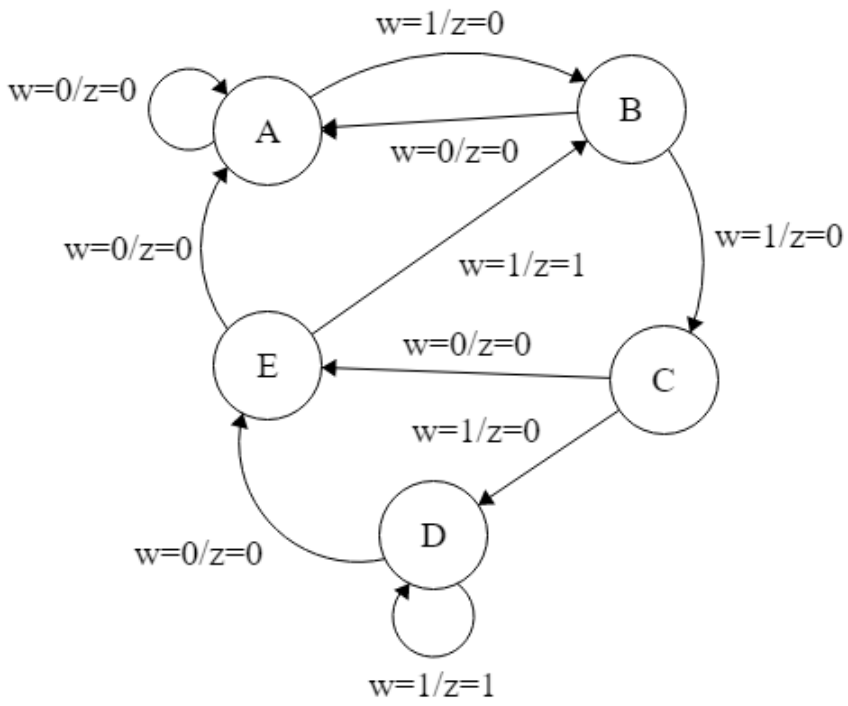
Problem statement:

Derive the state diagram for an FSM with an input w and an output z. The machine has to generate z = 1 when the four consecutive values of w are **1101 or 1111**; otherwise, z = 0. Overlapping input patterns are allowed. An example of the desired behavior is (attached photo)

2) Which type of FSM should be used?

Ans: Here, Mealy type FSM should be used.

State diagram:



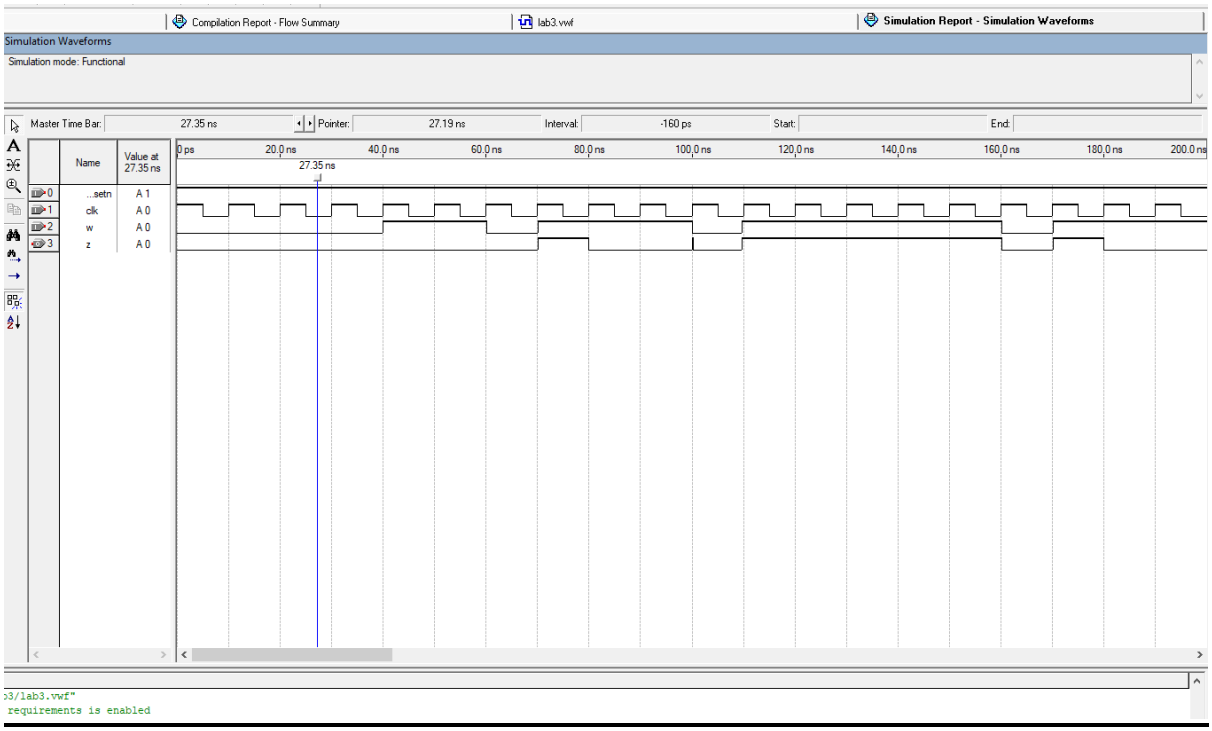
Code:

module lab3(z,w,clk,Resetn);

```
input clk, Resetn, w;
output reg z;
reg [3:1]y, Y;
parameter A=3'b000, B=3'b001, C=3'b010, D=3'b011, E=3'b100;
always @(w,y)
begin
case(y)
A: if (w)
begin
z=0;
Y=B;
end
else
begin
z=0;
Y=A;
end
B: if (w)
begin
z=0;
Y=C;
end
else
begin
z=0;
Y=A;
end
C: if (w)
begin
z=0;
Y=D;
end
```

```
else
begin
z=0;
Y=E;
end
D: if (w)
begin
z=1;
Y=D;
end
else
begin
z=0;
Y=E;
end
E: if (w)
begin
z=1;
Y=B;
end
else
begin
z=0;
Y=A;
end
endcase
end
always@(posedge clk, negedge Resetn)
if (Resetn == 0) y<=A;
else
y<=Y;
endmodule
```

Simulation Report:



Explanation: In this study, we apply Mealy-type FSM. The state and the current principal inputs determine the outputs in Mealy-type FSM. When the sequence is 1111 or 1101, the output is high(1) or z = 1, and when it is not, the output is low(0) or z= 0, as can be seen by looking at the output z. The output sequence is 000000110100010011 from the input sequence 010111110111011111. We can observe the same output for the given input if we look at the timing diagram. In timing diagram when 4 consecutive clock cycles w is 1 then the output z = 1 and when w = 1101 the the output z = 1 . Otherwise, the output z remains 0 in the timing diagram.