

L-1

Ch-9 : 8086/8088 Hardware Specifications:

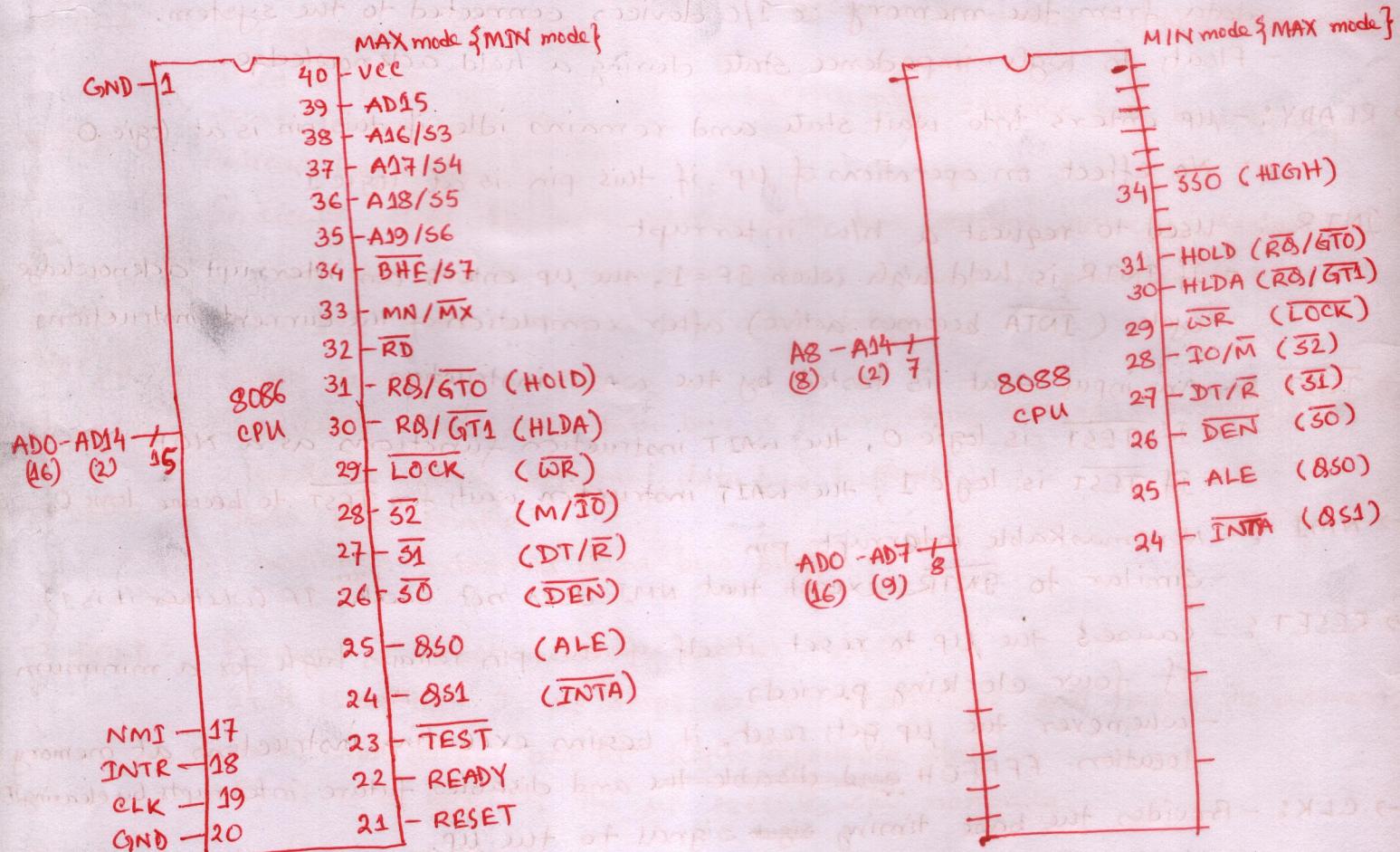
- Virtually no difference between these two chips; both are packaged in 40-pin dual in-line packages (DIPs)
- 8086: 16 bit chip with a 16-bit data bus (AD0 - AD15) 8088: 16 bit chip with an 8-bit data bus (AD0 - AD7) } Major difference
- 8086: M/IO ; 8088: IO/M } Minor difference
Pin 34 \Rightarrow 8086: BHE/57 ; 8088: SS0
- Power Supply Requirements:

Both: +5.0 V with a supply voltage tolerance of $\pm 10\%$.

Both: 32°F to 180°F

8086: 360 mA ; 8088: 340 mA (max supply current)

CMOS version \Rightarrow 80C86 and 80C88 : 10 mA and -40°F to 225°F



\Rightarrow Pin Connections!

- AD7 - AD0: - 8088 address / data bus lines
 - multiplexed address data bus; and - rightmost eight bits of the memory address or I/O port number whenever ALE is active (Logic 1) or data whenever ALE is inactive (Logic 0).
 - high-impedance state during a hold acknowledge
- A15 - AB: - 8088 address bus (upper half memory address bits)
 - high-impedance state during a hold acknowledge

- AD15-AD8 : - 8086 address/data bus lines
 - Contains address bits A15-A8, when ALE is logic 1
 - Enter in high-impedance state whenever a hold acknowledge occurs
- A19/56 - A16/53 : - Multiplexed address/status bus
 - Enter in high-impedance during hold acknowledge
- S6 : Always 0
- S5 : Indicates the condition of IF flag
- S4, S3 : ~~Indicate~~ Indicate segment accessed during current bus cycle
 - 0 0 → Extra segment
 - 0 1 → Stack segment
 - 1 0 → Code or no segment
 - 1 1 → Data segment
- RD : - Whenever this pin goes to logic 0, the data bus becomes receptive to data from the memory or I/O devices connected to the system.
 - Floats to high-impedance state during a hold acknowledge.
- READY : - MP enters into wait state and remains idle if this pin is at logic 0
 - No effect on operations of MP, if this pin is at logic 1
- INTR : - Used to request a h/w interrupt
 - If INTR is held high when IF=1, the MP enters an interrupt acknowledge cycle (INTA becomes active) after completion of the current instructions
- TEST : - An input that is tested by the WAIT instruction
 - If TEST is logic 0, the WAIT instruction functions as a NOP
 - If TEST is logic 1, the WAIT instruction waits for TEST to become logic 0.
- NMI : - Non maskable interrupt pin
 - Similar to INTR except that NMI does not check IF (whether it is 1)
- RESET : - Causes the MP to reset itself if this pin remains high for a minimum of four clocking periods.
 - Whenever the MP gets reset, it begins executing instructions at memory location FFFF0H ~~and disable the~~ and disables future interrupts by clearing
- CLK : - Provides the base timing ~~signal~~ signal to the MP.
 - Clock signal must have at least 33% duty cycle (or they high for one-third of the clocking period and low for two-third of the period)
- VCC : - Power supply input
 - Provides +5.0 Volt with 10% tolerance to the MP.

GND : - 2 pins, both must be connected to ground

→ MN/ \overline{M} : - Selects either minimum mode or maximum mode operation of MP

→ $\overline{BHE/S7}$: - Bus High Enable

- Used in 8086 to enable the most significant data bus bits (D15-D8) during a read or write operation
- The state of S7 is always a logic 1.

Minimum Mode Pins

→ $\overline{IO/M}$ or M/\overline{IO} : - Selects memory or I/O

- Indicates that MP's address bus contains either a memory address or an I/O port address.
- High impedance state during a hold acknowledge

→ \overline{WR} : - Indicates that the MP is outputting data to a memory or I/O device

→ \overline{INTA} : - A response to the INTR input pin

- Used to gate the interrupt vector number onto the data bus in response to an interrupt request

→ \overline{ALE} : - Address Latch Enable

- Indicates that the MP's address/data bus contains address information
- The address can be a memory address or an I/O port number
- Does NOT float during a hold acknowledge

→ DT/R : - Data Transmit or Receive

- Indicates that MP's data bus is transmitting ($DT/R=1$) or receiving ($DT/R=0$) data
- Used to enable external data bus buffers

→ DEN : - Data Bus Enable

- Activates external data bus buffers

→ HOLD : - Requests a direct memory access (DMA)

- If it is a logic 1, MP stops executing software and places its address, data, and control bus at high-impedance state.
- If it is a logic 0, the MP executes SW normally.

→ HLDA : - Hold Acknowledge

- Indicates that the MP has entered the hold state

→ $\overline{SS0}$: - Equivalent to the S0 pin in the maximum mode operation of the MP

- It is combined with $\overline{IO/M}$ and DT/R to decode the function of current bus cycle.

IO/M	DT/R	$\overline{SS0}$	Function	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Function
0	0	0	Interrupt acknowledge	0	0	0	Interrupt acknowledge
0	0	1	Memory read	0	0	1	I/O read
0	1	0	Memory write	0	1	0	I/O write
0	1	1	Halt	0	1	1	Halt
1	0	0	Opcode fetch	1	0	0	Opcode fetch
1	0	1	I/O read	1	0	1	Memory read
1	1	0	I/O write	1	1	0	Memory write
1	1	1	Passive/Inactive	1	1	1	Passive

Table: Bus cycle status (8088) [Minimum mode]

Table: Bus control functions generated by the bus controller 8288 [Maximum mode]

→ S_2 , S_1 , and S_0 : - Indicate the \$ function of current bus cycle
- Normally decoded by 8288 bus controller

→ $\overline{RQ}/\overline{GT}$ and $\overline{RO}/\overline{GTO}$: - Request/grant pins

- Requests direct memory access (DMA)

- Bi-directional lines

- Used to both request and grant a DMA operation

→ $LOCK$: - Used to lock peripherals off the system.

→ BSI and BSS : - Queue status bits

- Show status of the internal instruction queue.

- Accessed by numeric coprocessor (8087).

<u>BSI</u>	<u>BSS</u>	<u>Function</u>
0	0	Queue is idle
0	1	First byte of opcode
1	0	Queue is empty
1	1	Subsequent byte of opcode

Clock Generator (8284A)

⇒ Basic functions: - clock generation

- RESET synchronization

- READY synchronization

- TTL-level peripheral clock signal

⇒ Pin functions:

→ AEN_1 and AEN_2 : - Qualify the bus ready signals, RDY₁ and RDY₂ respectively

(Address enable) - Wait states are generated by the READY pin of MP, which is controlled by AEN_1 and AEN_2 pins

→ RDY₁ and RDY₂: - Bus ready inputs

- Cause wait states in conjunction with AEN_1 and AEN_2 pins

→ ASYNC: - Ready synchronization

- Selects either one or two stages of synchronization for RDY₁ and RDY₂ inputs.

→ READY: - An output pin that connects to the MP's READY input

- Synchronized with RDY₁ and RDY₂ inputs.

→ X₁ and X₂: - Crystal oscillator pins

- Connect to an external crystal, which is used as the timing source for the clock generator and all its functions.

→ F/C: - Frequency/crystal select input

- Chooses the clocking source

- If it is held high, an external clock is provided to the EFI pin

- If it is held low, the internal crystal oscillator provides the timing signal

→ EFI: - External frequency input

- Supplies timing whenever the F/C pin is high

→ CLK: - Clock output pin, which provides CLK input to MP and other components

- Output signal is one-third of the crystal or EFI input freq., and has a 33% duty cycle (freq by 8086/8088)

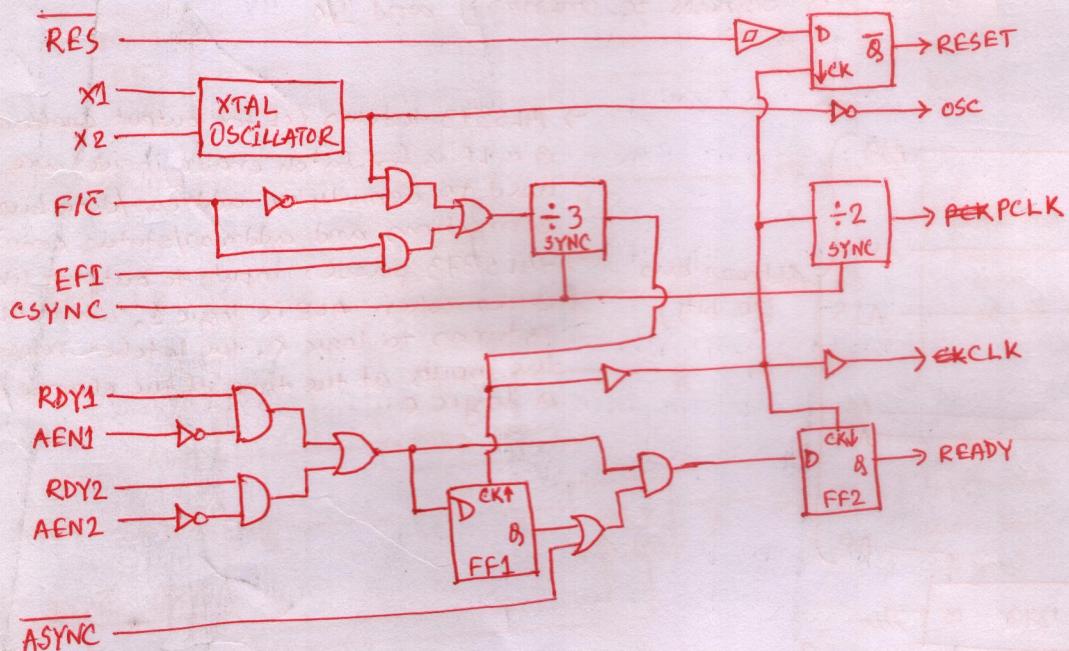
→ PCLK: - Peripheral clock

- One sixth of the crystal or EFI input frequency, and has a 50% duty cycle



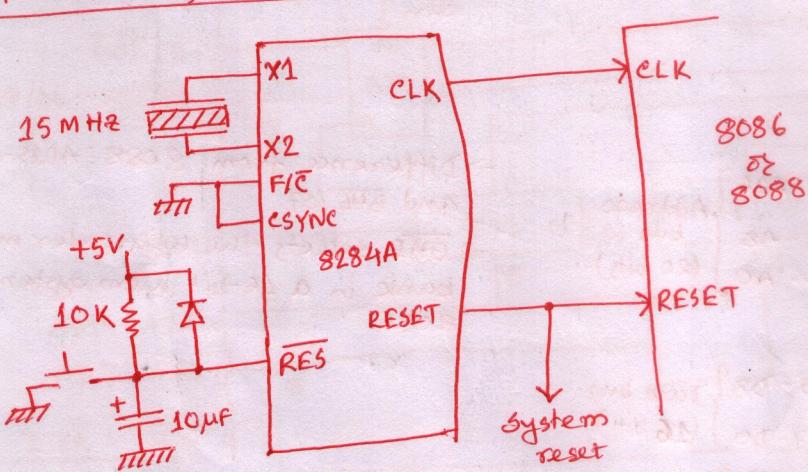
- OSC: - Oscillator output
 - At same freq as the crystal or ESI input
 - Provides an ESI input to other 8284A in multiprocessor systems
- $\rightarrow \overline{\text{RES}}$: - Reset input
 - Often connected to an RC network that provides power-on resetting
- $\rightarrow \text{RESET}$: - Reset output
 - Connected to μP's RESET input pin
- $\rightarrow \text{CSYNC}$: - Clock synchronization
 - Used whenever the ESI input provides synchronization in multi-processor systems
 - If the internal oscillator is used, this pin must be grounded.

Internal Block Diagram of 8284A Clock Generator



- \rightarrow If a crystal is attached to X1 and X2, the oscillator generates a square-wave signal
- \rightarrow CLK = freq / 3 ; PCLK = freq / 16

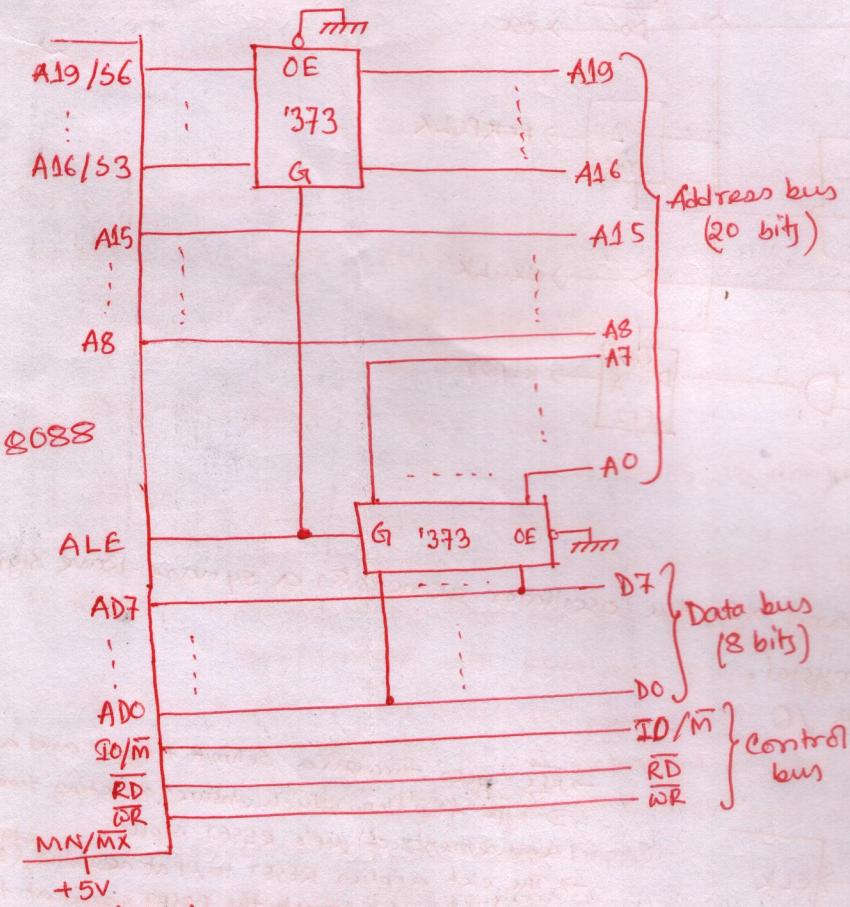
Operation of the RESET section



- $\rightarrow \overline{\text{RES}}$ goes through a Schmitt trigger and a D-type flip flop, which ensures meeting timing requirements of μP's RESET input
- \rightarrow The ckt applies RESET to μP at negative edge ($1 \rightarrow 0$), and the μP samples the RESET signal at the positive edge ($0 \rightarrow 1$)
- \rightarrow When power is first applied to the system, the RC ckt provides a logic 0 to $\overline{\text{RES}}$
- \rightarrow After a short time, $\overline{\text{RES}}$ becomes logic 1, as the capacitor charges to +5V through the resistor.
- \rightarrow A push button allows the μP to be reset by an operator
- \rightarrow Correct reset timing requires the RESET input to become a logic 1 no later than 4 clock cycles after power is applied, and held high for at least 50 μs
- \rightarrow RESET goes high in 4 clocks; by the flip flop, RESET stays high for 50 μs; by RC time constant

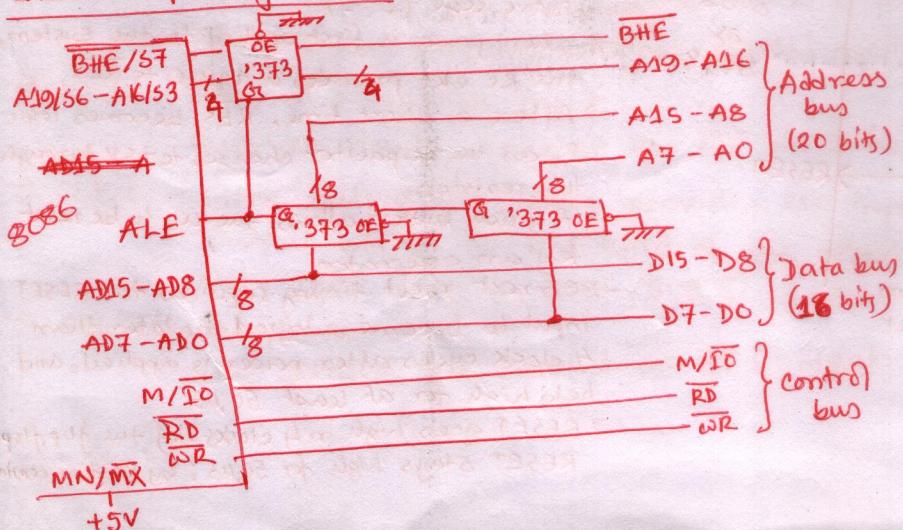
- The address/data bus on the MP is multiplexed (shared) to reduce the # of pins, which, on the other hand, burdens with the task of extracting or demultiplexing info from these pins.
- Why not leave the buses not multiplexed?
 - ⇒ Memory and I/O require that the address remains valid and stable throughout a read or write cycle. If the buses are multiplexed, the address can get changed causing read or write in ~~a~~ wrong locations.
- All computer systems have three types of buses:
 - ① Address bus: Provides memory address or I/O port number
 - ② Data bus: Transfers data between MP and mem/~~mem~~ and I/O.
 - ③ Control bus: Provides control signals to memory and I/O

Demultiplexing 8088:



- 74LS373 latches (OE for output enable and G or LE is for latch enable inside) are used to demultiplex address/data bus connections and address/status conn?
- 74LS373 passes inputs to outputs like wires when ALE is logic 1; when ALE returns to logic 0, the latches remember the inputs at the time of the change to a logic 0

Demultiplexing 8086:

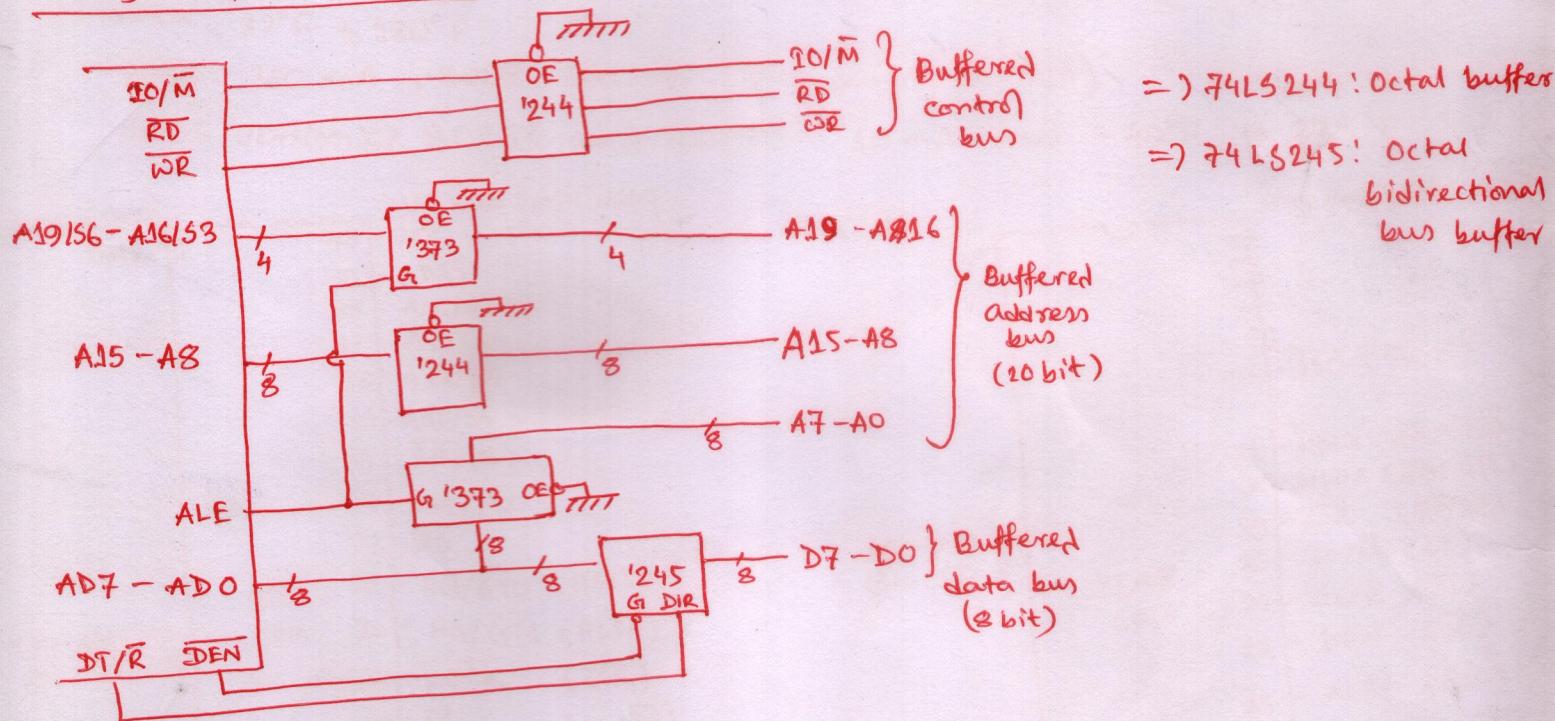


- Difference from 8088: AD15-AD8, and BHE/S7
- BHE selects the high-order memory bank in a 16-bit mem system of 8086

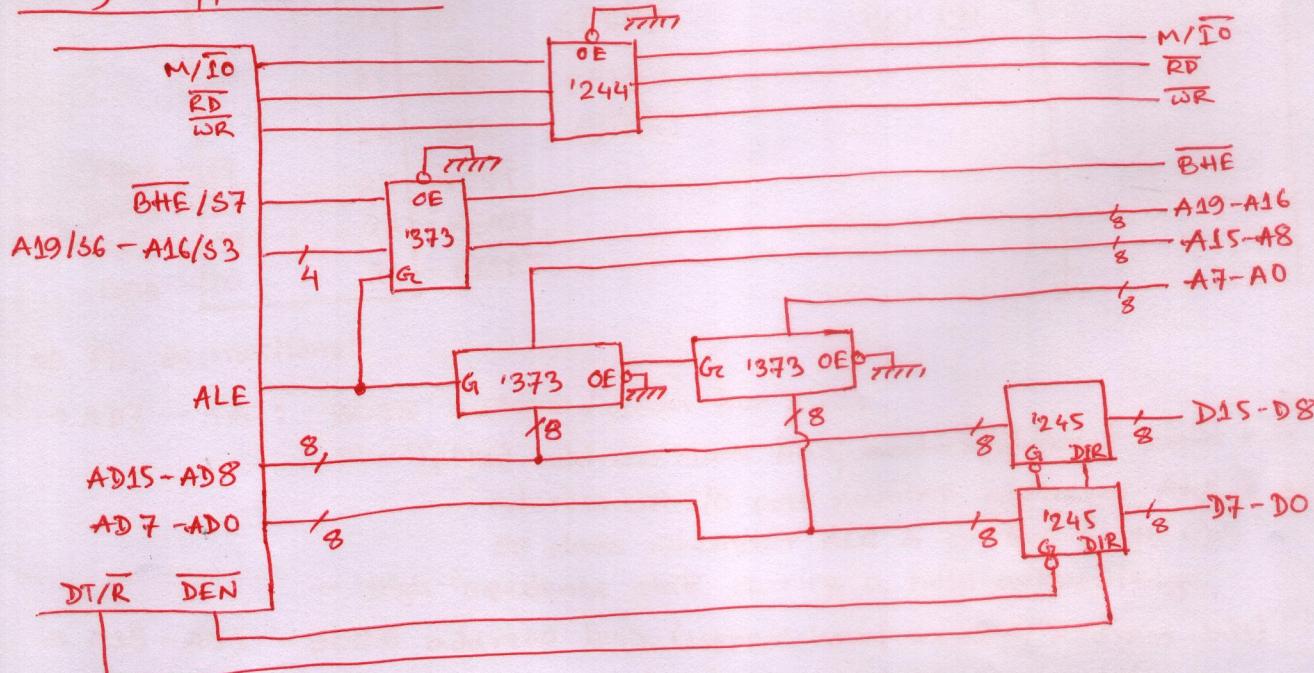
buffered System

- If more than 10 unit loads are attached to any bus pin, the entire μP system must be buffered (Buffer \Rightarrow provides amplification in a digital ckt to drive output loads, enabling more TTL unit loads to be driven).
- The demultiplexed pins are already buffered by the 74LS373 latches.
- A fully buffered signal will introduce a timing delay, which causes no difficulty unless memory or I/O devices are used that function at near the maximum speed of the bus.

Fully Buffered 8088



Fully Buffered 8086



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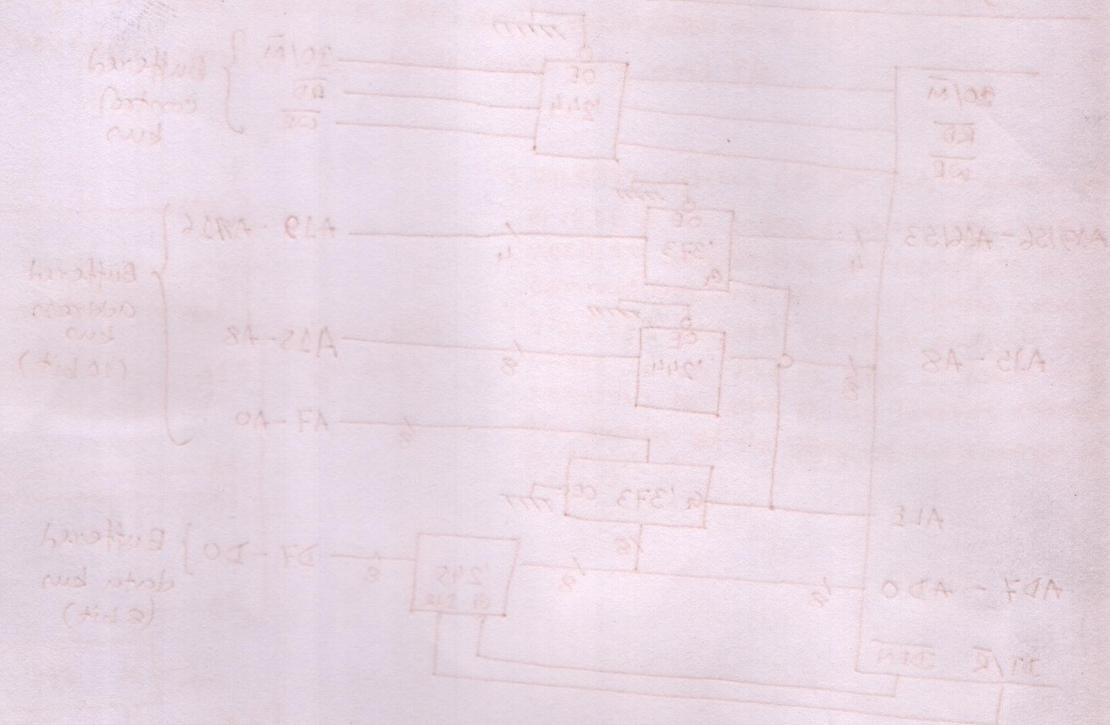
memory buffering

of chips required for fully Buffered MP

μ P	74LS244 (Octal buffer)	74LS245 (Octal bidirectional bus buffer)	74LS273
8088	2	1	2
8086	1	2	3

on various words would probably prefer to use buffered logic buffered multiplexers
in order to minimize total board area cost of program cost of buffers
and with to board minimization

2303 Buffering Unit



2303 Buffering Unit

