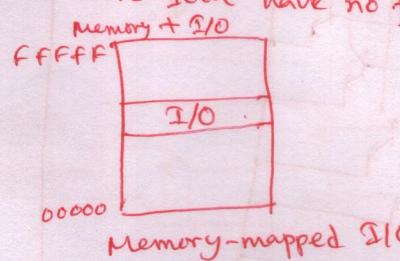
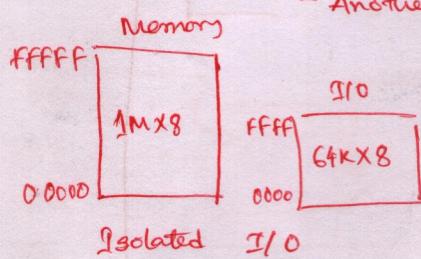


L-3 Basic I/O Interface :

Isolated and Memory-mapped I/O:

- Isolated I/O : - I/O locations are isolated from the memory system in a separate I/O address space
 - Addressed of I/O is called ports, which are separated from memory
 - Adv: User can expand the memory to its full size
 - Disadv: New instructions (IN, OUT, etc.) are needed for data xfer
- Memory-mapped I/O : - Uses any instrucn that xfers data between CPU and mem (adv.)
 - Memory-mapped I/O devices are treated as memory locations within memory map
 - Disadv.: Reduces the amount of memory available to an application
 - Another adv.: IORc and IOWc have no func? reducing ckt required for decoding



Basic Input output Interfaces

I/O Port address Decoding \Rightarrow Similar as memory } Self study

Programmable Peripheral Interface

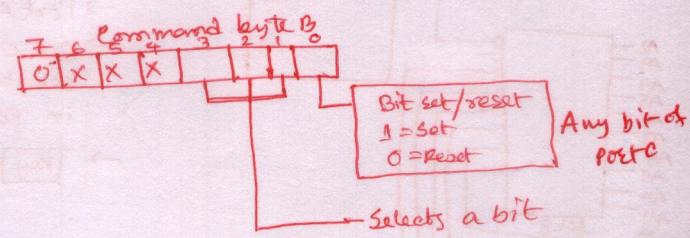
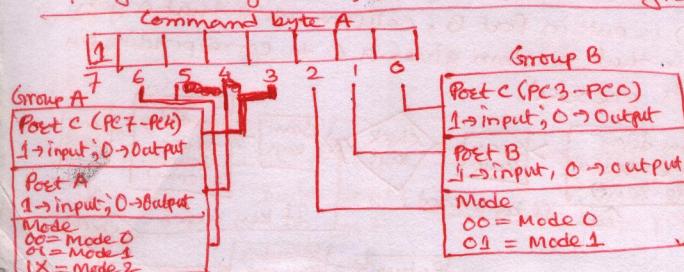
- 82C55 : - Low-cost interfacing component having 24 pins for I/O that are programmable in groups of 12 pins : It operates in three modes of operation .
 - It is compatible with any TTL-compatible I/O device
 - Requires insertion of wait states in case of operating with CPU having more than 8MHz clock.
- Basic description of 82C55 :
 - Has 3 I/O ports (labeled A, B, and C)
 - Programmed as groups (Group A = Port A (PA7-PA0) and the upper half of Port C (PC7-PC4); Group B: Port B (PB7-PB0) and the lower half of Port C (PC3-PC0)).

- Register selection by A1 and A0

A1	A0	Function
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Command Register

- RESET input causes all ports to set up as simple input ports using mode 0 operat. (as set up as input, damage is prevented when the power is first applied)

Programming 82C55: Command Registers



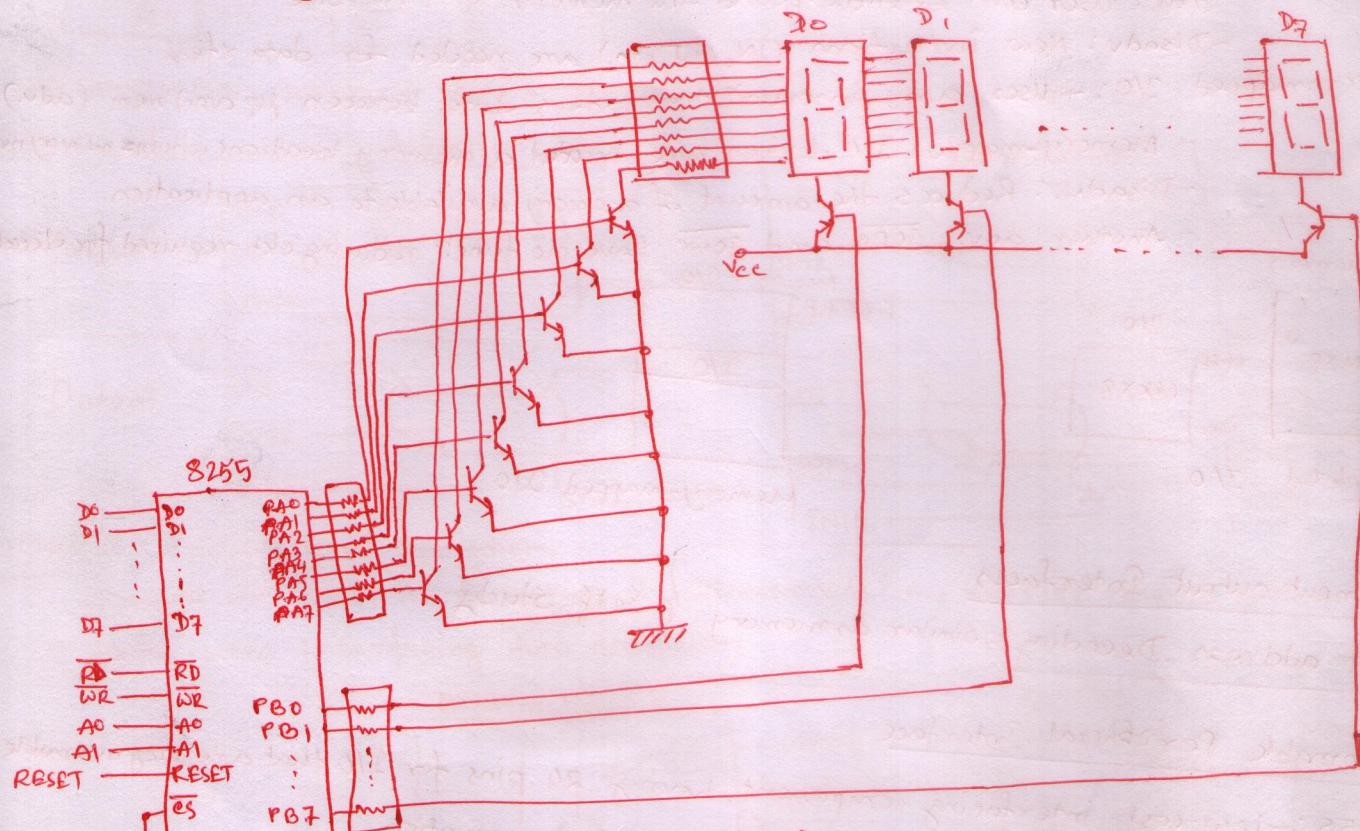
- Gr A \rightarrow 0/1/2 mode
Gr B \rightarrow 0/1 mode

| - mode 0 \rightarrow Simple I/O
mode 1 \rightarrow Strobed I/O
[Double handshaking I/O]
mode 2 \rightarrow Bidirectional H/S I/O

(2)

Mode 0 Operation :

- Functions either as a buffered input device or as a latched output device
 \Rightarrow LED Display:

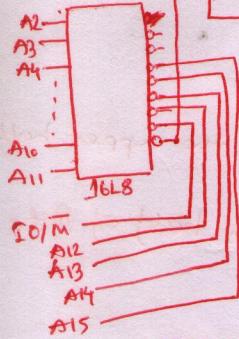


PAL logic (PAL16L8)

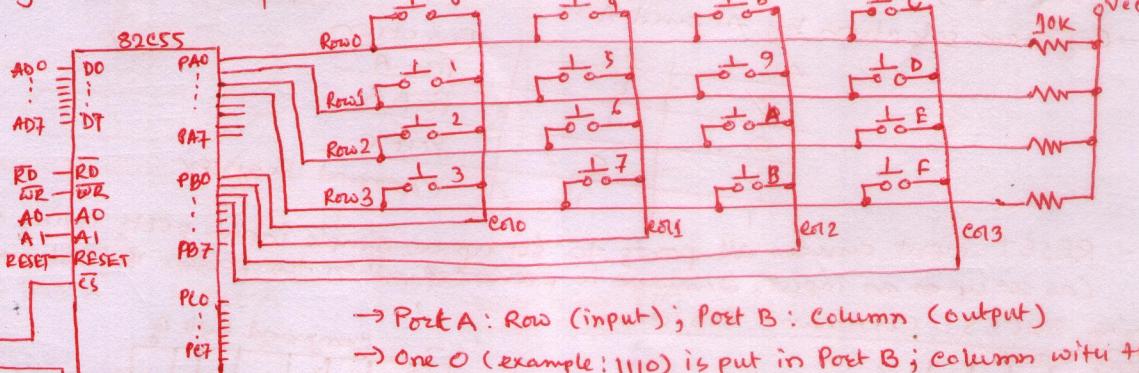
$$\overline{es} = \overline{A5} * \overline{A4} * \overline{A3} * \overline{A2} * \overline{A1} * \overline{A0} * \overline{A9} * \overline{A8} * \overline{A7}$$

$$* \overline{A6} * \overline{A5} * \overline{A4} * \overline{A3} * \overline{A2} * \overline{D0}$$

- 8255 is interfaced to an 8088 MP through a PAL16L8 so that it functions at 140ns port numbers
- Resistors are chosen to limit the segment current
- Different assembly codes \Rightarrow self start.

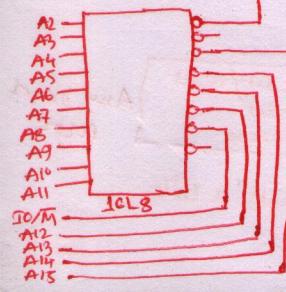
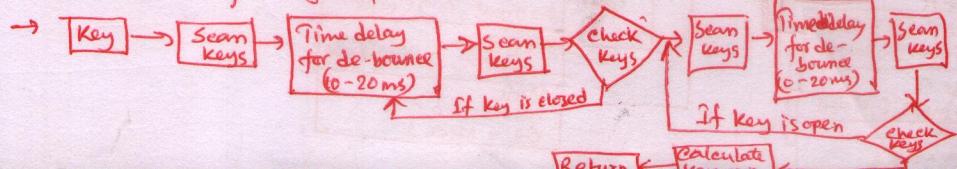


\Rightarrow Key Matrix Interface:



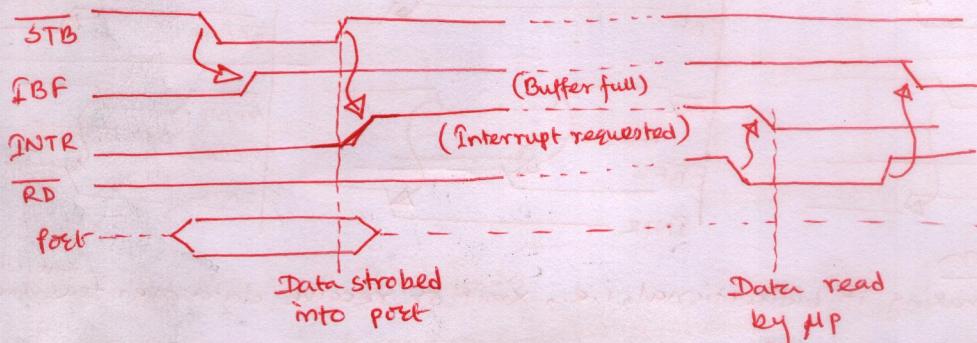
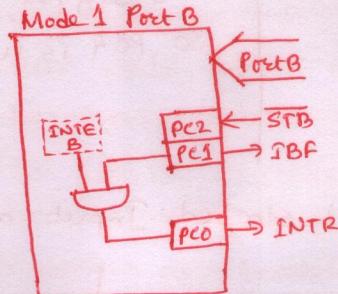
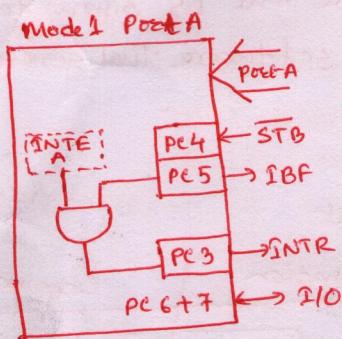
\rightarrow Port A: Row (input); Port B: Column (output)

\rightarrow One 0 (example: 1110) is put in Port B; column with that 0 gets selected; Any key in that column gives a 0 to corresponding pin in Port A, if it gets pressed



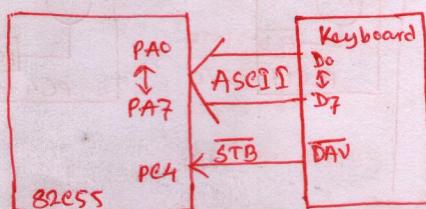
Mode 1 : Strobed Input

- Allows external data to be stored into the port until the μP is ready to retrieve it



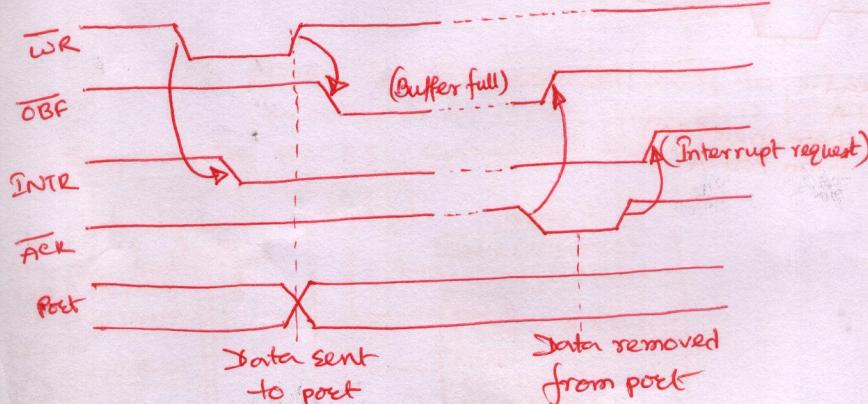
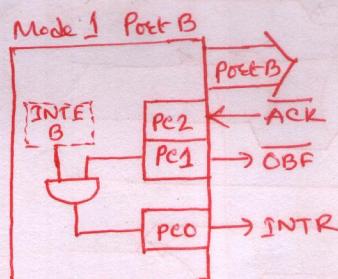
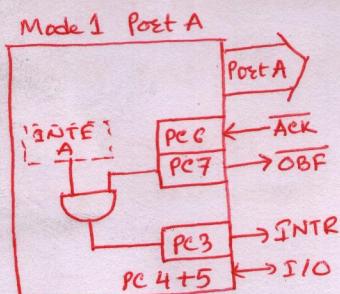
\overline{STB} \Rightarrow Input; Loads data into port latch, which holds the info until the μP reads it via IN
 \overline{IBF} \Rightarrow (Input Buffer Full) Output; Indicates that the input latch contains info
 \overline{INTR} \Rightarrow (Interrupt Request) Output; Requests an interrupt; Becomes 1 when \overline{STB} returns to 1; Gets cleared when data is read by the μP
 \overline{INTE} \Rightarrow (Interrupt Enable) neither an input nor an output. It is an internal bit programmed via the port PC4 (Port A) or PC2 (Port B) bit pos?
 $\overline{PC6,7}$ \Rightarrow General-purpose I/O pins, available for any purpose

- Strobed input port captures data from the port pins when the strobe (\overline{STB}) is activated. Strobe captures the data on the 0-to-1 transition
 - Strobe activates IBF and INTR
- \Rightarrow Strobed Input: Keyboard



- The keyboard encoder de-bounces key switches, and provides a strobe signal whenever a key is depressed (data output contains ASCII of the key)
- DAV (Data Available) is activated for 1'0 μs each time a key is typed. This causes data to be strobed in Port A - through \overline{STB} . \overline{STB} also activates IBF.

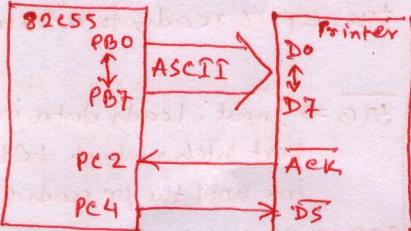
Mode 1: Strobed Output



\overline{OBF} \Rightarrow (Output Buffer Full) Output; Goes low whenever data are output to Port A or Port B latch. Set to 1 whenever ACK returns from device.
 \overline{ACK} \Rightarrow causes \overline{OBF} to return 1. It is a response from external device indicating it has received data from 8255 port
 \overline{INTR} \Rightarrow Interrupts μP when external device receives data via ACK signal

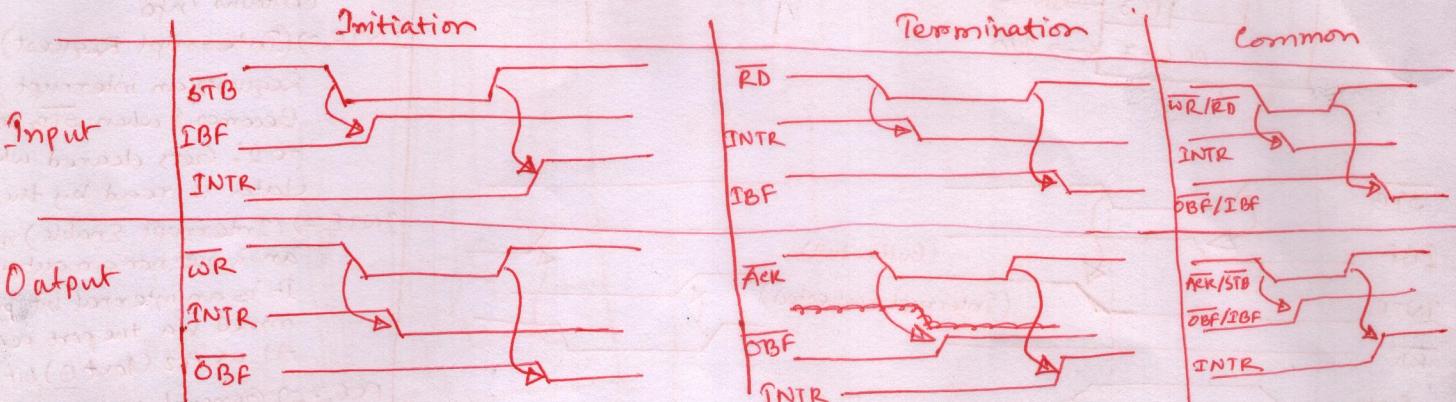
\overline{INTE} \Rightarrow Programmed to enable INTR. (PC6 for Port A and PC2 for Port B)

⇒ Strobed Output : Keyboard Printer



→ Port B connected to a parallel printer
→ No signal to generate the DS signal to the printer, so PC4 is used with software that generates the DS.

⇒ Comparison between Mode 1 Strobed Input and Output



⇒ Mode 2 : Bidirectional Operation

- Allowed with group A only making it bidirectional, i.e., xmit or receive data over the same eight wires
- Useful when interfacing two computers

