ShanghaiTech University

EE 115B: Digital Circuits

Solution

Fall 2022

Midterm Exam 2, November 29, 2022

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Student ID: _____ Name in Chinese: _____

1. Short questions. (15 points. 3 points each.)
   (1) What does "VHDL" stand for?

VHSIC (Very High Speed Integrated Circuits)
Hardware Description Language

   (2) What does "FPGA" stand for?

Field Programmable Gate Array

   (3) (True or False) IF statements can only appear in PROCESS blocks.

True

   (4) Given the following VHDL code, determine the value of A(5 downto 2).

```
signal A: std_logic_vector (8 downto 1);
A <= "01101001";
```

   A(5 downto 2)= 0100

   (5) Given the following VHDL code, write the logic function for F.

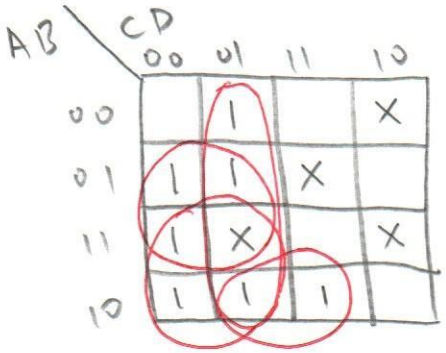
```
F <= A xor B or C and D;
```

   F= $(A \oplus B + C)D$

2. Develop the minimum SOP and POS expressions with the don't cares using Karnaugh map. (20 points. 10 points each.)

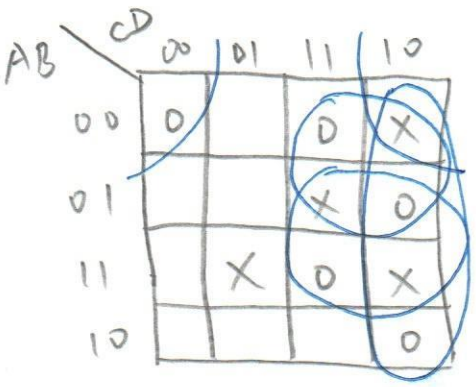
$$Y(A,B,C,D) = \sum m(1,4,5,8,9,11,12) + D(2,7,13,14)$$

(1) SOP



$$Y = \bar{C}D + B\bar{C} + A\bar{C} + A\bar{B}D$$

(2) POS



$$Y = (\bar{C}+D)(A+\bar{C})(\bar{B}+\bar{C})(A+B+D)$$

$\overline{A+BC} = \overline{A}\ \overline{B}\ \overline{C}$ $\quad (\,(AC+B'C+A'BC')'\,)' = (\overline{AC}\cdot\overline{B'C}\cdot\overline{A'BC'}\,)'$

3. Convert the following AND-OR expression to NAND, AND-OR-Invert (AOI), and NOR expressions. (21 points. 7 points each.)

$$Y(A,B,C) = AC + B'C + A'BC'$$

(1) NAND (SOP)

$$Y = AC + \overline{B}C + \overline{A}B\overline{C} = \overline{AC + \overline{B}C + \overline{A}B\overline{C}}$$

$$= \overline{\overline{AC}\cdot\overline{\overline{B}C}\cdot\overline{\overline{A}B\overline{C}}}$$

(2) AOI combine 0 → SOP.

A \ BC	00	01	11	10
0	0	1	0	1
1	0	1	1	0

$$Y = \overline{\overline{B}\overline{C} + A\overline{C} + \overline{A}BC}$$

(3) NOR

$$Y = \overline{\overline{B}\overline{C} + A\overline{C} + \overline{A}BC} = \overline{\overline{\overline{B}\overline{C}} + \overline{A\overline{C}} + \overline{\overline{A}BC}}$$

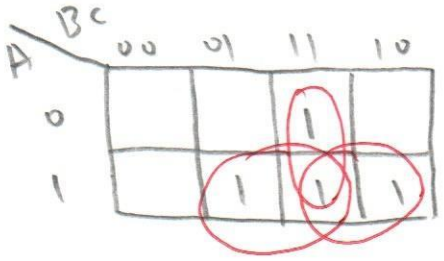
$$= \overline{\overline{B+C} + \overline{\overline{A}+C} + \overline{A+\overline{B}+\overline{C}}}$$

4. Design a circuit with three inputs and one output. The output is 1 if at least two inputs are 1. You need to: (a) define the logic variables and build the truth table (8 points), (b) develop the minimum SOP expression for the output (4 points), and (c) draw the circuit diagram using AND, OR, and NOT gates based on the minimum SOP expression (8 points). (20 points.)

(a) Inputs: A, B, C. Output: Y.

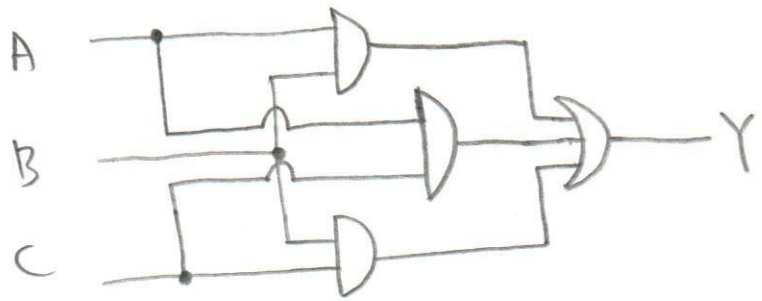
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(b)



$Y = AC + AB + BC$

(c)



5. Plot the output (Y_0 through Y_7) waveforms given the following inputs to the 3-8 decoder (also a DEMUX) 74LS138. The enable inputs G_{2A} and G_{2B} are set as LOW all the time. (24 points. 3 points each.)