ShanghaiTech University

EE 115B: Digital Circuits

Fall 2022

Lecture 12

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Comparators

The function of a comparator is to compare the magnitudes of two binary numbers to determine the relationship between them. In the simplest form, a comparator can test for equality using XNOR gates.

Example How could you test two 4-bit numbers for equality?

Solution AND the outputs of four XNOR gates.

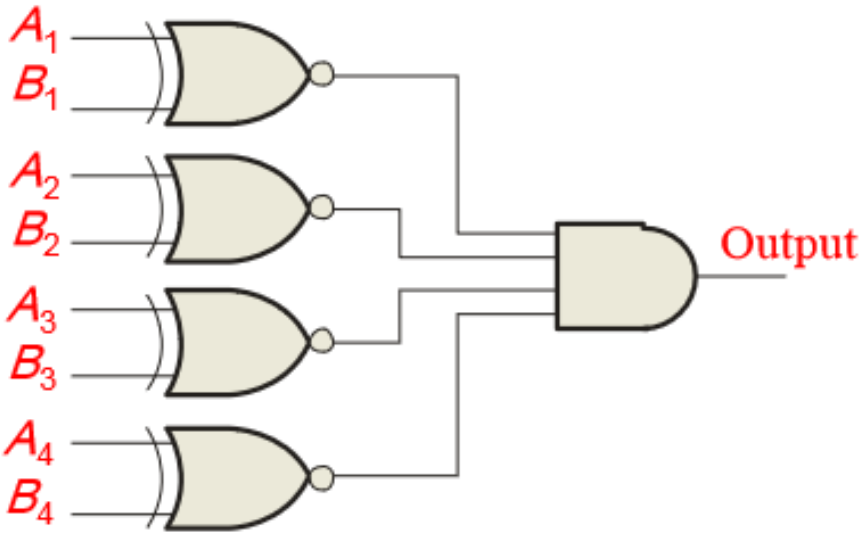


FIGURE 6-18 Basic comparator operation.

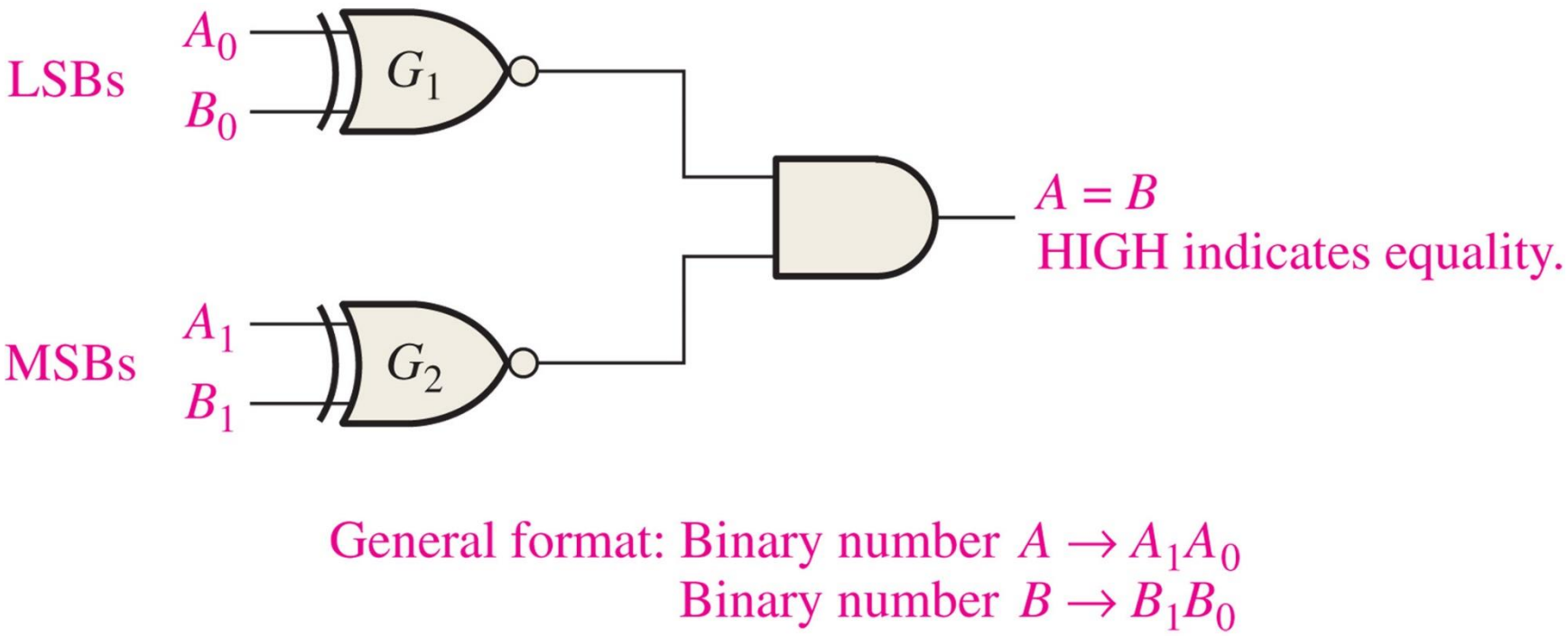


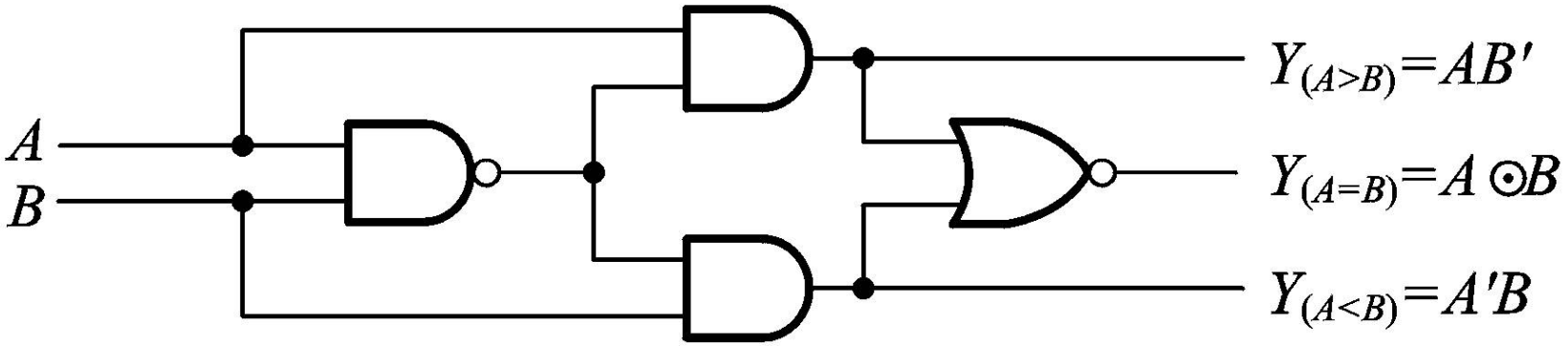
FIGURE 6-19 Logic diagram for equality comparison of two 2-bit numbers.

4.4.5 数值比较器

- 用来比较两个二进制数的数值大小

一、1位数值比较器　　A,B比较有三种可能结果

* $A>B(A=1,B=0)$则$AB'=1,\therefore Y_{(A>B)}=AB'$
* $A<B(A=0,B=1)$则$A'B=1,\therefore Y_{(A<B)}=A'B$
* $A=B(A,B$同为0或1$),\therefore Y_{(A=B)}=(A\oplus B)'$



二、多位数值比较器

1. 原理：从高位比起，只有高位相等，才比较下一位。
2. C and D: numbers with n+1 bits (general expressions)

$$Y_{(C>D)} = C_n\overline{D_n} + (C_n \odot D_n)C_{n-1}\overline{D_{n-1}} + \cdots +$$
$$(C_n \odot D_n)(C_{n-1} \odot D_{n-1}) \cdots (C_1 \odot D_1)C_0\overline{D_0}$$

$$Y_{(C<D)} = \overline{C_n} D_n + (C_n \odot D_n)\overline{C_{n-1}} D_{n-1} + \cdots +$$
$$(C_n \odot D_n)(C_{n-1} \odot D_{n-1}) \cdots (C_1 \odot D_1)\overline{C_0} D_0$$

$$Y_{(C=D)} = (C_n \odot D_n)(C_{n-1} \odot D_{n-1}) \cdots (C_1 \odot D_1)(C_0 \odot D_0)$$

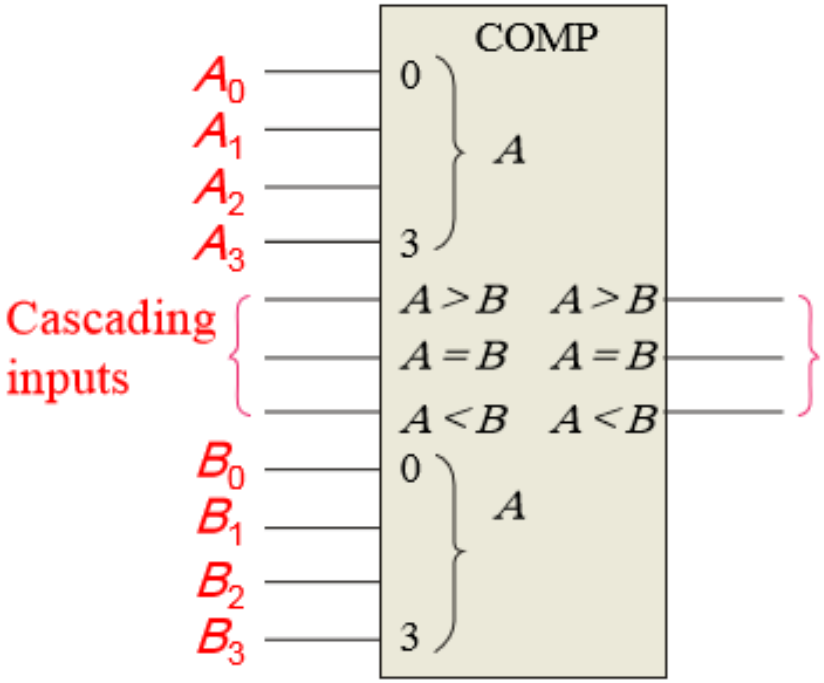
Cascaded structure

1. A and B: 4 highest-order bits of numbers with >=4 bits
2. Results of lower-order bits: $I_{(A>B)}$, $I_{(A<B)}$, and $I_{(A=B)}$
3. For numbers with <=4 bits (first stage of cascaded structure): $I_{(A>B)}=I_{(A<B)}=0$, $I_{(A=B)}=1$

$$
\begin{aligned}
Y_{(A>B)} &= A_3B_3' + (A_3 \odot B_3)A_2B_2' + (A_3 \odot B_3)(A_2 \odot B_2)A_1B_1' \\
&\quad + (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)A_0B_0' \\
&\quad + (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \odot B_0)I_{(A>B)} \\
Y_{(A<B)} &= A_3'B_3 + (A_3 \odot B_3)A_2'B_2 + (A_3 \odot B_3)(A_2 \odot B_2)A_1'B_1 \\
&\quad + (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)A_0'B_0 \\
&\quad + (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \odot B_0)I_{(A<B)} \\
Y_{(A=B)} &= (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \odot B_0)I_{(A=B)}
\end{aligned}
$$

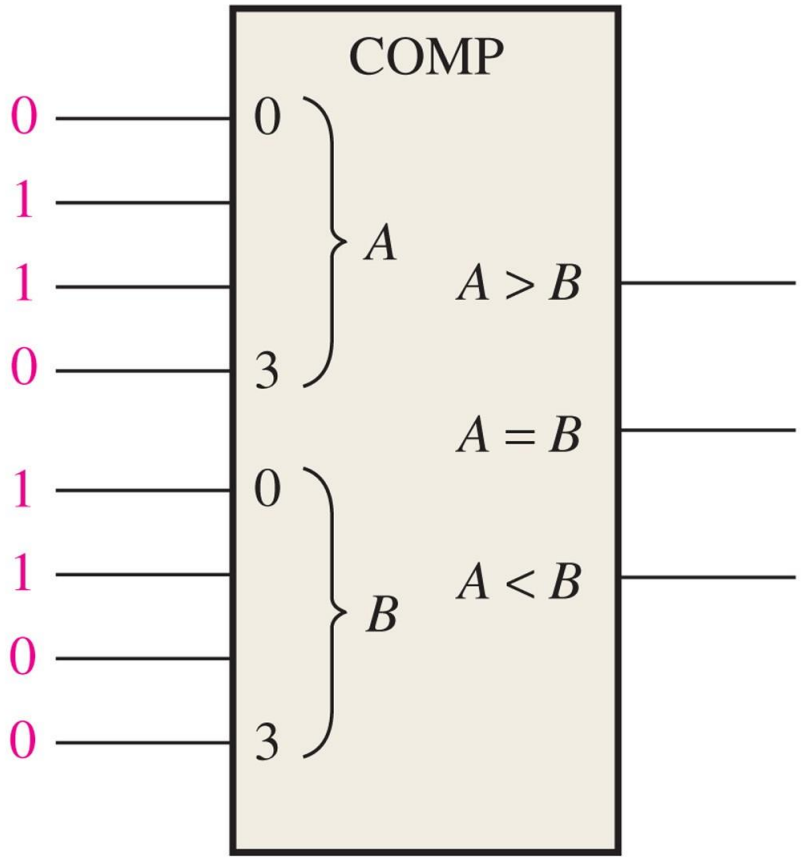
Comparators

IC comparators provide outputs to indicate which of the numbers is larger or if they are equal. The bits are numbered starting at 0, rather than 1 as in the case of adders. Cascading inputs are provided to expand the comparator to larger numbers.



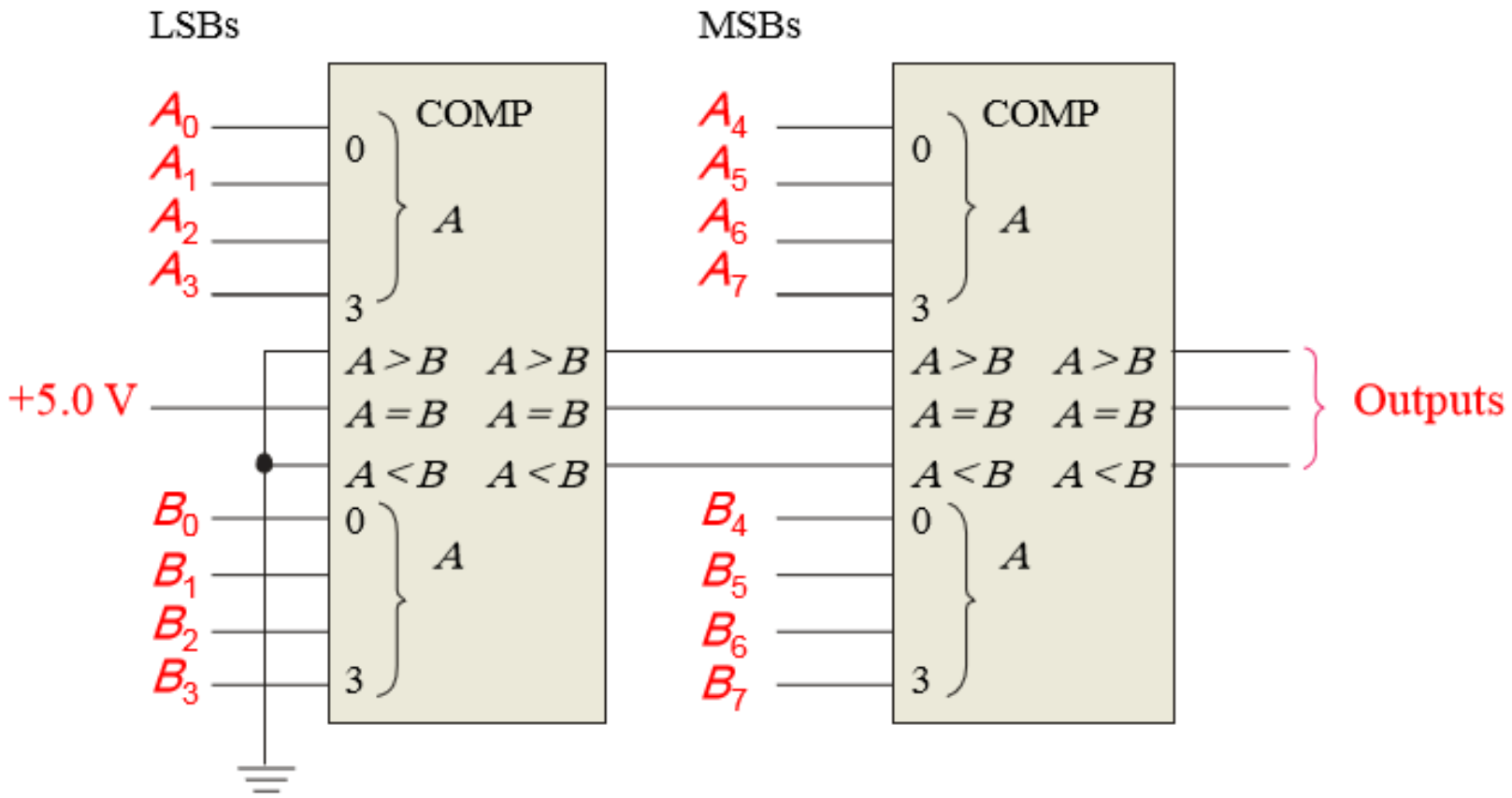
The IC shown is the 4-bit 74LS85.

Example: A>B output is HIGH. The other two outputs are LOW.



Comparators

IC comparators can be expanded using the cascading inputs as shown. The lowest order comparator has a HIGH on the $A = B$ input.



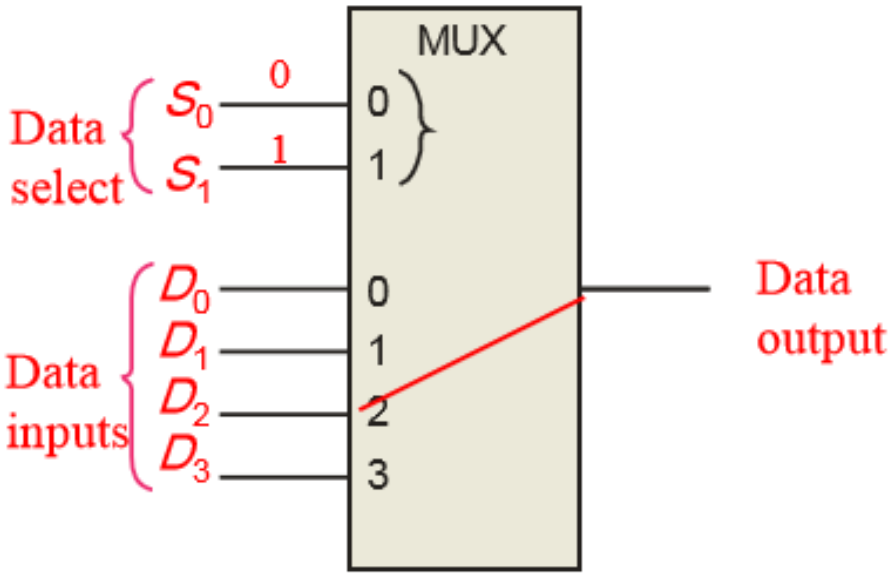
Multiplexers (Data Selectors)

A multiplexer (MUX) selects one data line from two or more input lines and routes data from the selected line to the output. The particular data line that is selected is determined by the select inputs.

Two select lines are shown here to choose any of the four data inputs.

Question

Which data line is selected if $S_1S_0 = 10$? D_2



4-to-1 (1-of-4) MUX

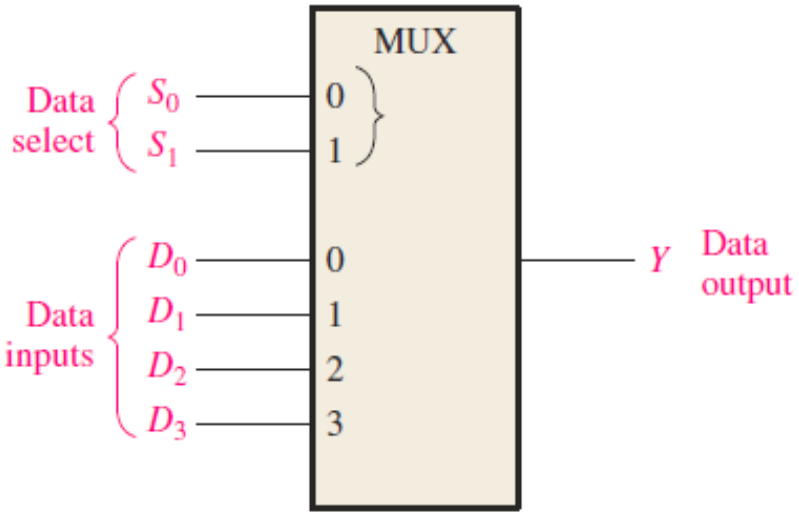


TABLE 6–8

Data selection for a 1-of-4-multiplexer.

Data-Select Inputs		
S_1	S_0	Input Selected
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

The data output is equal to D_0 only if $S_1 = 0$ and $S_0 = 0$: $Y = D_0\overline{S}_1\overline{S}_0$.

The data output is equal to D_1 only if $S_1 = 0$ and $S_0 = 1$: $Y = D_1\overline{S}_1S_0$.

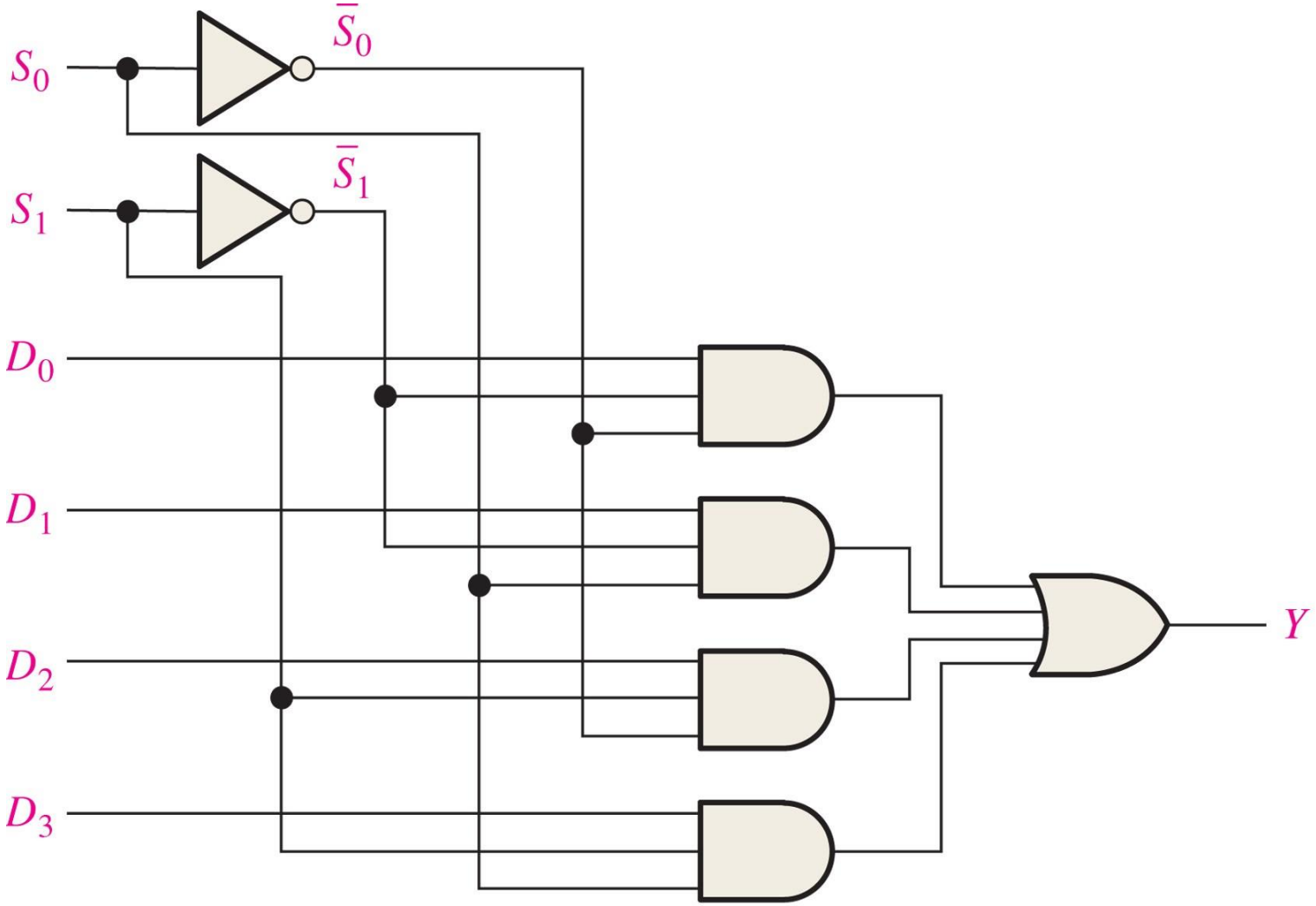
The data output is equal to D_2 only if $S_1 = 1$ and $S_0 = 0$: $Y = D_2S_1\overline{S}_0$.

The data output is equal to D_3 only if $S_1 = 1$ and $S_0 = 1$: $Y = D_3S_1S_0$.

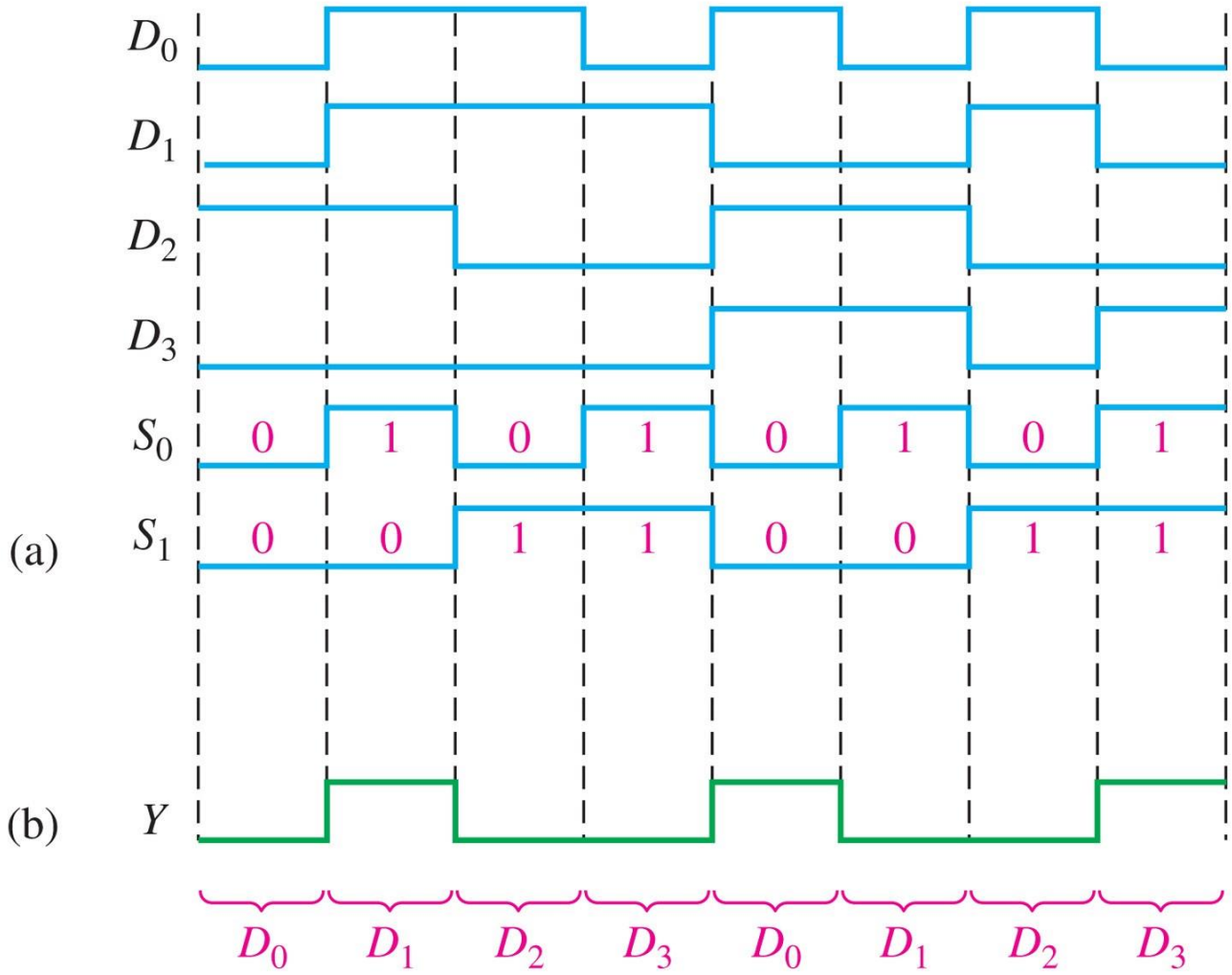
When these terms are ORed, the total expression for the data output is

$$Y = D_0\overline{S}_1\overline{S}_0 + D_1\overline{S}_1S_0 + D_2S_1\overline{S}_0 + D_3S_1S_0$$

FIGURE 6-44 Logic diagram for a 4-input multiplexer.

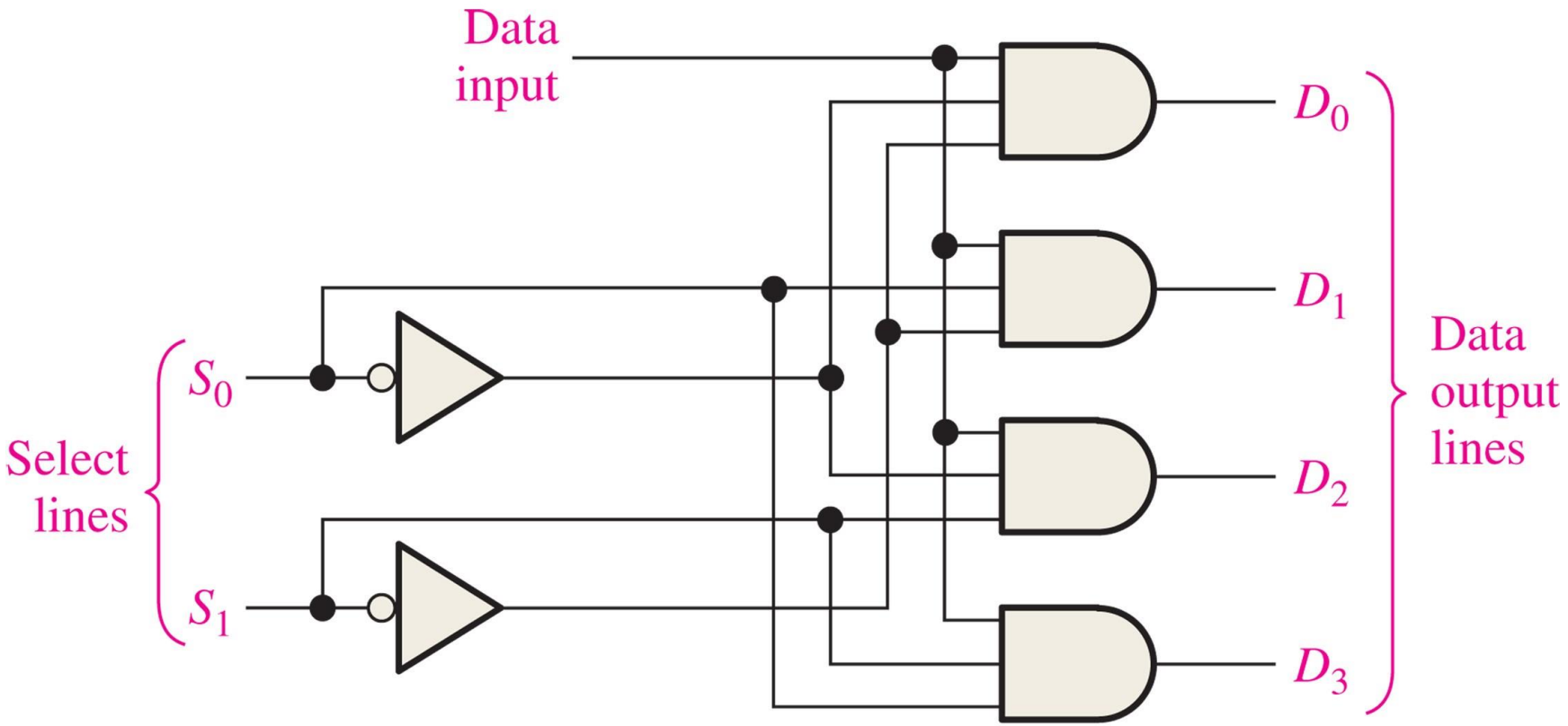


Example: Output waveform of a 4-to-1 MUX.

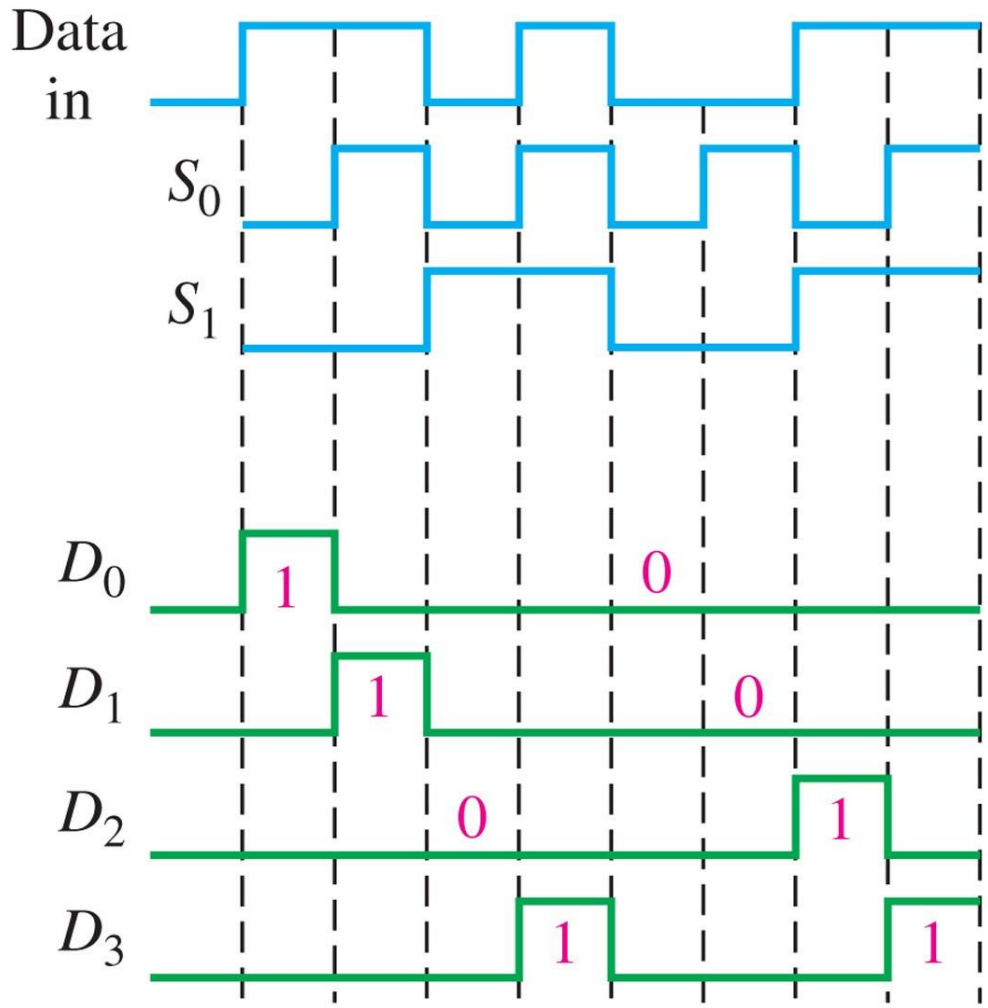


Demultiplexers (Data Distributors)

FIGURE 6-52 A 1-line-to-4-line demultiplexer.



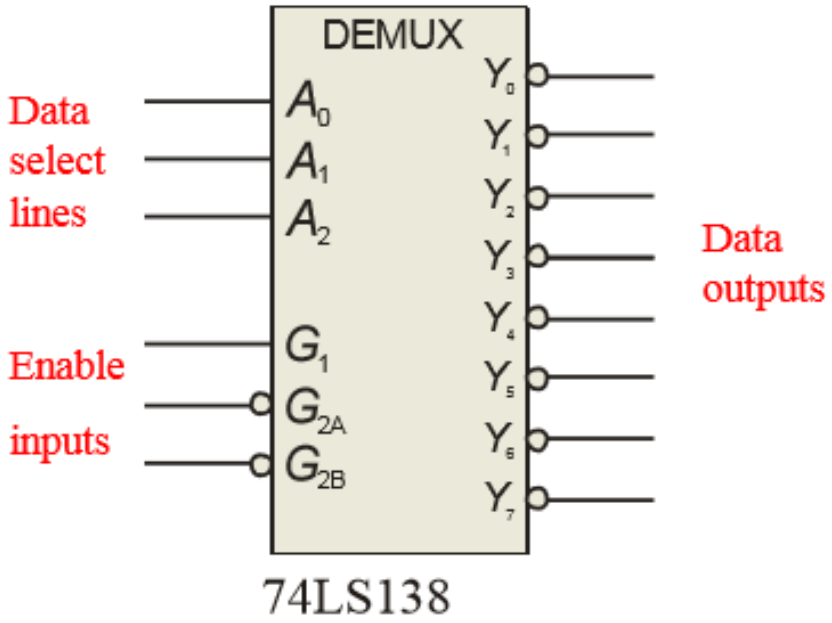
Example: Output waveforms.



Demultiplexers (Data Distributors)

A demultiplexer (DEMUX) performs the opposite function from a MUX. It switches data from one input line to two or more data lines depending on the select inputs.

The 74LS138 was introduced previously as a decoder but can also serve as a DEMUX. When connected as a DEMUX, data is applied to one of the enable inputs, and routed to the selected output line depending on the select variables. Note that the outputs are active-LOW as illustrated in the following example…



74LS138

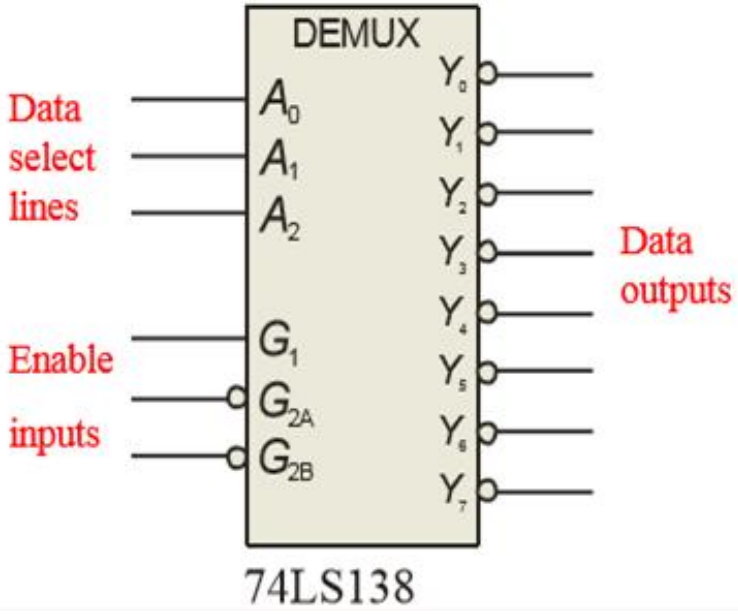
Demultiplexers

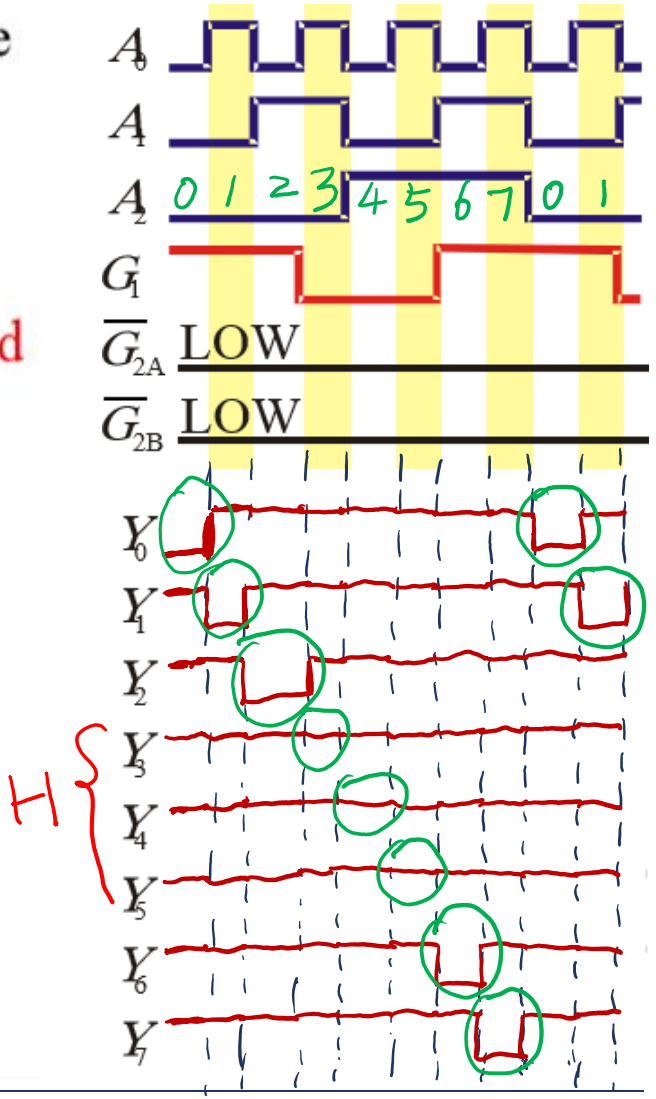
Example

Solution

Determine the outputs, given the inputs shown.

The output logic is opposite to the input because of the active-LOW convention. (Red shows the selected line).





VHDL

- Introduction
- Entity
- Architecture

Introduction

- VHDL
  - VHSIC (Very High Speed Integrated Circuits) Hardware Description Language
- FPGA
  - Field Programmable Gate Array
- IEEE standard 1076
  - Original version adopted in 1987
  - Revised in 1993, 2000, 2002, and 2008

VHDL code: overview

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity circuit1 is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : in  STD_LOGIC;
           f : out  STD_LOGIC);
end circuit1;

architecture behv1 of circuit1 is

-- this is a comment line

signal f1 : std_logic;
signal f2 : std_logic;

begin
   f1<=a and b;
   f2<=c and NOT b;
   f<=f1 or f2;
end behv1;
```

Libraries & packages header

Interface definition: input/output ports

Functional/behavioral description of circuit

VHDL code: overview

- Basic constructs (building blocks)
  - Entity
    - Analogy: circuit symbol
    - Define circuit interface
  - Architecture
    - Analogy: circuit diagram
    - Define circuit functionality