EE115B-Digital Circuits
2nd semester AY 2021/2022
HW2
Due on April 13, 2022

1. Which of the following statements are correct?
(a) The phosphorus doped semiconductor belongs to the N-type
(b) The phosphorus doped semiconductor belongs to the P-type
(c) E_F is closer to E_v in the N-type semiconductor
(d) E_F is closer to E_v in the P-type semiconductor

2. When a N-type and P-type semiconductor make contact, describe the force experienced by the electrons and holes.

3.
(a) Plot the device structure of NMOS and PMOS.
(b) In order to enable the NMOS and PMOS, how should we connect their gates?
(c) Describe the operation principle of NMOS and PMOS.

4.

(a) Construct a three-inputs NAND gate using NMOS and PMOS

(b) Describe its operation

5. Simplify the following expressions using the rules of Boolean algrbra

(a) AB'CD'+(AB')'E+A'CD'E

(b) B'+ABC

(c) (AB+A'B'+A'B+AB')'

6. Transforms $\mathrm{L(A,B,C)} = \overline{(AB + \overline{A}\,\overline{B} + \overline{C})\overline{AB}}$ into the standard SOP form.

7. The logical expression is $L = \overline{A}B\overline{D} + A\overline{B}\,\overline{D} + \overline{A}BD + A\overline{B}\,\overline{C}D + A\overline{B}CD$

(a) Find the simplest AND-OR logical expression and draw the corresponding logic diagram.

(b) Draw a logical diagram of the expression use only NAND gate.

8. Draw the following function using Karnaugh map.

$$\mathrm{L(A, B, C, D)} = (\overline{A} + \overline{B} + \overline{C} + \overline{D})(\overline{A} + \overline{B} + \mathrm{C} + \overline{D})(\overline{A} + \mathrm{B} + \overline{C} + \mathrm{D})(\mathrm{A} + \overline{B} + \overline{C} + \mathrm{D})(\mathrm{A} + \mathrm{B} + \mathrm{C} + \mathrm{D})$$

9.

(a) Develop the minimum SOP and POS expressions for the following function using Karnaugh map.

$$Y(A, B, C, D) = \sum m\,(0, 2, 8, 9, 10, 15) + D(1, 3, 6, 7)$$

(b) Compare their gate usage.