FPGA Design Flow and Vivado Tutorial

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Overview

VHDL Stands for?

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Very High Speed Integrate Circuits (VHSIC) Hardware Description Language

Design Flow

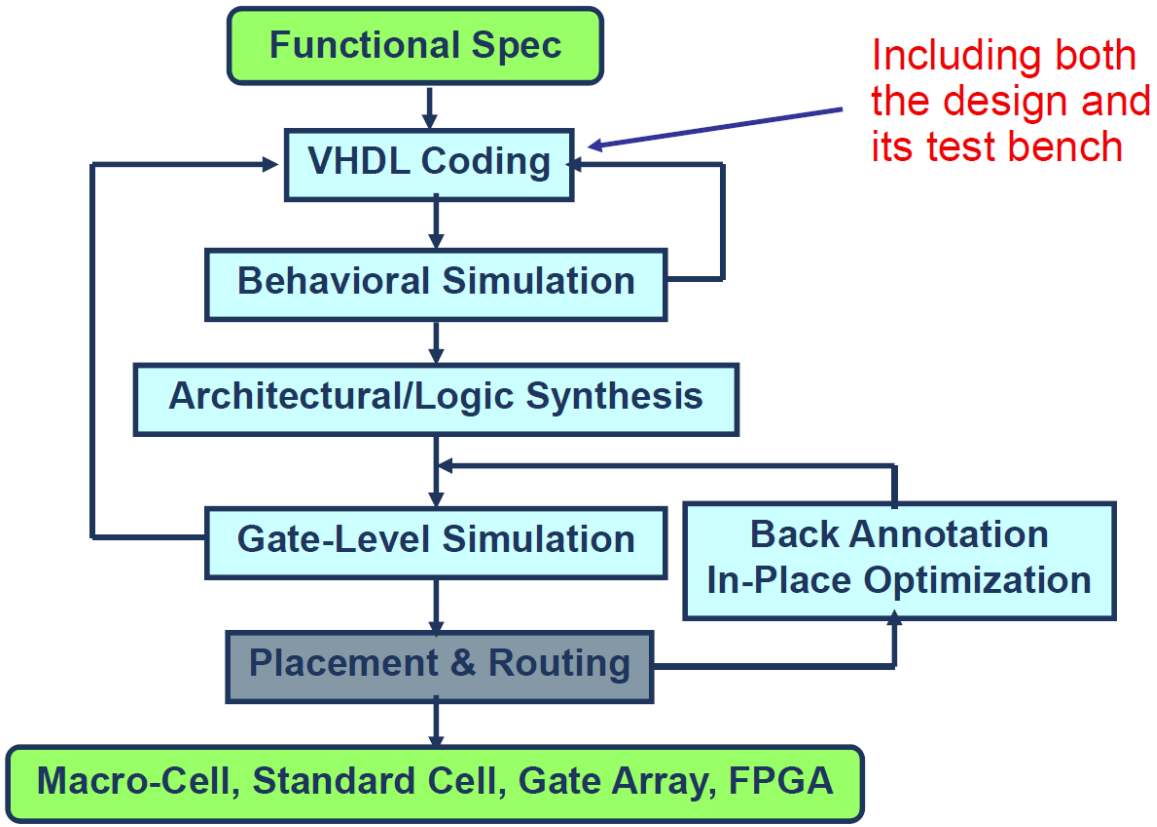

Figure: Typical Design Flow(Credit to: Prof. Ha's Slides)

Design Flow

In this tutorial, we will go through

- Component Description (i.e. Behavioral Coding)
- Structural Design (i.e. Structural Coding)
- Testbench Setup and test vector generation
- Behavioral Simulation
  - No logic delay, all ideal
- Synthesis (optional)
  - Not compulsory, but good for debugging

Before we get started...

Several Hint:

- Keep your entity name and file name aligned
  - e.g. the file name of a DFF should be DFF.vhd
- Be aware of code format, even if there are nearly no restrictions in VHDL

Code Format

Code format I learnt (from failed projects)

- Keywords (except data type) are all lowercase
- The library names and data types are all capitalized.
- Naming must be meaningful (except for the prescribed name). There are no restrictions on naming, and you can reasonably use uppercase letters and underscores to make your name easier to read and understand
- Use four Spaces or a Tab to indent your code. Reasonable indentation makes your code easier to read and understand.

Component Description

An entity contains

- Entity name
- IO(Input and Output)
- Process
  - Sensitivity list may sometimes need
  - Include ALL the signals you need in the list
  - Never present one signal into two separate lists

Structural Description

- Top-level of the whole design (Wrapper)
- Should **NOT** contain any functional description

Testbench Setup

- Testbench should NOT contain neither functional nor structural description
- Testbench has better flexibility, since non-synthesis-able

Vivado Intro.

- From RTL to BitStream, Complete flow
- Good-looking GUI (Personal point of view)

Source Classification

Design Source

- Component Definition and Function Description
- Structural Demonstration and Connecting

Simulation Source

- Testbench itself and input vectors
- Input files, mem files

Schematic Checking

Another way to debug (besides from seeing the wave form)

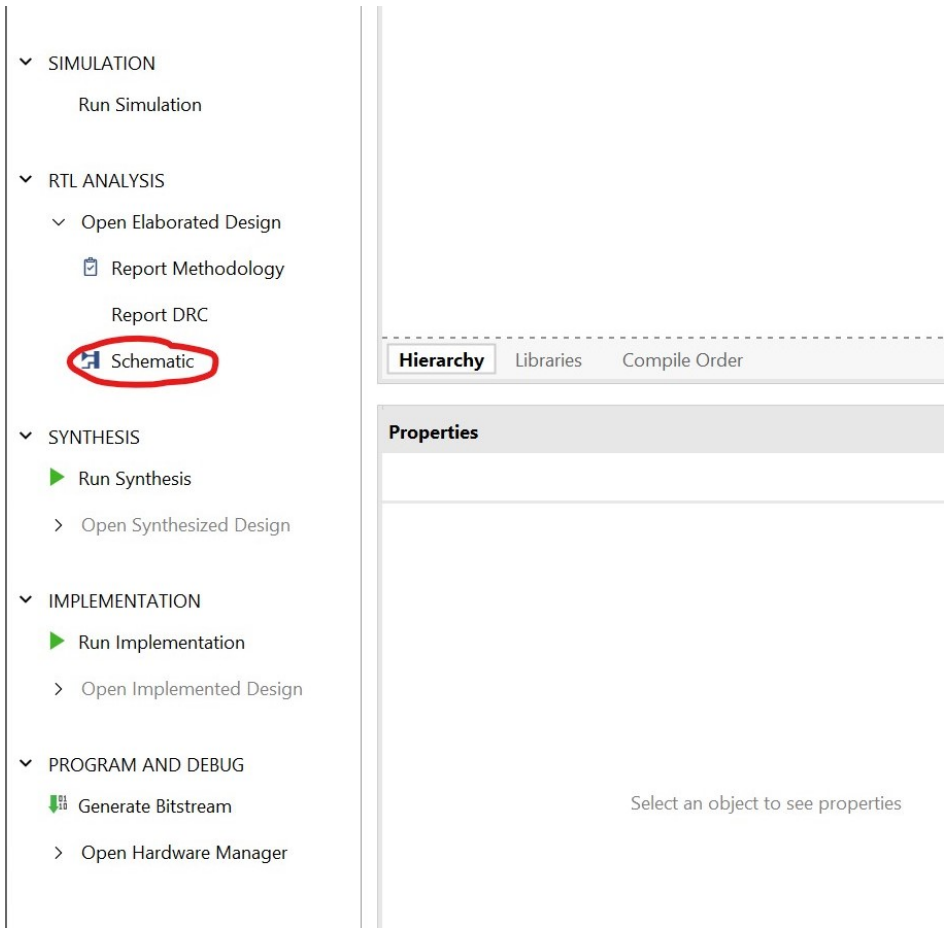

Figure: Indication of the check

Thanks