SIST; ShanghaiTech

Mid-exam; Spring semester; 2021-2022 academic year

EE115B – Digital Circuits

Instructors: Zhifeng Zhu
10:30 a.m., May 06 to 10:30 a.m., May 07, 2022

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INSTRUCTIONS:

- You have 24 hours to complete the exam.
- Your exam will not be graded unless you complete the above section and the cover sheet, and turn in both this exam book and the cover sheet.
- Mark your answers on the exam itself. We will not grade answers written on scratch paper. Please provide details for your answer

STOP! Do not turn this page until the instructor tells you to do so.

Important: This paper contains 16 questions and comprises nine (9) printed pages.

This is an Open BOOK examination with authorized material. The candidate is allowed to bring into the examination hall hardcopy materials.

Do NOT write in this section.

Problem	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Total
Max																	
Points																	

Marker's Signature:
Date:
Rechecker's Signature:
Date:

1. Convert the following unsigned numbers (8 points, 2 points each)

a) $(1100.0101)_2$ = ( )$_{10}$

b) $(76.21875)_{10}$=( )$_2$

c) $(11\times101)_2$=( )$_2$

d) $(1110/10)_2$=( )$_2$

2. The number in the sign-magnitude form is 10101.110, write down its 2's complement form. (4 points)

3. Determine the decimal value of the following numbers, which are expressed in 2's complement (4 points, 2 points each)

a) 111101001

b) 111111111111110010

4. Perform the following calculations using 2’s complement (12points, 3 points each)

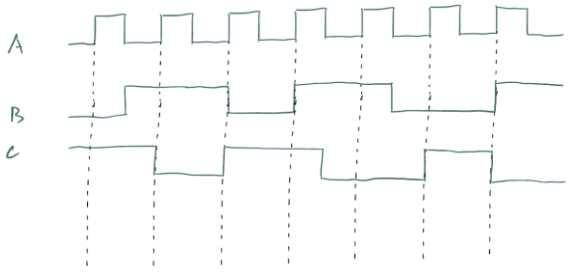
a) 25+32
b) 33−15
c) 9×−4
d) 888/222

5. Draw the truth table of the following gates (6 points, 2 points each)

a) 4-input NAND gate
b) 4-input NOR gate
c) 4-input XOR gate

6. Draw the waveform of the output signal (5 points)

$Y = (A+B)C + (B+C)'(A \oplus B) + A \odot C$



7. Draw the circuit diagram (using MOSFET) of the following gates (4points, 2 points each)

a) 3-input OR gate

b) 4-input NOR gate

8. Which of the following statements are correct? (5 points)

(A) When E_F becomes higher, the number of electrons increases

(B) When E_F becomes lower, the number of electrons increases

(C) When E_F becomes higher, the number of holes increases

(D) When E_F becomes lower, the number of holes increases

9. Write down the 4 variable DeMorgan's Theorem (4 points)

10. Simplify the following expression (6 points, 3 points each)

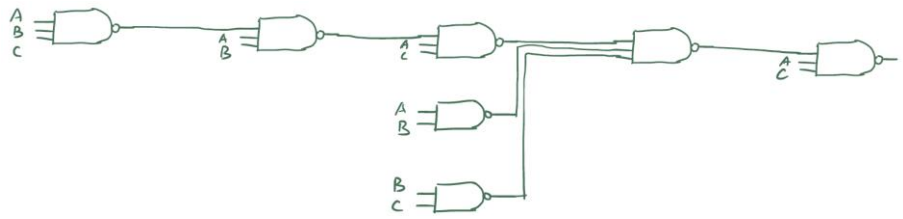
a) (ABC+ABD)'+AC'+B'D

b) AB'+A'B+BC'+B'C

11. For the Boolean expression AB'+AC'D+B'D (15points, 3 points each)

a) Convert to the standard SOP form
b) Simplify the standard SOP form using the Karnaugh map
c) Convert to the standard POS form
d) Simplify the standard POS form using the Karnaugh map
e) Compare their MOSFET gate usage (assume both the true and inverted signals are already available)

12. Write down the logic expression of the following circuit using the principle of bubble-bubble cancellation) (3 points)



13. For the traffic light example discussed in the lecture note 7-Combinational Logic Analysis-publish.pdf, define light on is 0 and light off is 1. For the normal state, define the output as 1. For the problematic state, define the output as 0. Redesign the circuit using only NAND gate. (8 points)

a) Write down the truth table (3 points)
b) Write down the Boolean expression (2 points)
c) Design the circuit using only NAND gates. (3 points)

14. Design the full adder by circling 1 in the Karnaugh map (6 points)

a) Write down the truth table (1 points)

b) Draw the Karnaugh map and simplify the expression (3 points)

c) Draw the circuit (2 points)

15. For the 7 bit Ripple carry adder adding two binary numbers (4 points, 2 points each)

a) Provide two input numbers that gives the worst delay.

b) Assume that it takes t_p to generate the carry in each stage, what is the worst delay to get the carry in the highest stage?

16. Plot the circuit diagram of a 5 bit Look-Ahead Carry Adder (6 points)