ShanghaiTech University

EE 115B: Digital Circuits

Fall 2022

Lecture 16

Hengzhao Yang
November 29, 2022

Flip-Flops

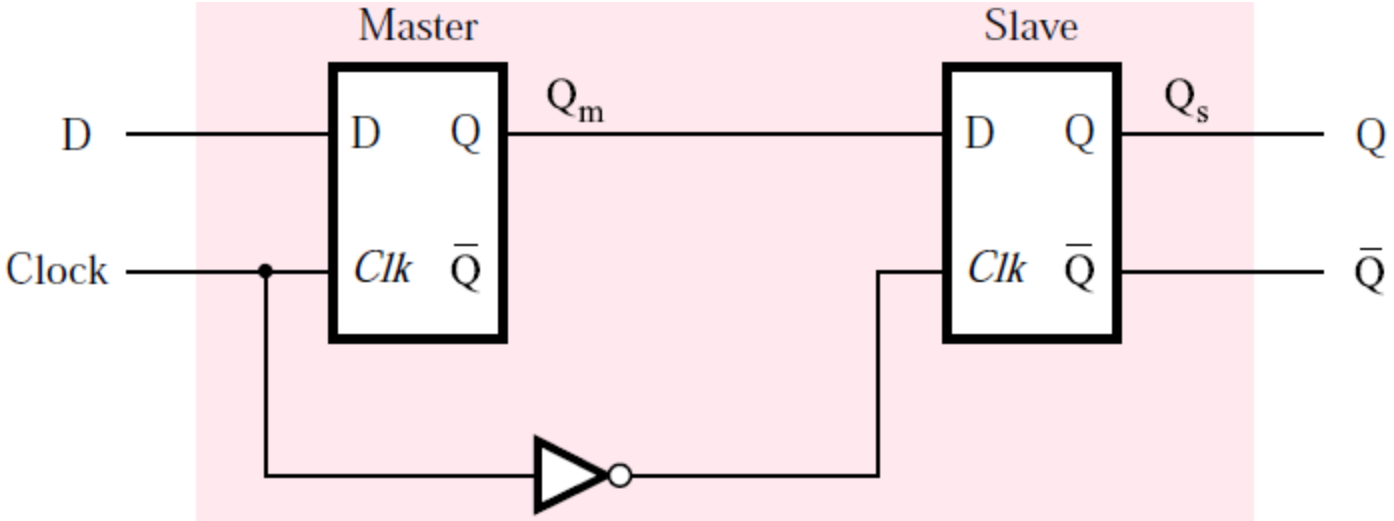
- Edge triggered circuits
  - Output only changes at clock edges (i.e., clock changes from one value to the other)
  - Positive edge: clock changes from 0 to 1
  - Negative edge: clock changes from 1 to 0
  - Output value changes no more than once during one clock cycle
- Examples
  - D flip-flop
  - T flip-flop
  - JK flip-flop

D flip-flops

- Operation
  - Output follows input at active clock edge
- Implementations
  - Master-slave D flip-flop
    - Output changes at negative edge of clock
    - Output changes at positive edge of clock
  - Edge-triggered D flip-flop
    - Positive-edge-triggered
    - Negative-edge-triggered

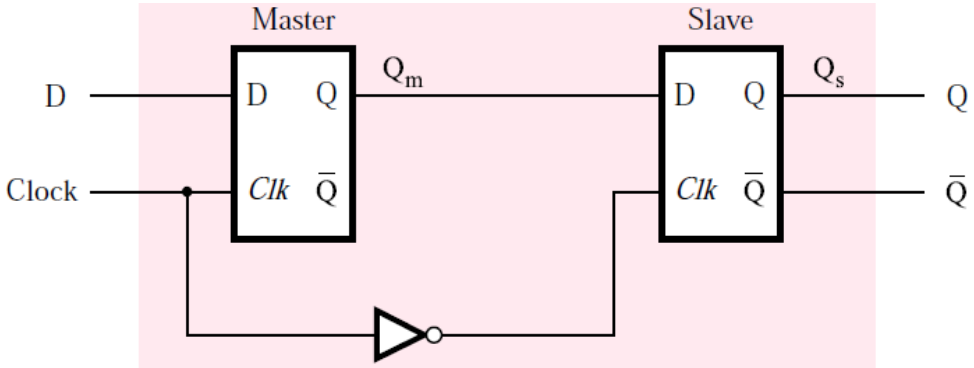
Master-slave D flip-flop: negative edge

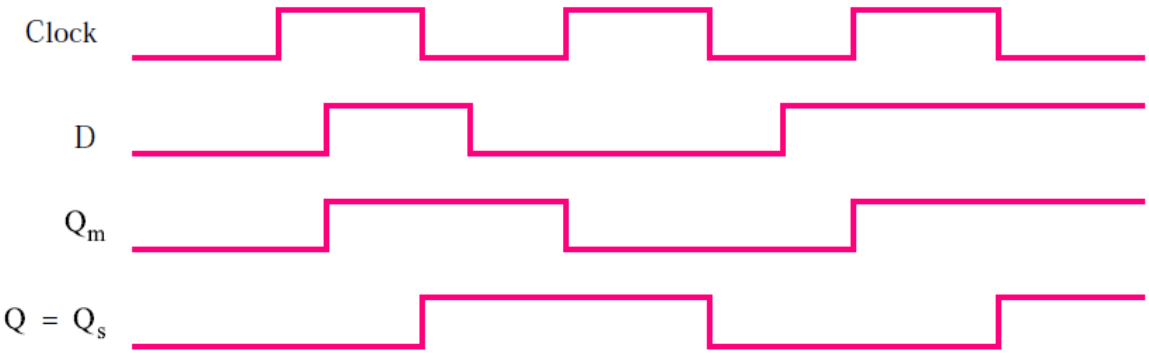
- Master-slave D flip-flop: negative edge
  - Built on 2 gated D latches: master and slave
  - Clock: original for master and complement for slave
  - Output changes at negative edge of clock



Master-slave D flip-flop: negative edge

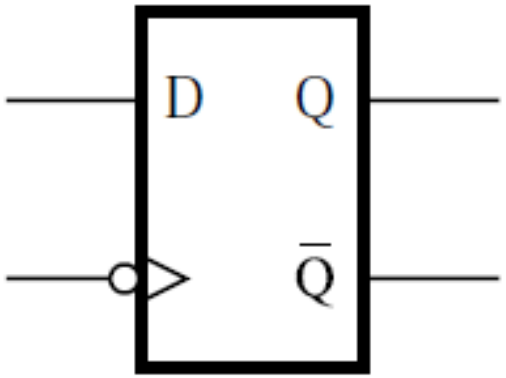
- Operation and timing diagram
  - While Clock=1
    - Master is active
    - Q_m follows D
    - Q_s remains unchanged
  - While Clock=0
    - Slave is active
    - Q_s responds to Q_m, Q (final output) changes at negative edge





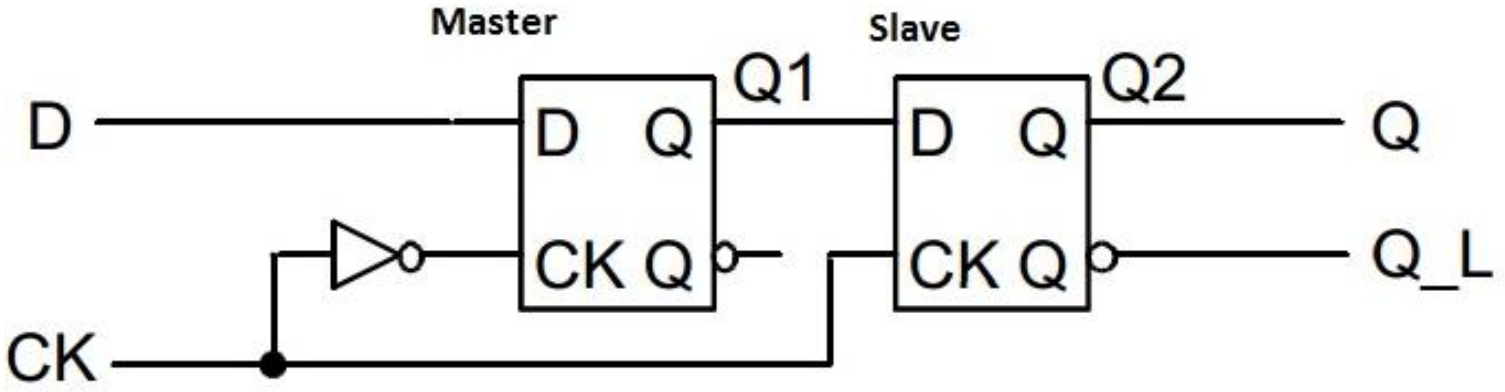
Master-slave D flip-flop: negative edge

- Circuit symbol
  - Symbol “>” denotes active edge of clock
  - Bubble on clock indicates negative edge



Master-slave D flip-flop: positive edge

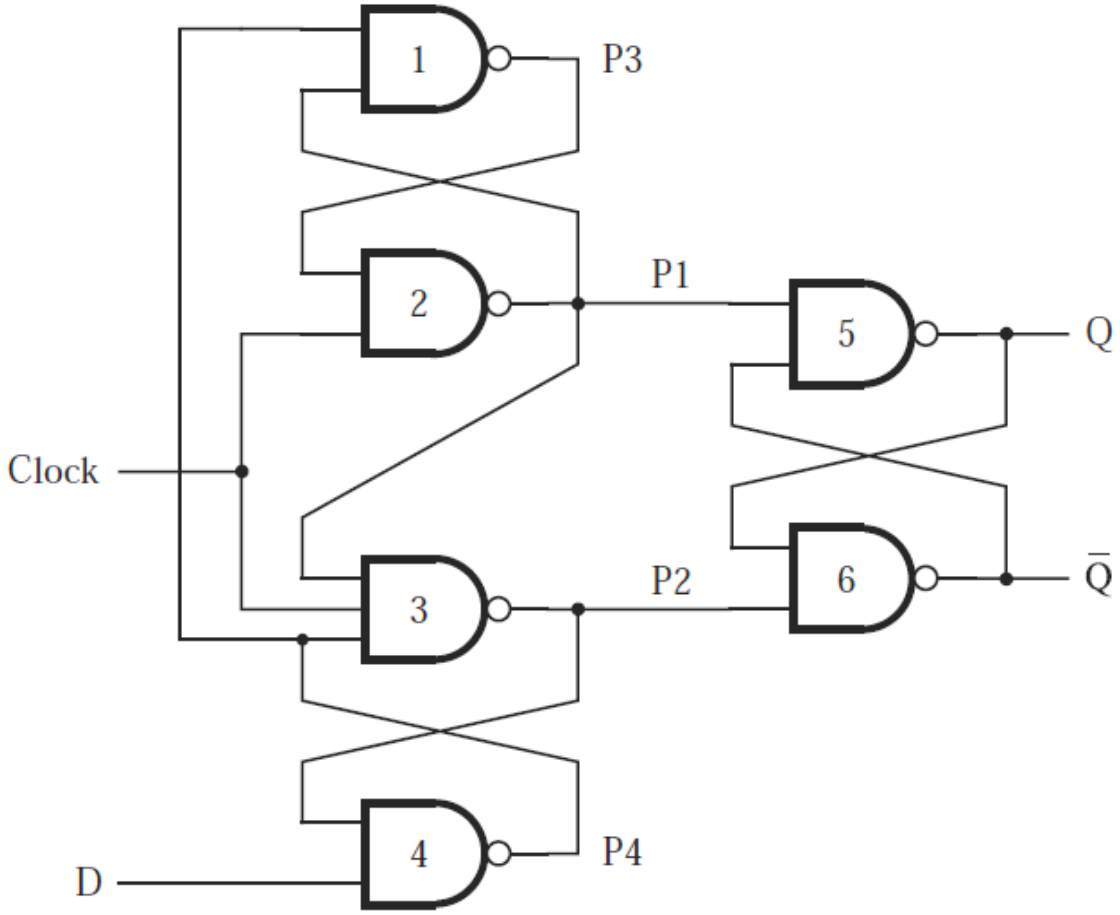
- Master-slave D flip-flop: positive edge
  - Built on 2 gated D latches: master and slave
  - Clock: complement for master and original for slave
  - Output changes at positive edge of clock

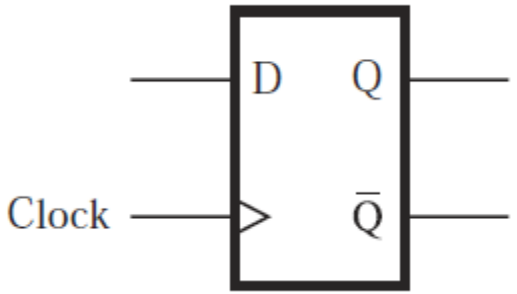


Source: https://allthingsvlsi.files.wordpress.com/2013/04/master-slave-dff.jpg

Edge-triggered D flip-flop: positive

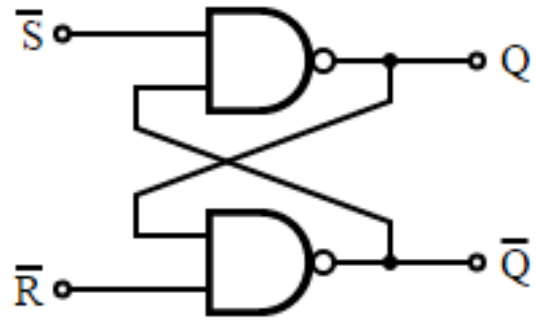
- Circuit and circuit symbol





Edge-triggered D flip-flop: positive

- Clock=0
  - P1=1, P2=1, basic S'R' latch holds
  - P4=D', P3=D
- Positive edge
  - P1=(P3 AND Clock)'=D'
  - P2=(P1 AND Clock AND P4)'=D
  - Q=P1'=D, Q'=P2'=D' (latch: S'=P1, R'=P2)



$\overline{SR}$ latch operation		
$\overline{S}$	$\overline{R}$	Action
0	0	Not allowed
0	1	Q = 1
1	0	Q = 0
1	1	No change