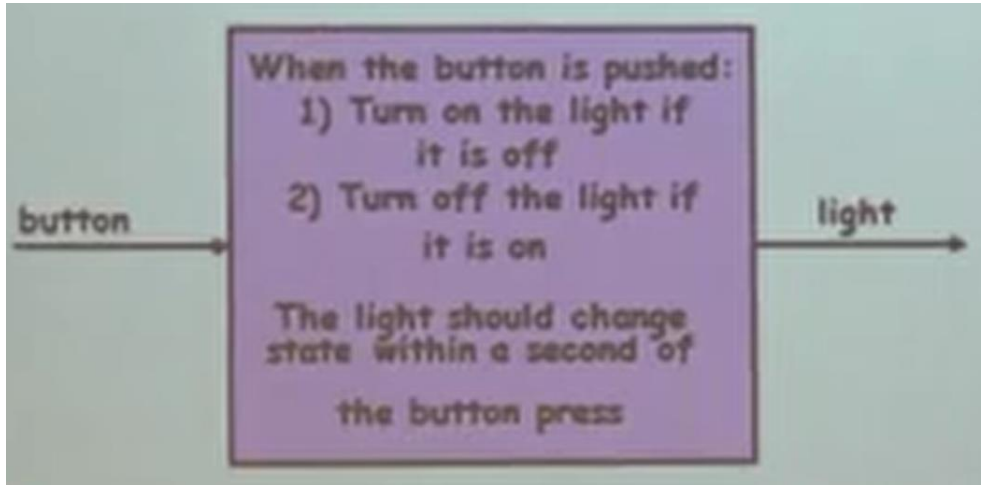
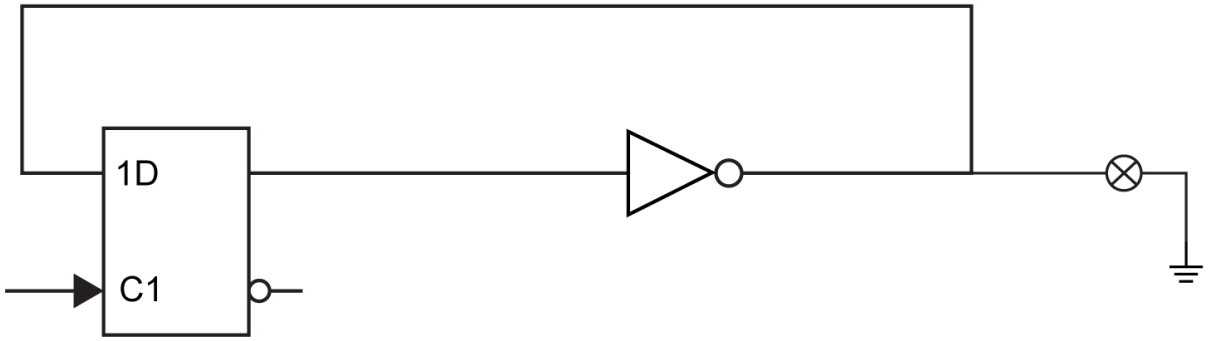
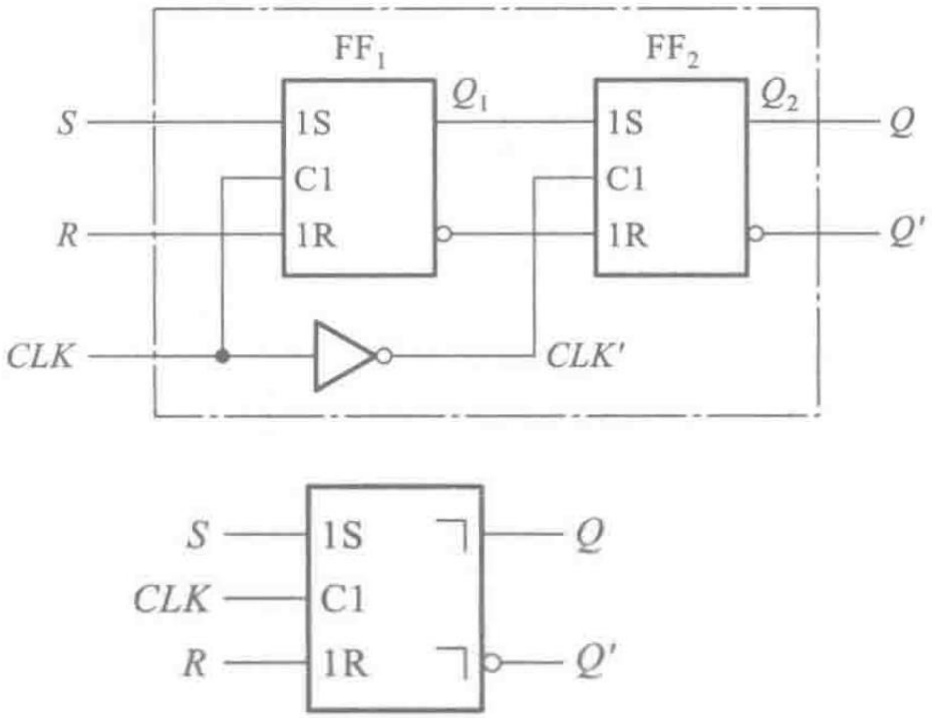
Can we build the button now?





- One needs to press the button precisely the propagation delay of an inverter!

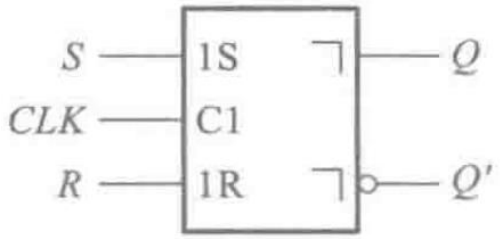
Pulse Trigger S-R Flip-Flops

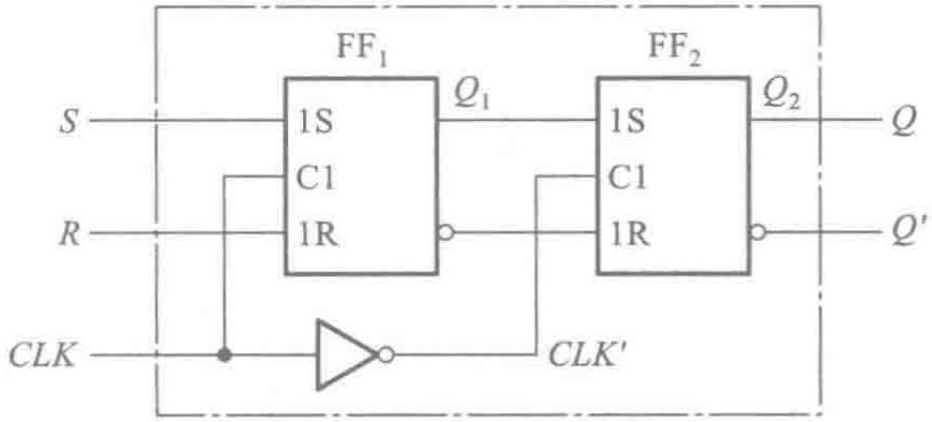


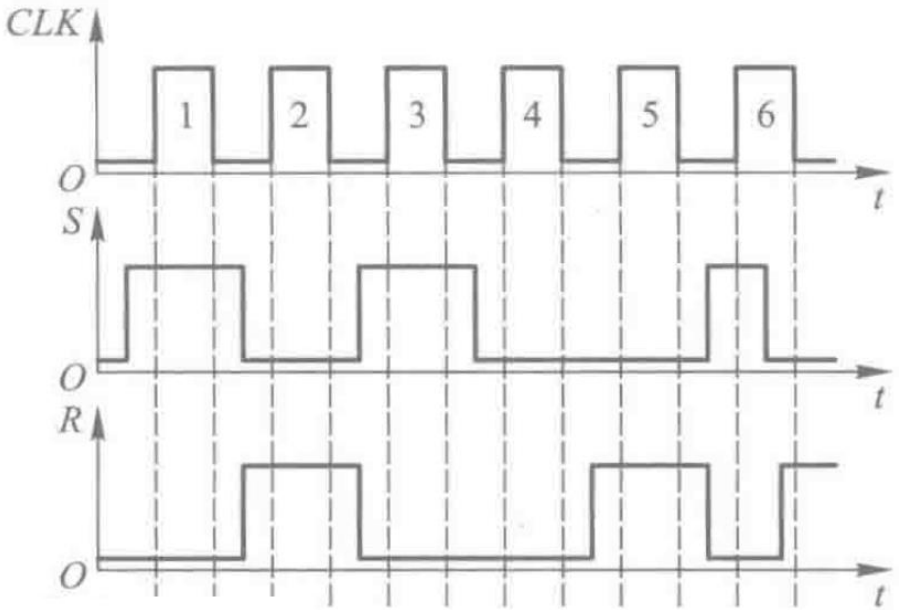
CLK	S	R	Q	Q^*
×	×	×	×	Q
⊓	0	0	0	0
⊓	0	0	1	1
⊓	1	0	0	1
⊓	1	0	1	1
⊓	0	1	0	0
⊓	0	1	1	0
⊓	1	1	0	1①
⊓	1	1	1	1①

- Compared to the level-sensitive latch, the Flip-Flops changes state only on the edge of CLK.
- "⊓" denotes the pulse trigger
- Triggered at the falling edge

Pulse Trigger S-R Flip-Flops

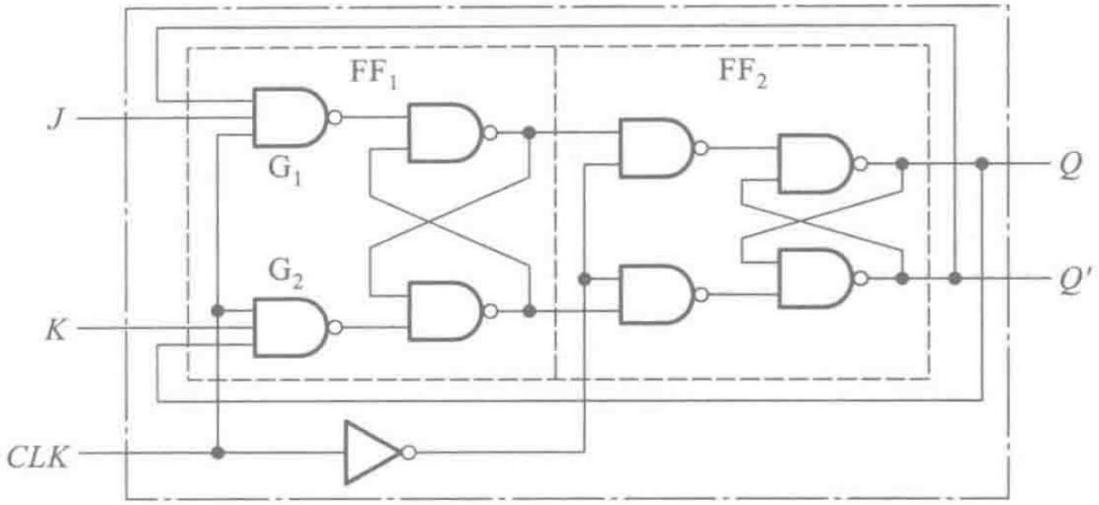


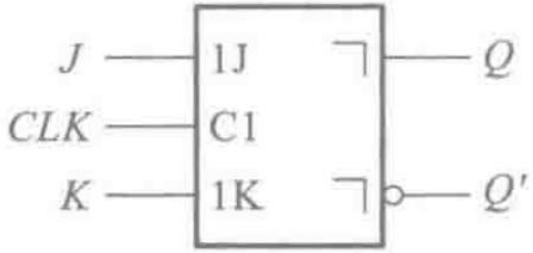




Question: plot the waveform of Q and Q', assume the initial Q and Q_1 is 0

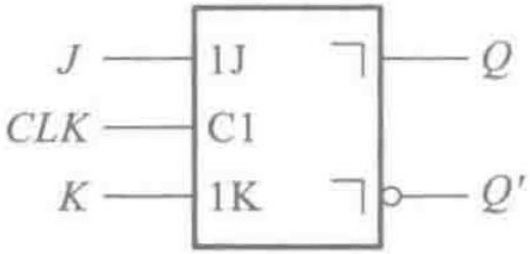
Pulse Trigger J-K Flip-Flops

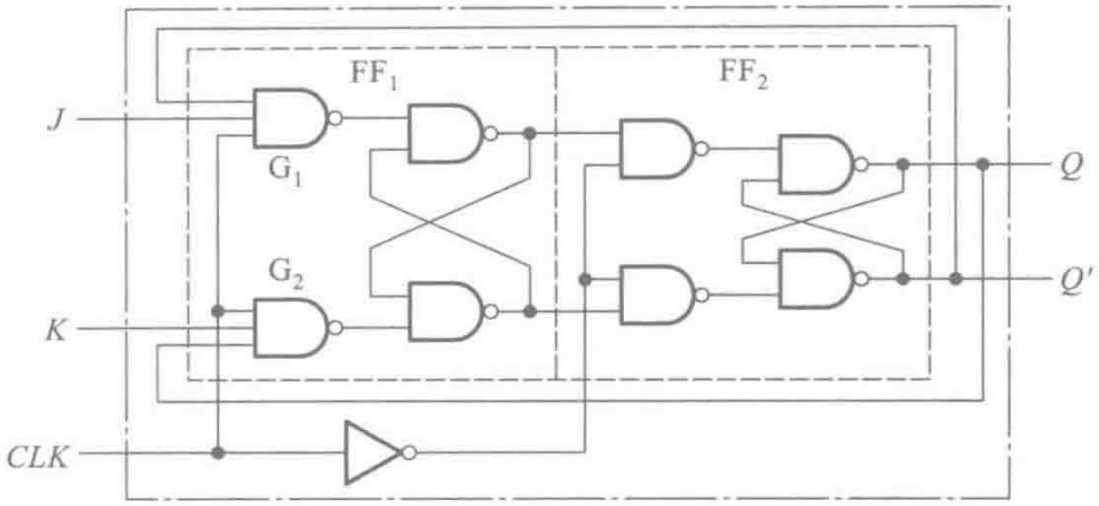


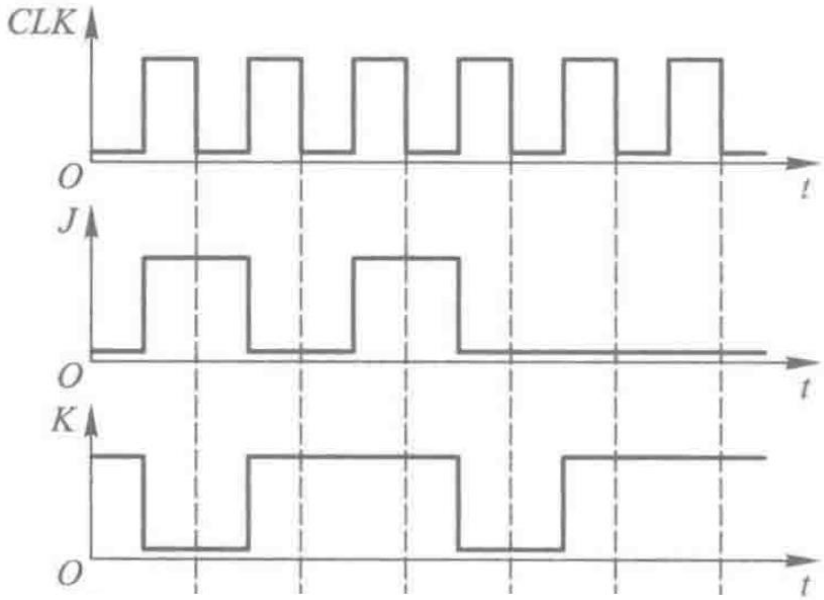


CLK	J	K	Q	Q^*
×	×	×	×	Q
↓	0	0	0	0
↓	0	0	1	1
↓	1	0	0	1
↓	1	0	1	1
↓	0	1	0	0
↓	0	1	1	0
↓	1	1	0	1
↓	1	1	1	0

Pulse Trigger J-K Flip-Flops

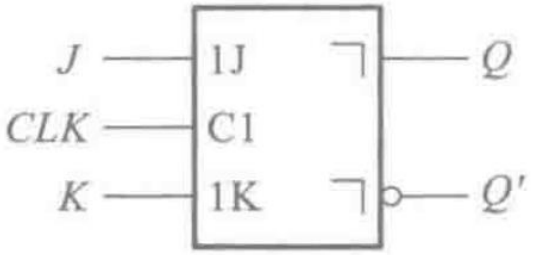


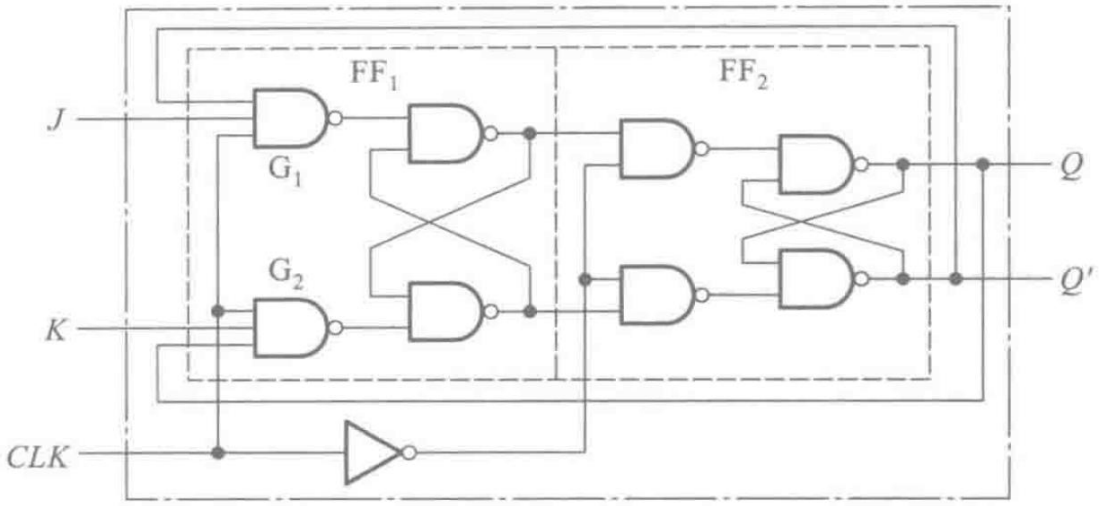


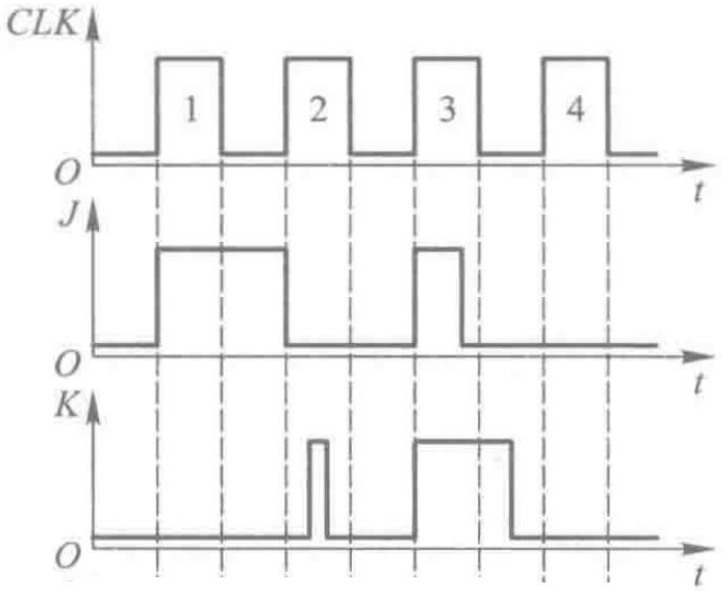


Question: plot the waveform of *Q* and *Q*', assume the initial *Q* and the output of the master stage are 0

Pulse Trigger J-K Flip-Flops



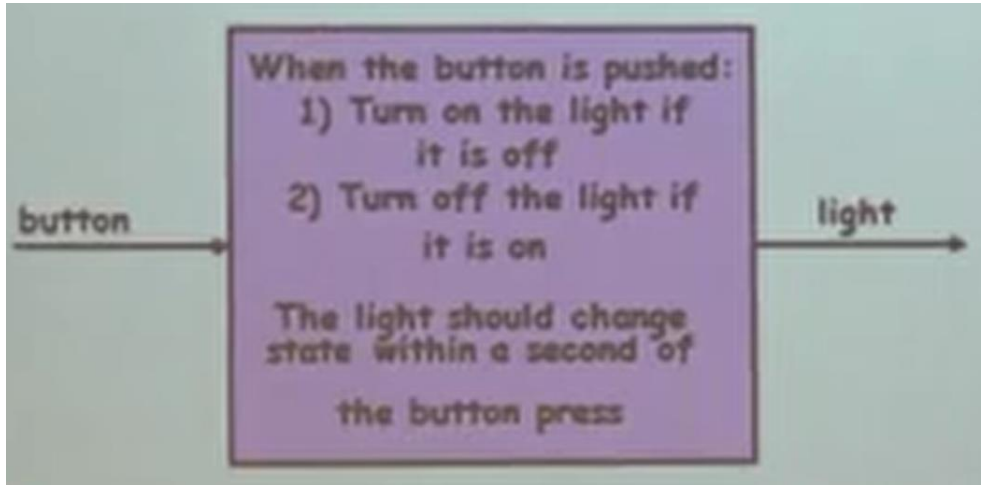


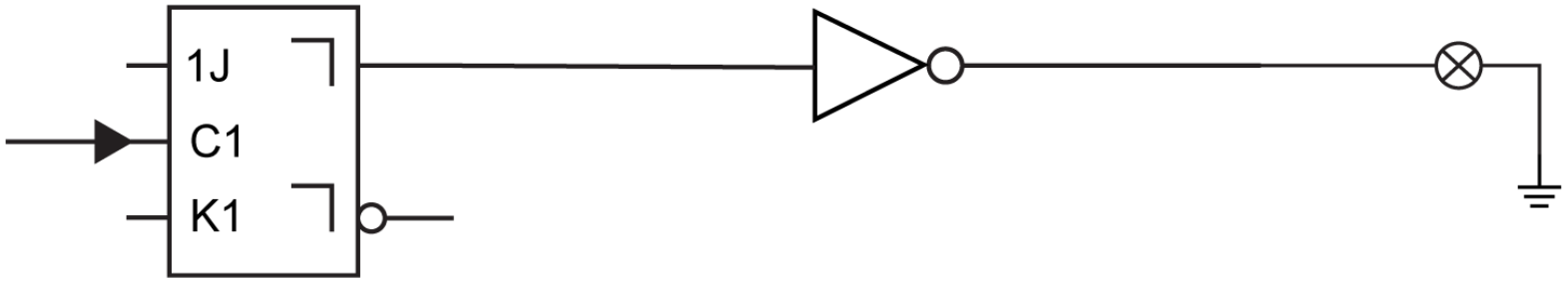


Question: plot the waveform of *Q* and *Q'*, assume the initial *Q* and the output of the master stage are 0

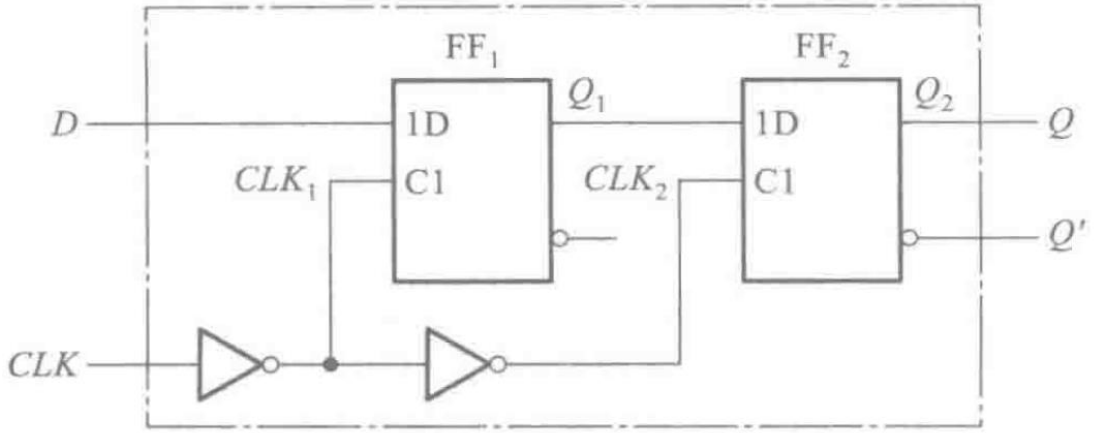
- When *CLK*=1, the output of the master stage can only change once. This is different from the S-R flip flop.

Can we build the button now?

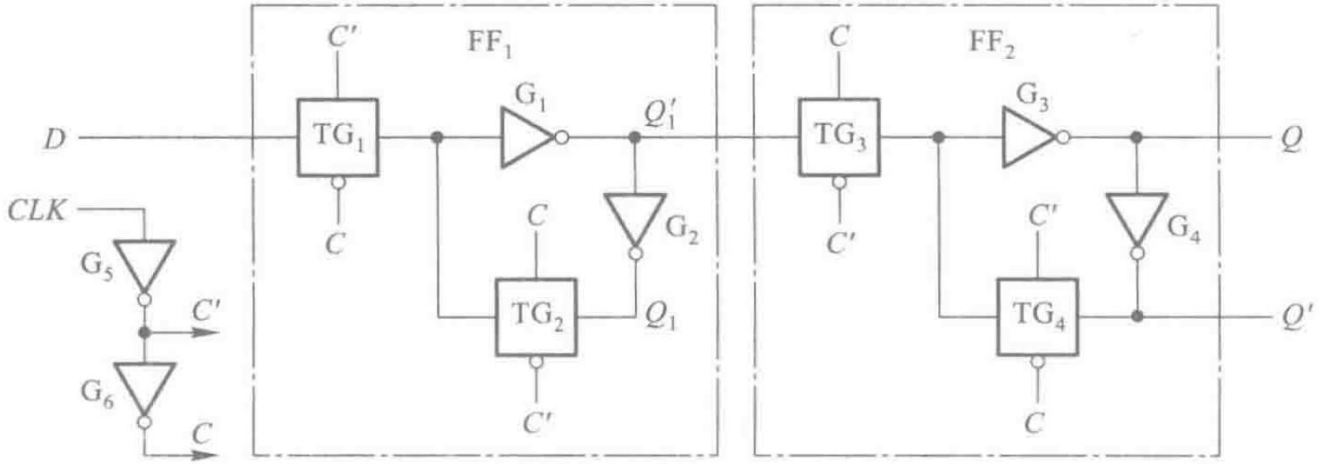


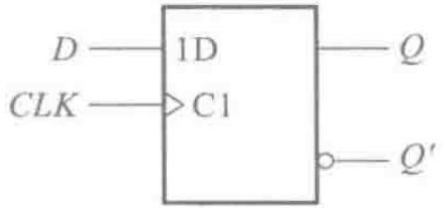


Edge Trigger Flip-Flops



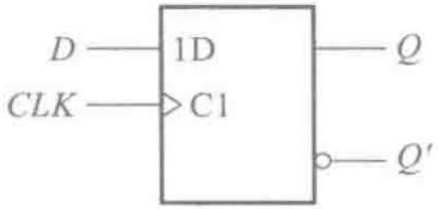
CLK	D	Q	Q*
×	×	×	Q
↑	0	0	0
↑	0	1	0
↑	1	0	1
↑	1	1	1

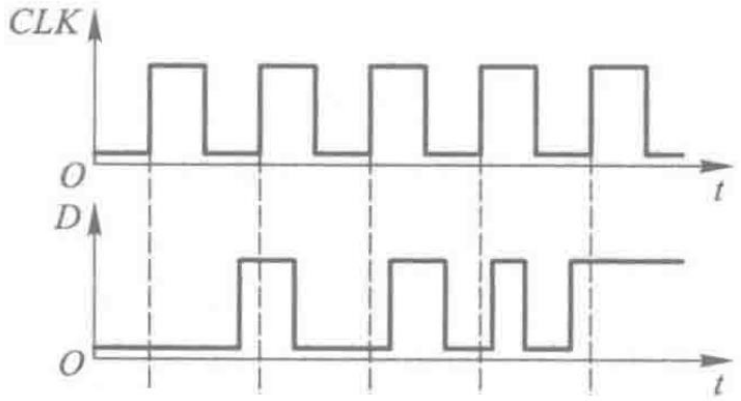




- To improve the noise tolerance, it is desired to have an edge trigger FF rather than the pulse trigger FF.
- “>” denotes the edge trigger
- Triggered at the rising edge

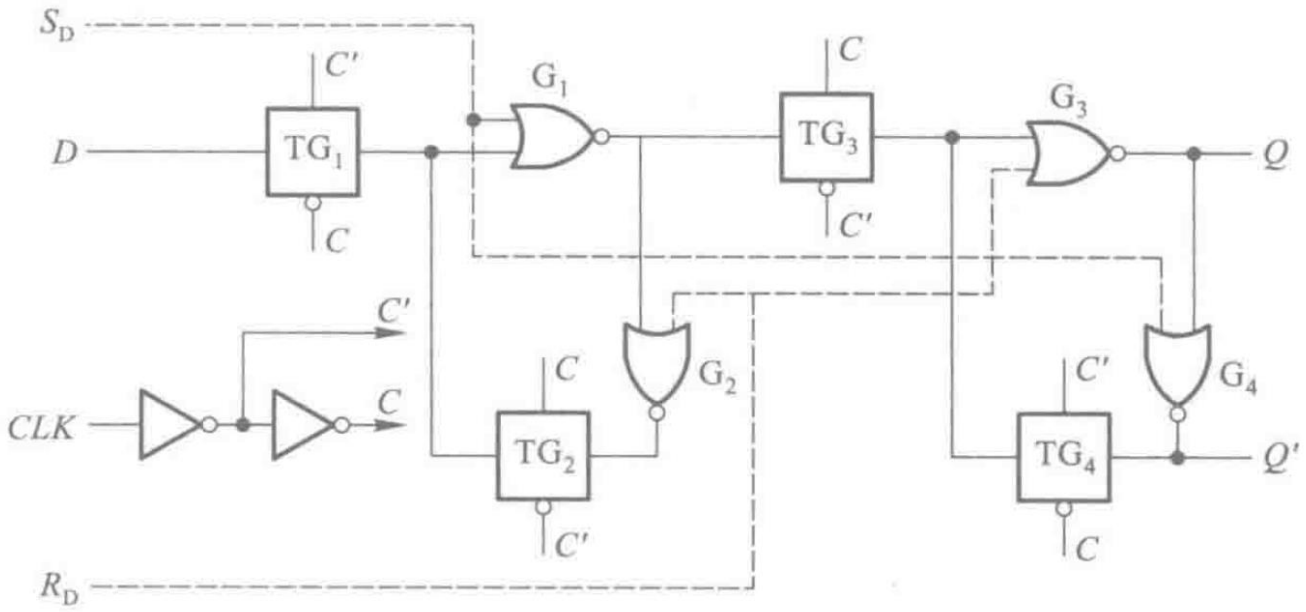
Edge Trigger Flip-Flops





Question: plot the waveform of *Q*, assume the initial *Q* is 0

The asynchronous Edge Trigger Flip-Flops



- The asynchronous set or reset should apply to both the master and slave stage

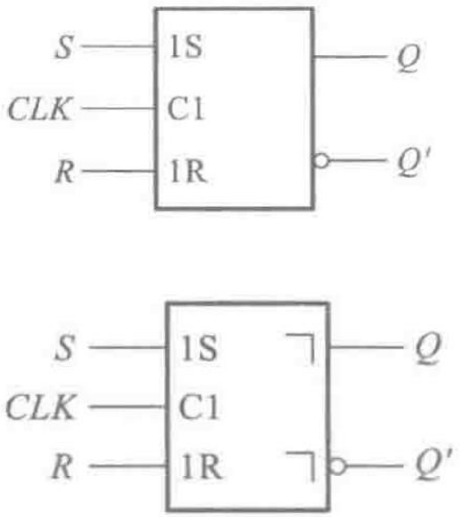
Content

Classification based on the functionality

Timing analysis

S-R Flip-Flops

S	R	Q	Q^*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	不定
1	1	1	不定

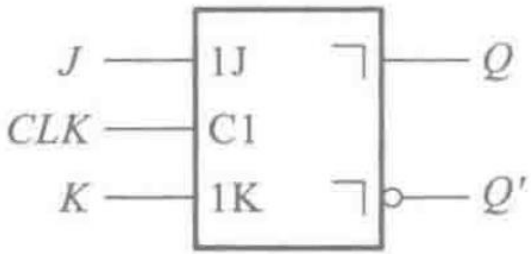


$$\begin{cases} Q^* = S'R'Q + SR'Q' + SR'Q = SR' + S'R'Q \\ SR = 0 \quad \text{（约束条件）} \end{cases}$$

$$\begin{cases} Q^* = S + R'Q \\ SR = 0 \quad \text{（约束条件）} \end{cases}$$

J-K Flip-Flops

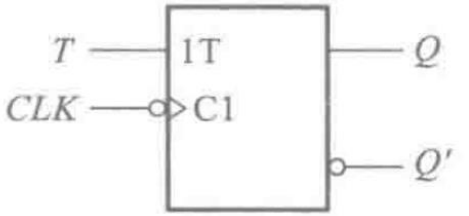
J	K	Q	Q^*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



$$Q^* = JQ' + K'Q$$

T Flip-Flops

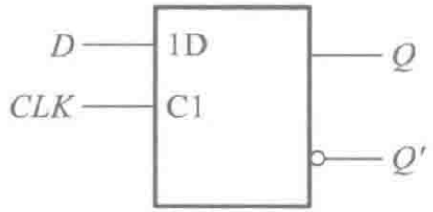
T	Q	Q^*
0	0	0
0	1	1
1	0	1
1	1	0

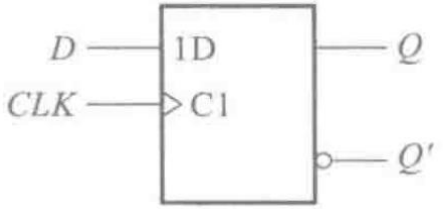


$$Q^* = TQ' + T'Q$$

D Flip-Flops

D	Q	Q^*
0	0	0
0	1	0
1	0	1
1	1	1





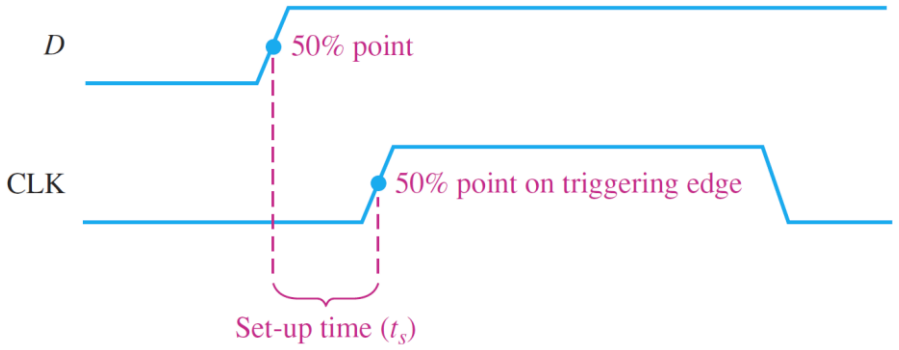
$$Q^* = D$$

Content

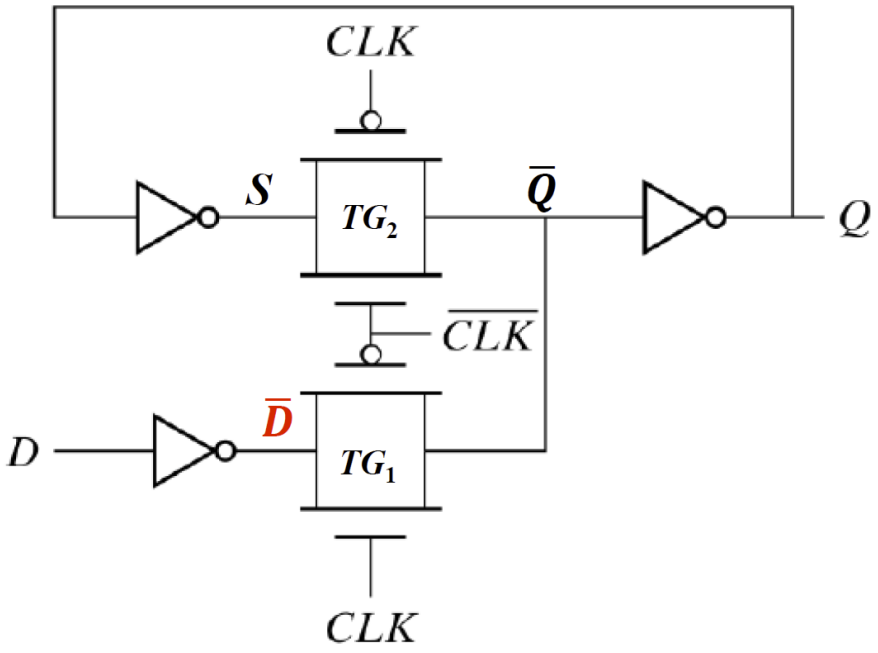
Classification based on the functionality

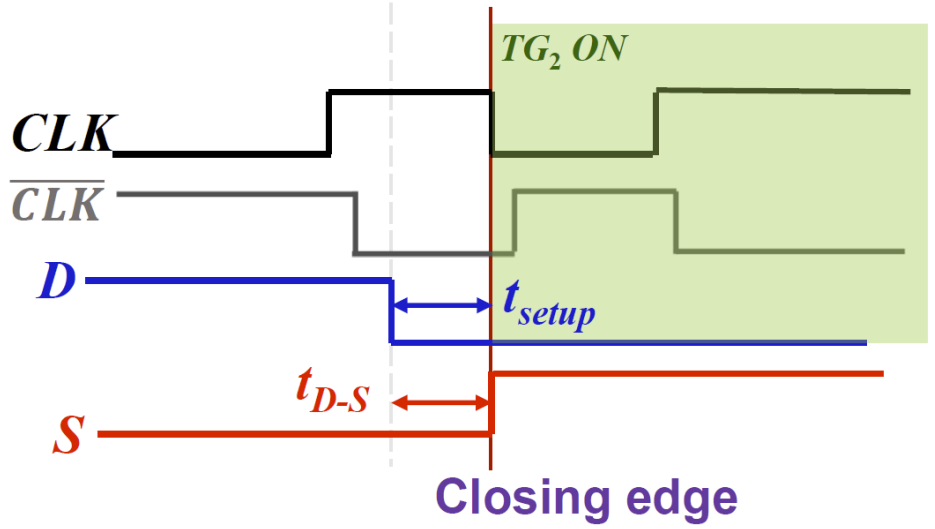
Timing analysis

Setup time



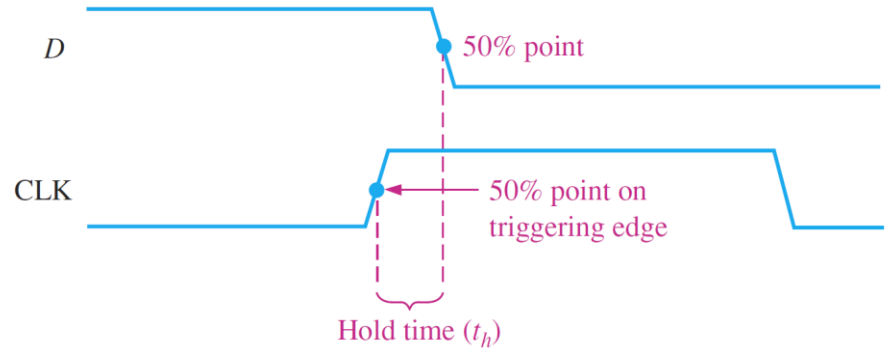
- Set-up time t_{su} is the minimum interval required for the logic levels to be maintained prior to the triggering edge of CLK



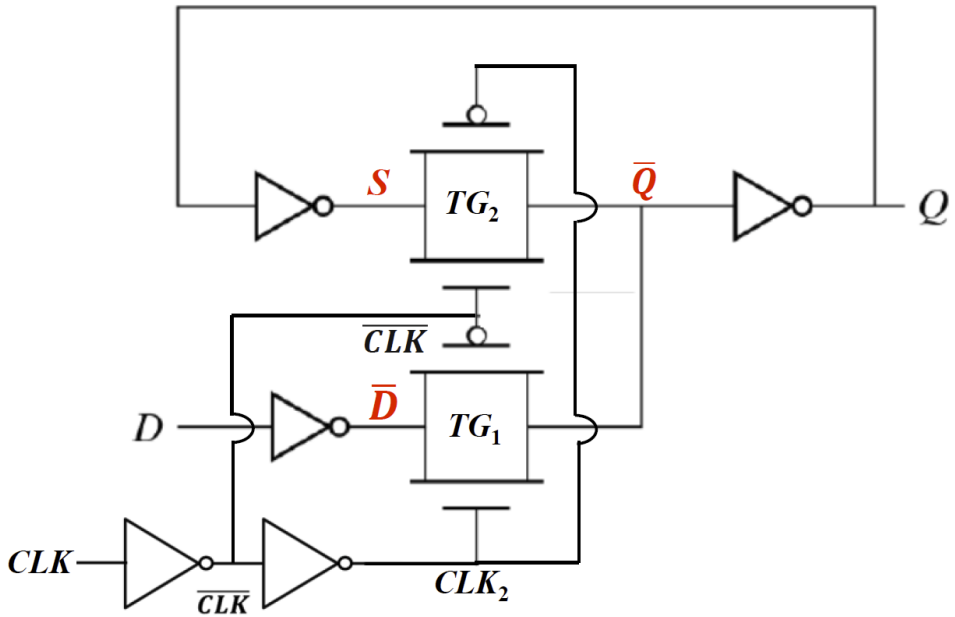


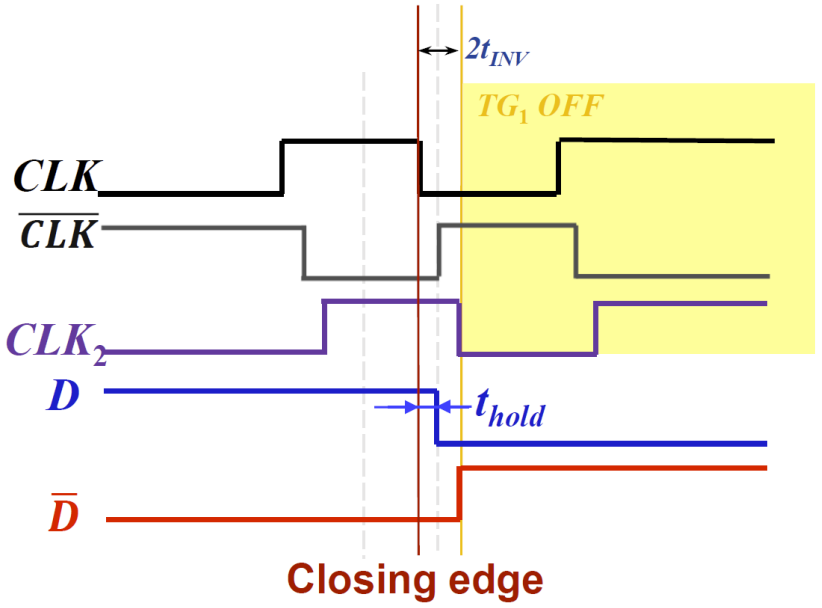
$t_{su} = t_{TG1} + 3t_{INV}$

Hold time



- Hold time t_h is the minimum interval required for the logic levels to be maintained after to the triggering edge of CLK

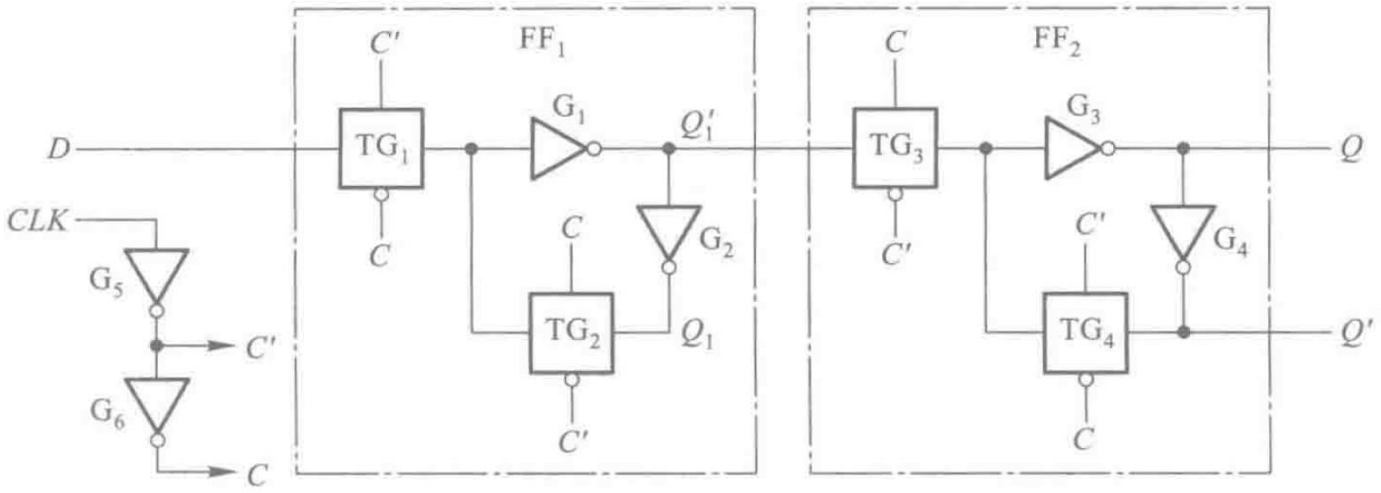


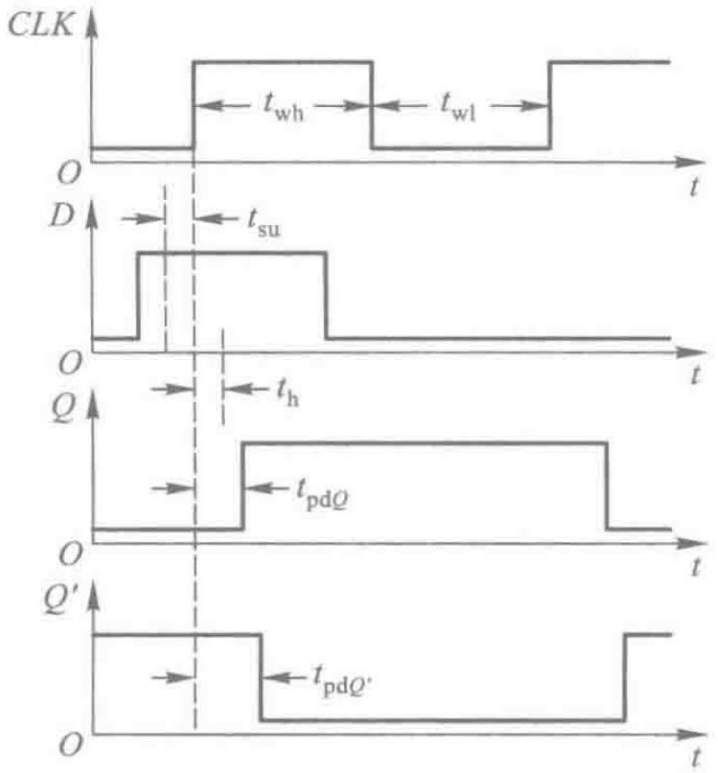


$t_h = t_{INV}$

Setup time and hold time

- Assume the propagation delay of both the inverter and transmission gate is t_d





$t_{su} = 2t_{INV} + t_{TG} - t_{INV} = t_{INV} + t_{TG}$

$t_h = 2t_{INV}$