Content

Semiconductor

PN Junction

MOSFET & Advanced FET

CMOS Inverter

Classification of Solids

Metal

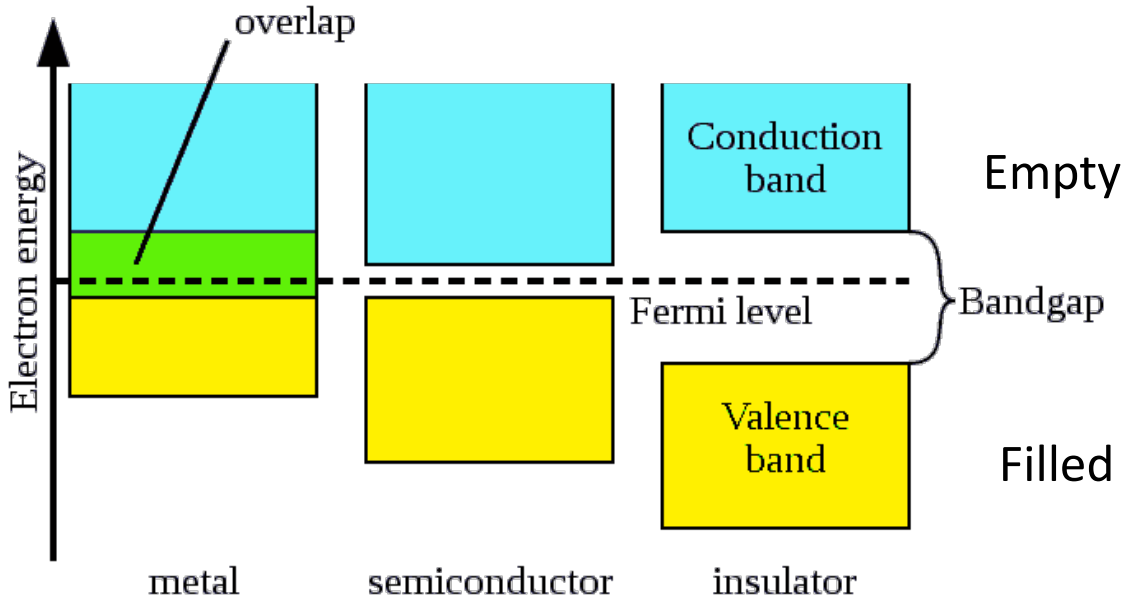
Current cannot be controlled
Always ON

Semiconductor

Controlled conduction

Insulator

No conduction at all!
Always OFF



Empty (i.e., no electrons)

Filled with electrons

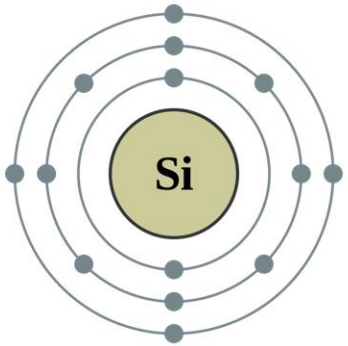
Periodic table

PERIODIC TABLE

GROUP I	II										III	IV	V	VI	VII	0
1 **H** Hydrogen 1.00794																2 **He** Helium 4.0026
3 **Li** Lithium 6.941	4 **Be** Beryllium 9.0122										5 **B** Boron 10.81	6 **C** Carbon 12.011	7 **N** Nitrogen 14.0067	8 **O** Oxygen 15.9994	9 **F** Fluorine 18.998	10 **Ne** Neon 20.179
11 **Na** Sodium 22.9898	12 **Mg** Magnesium 24.305										13 **Al** Aluminium 26.9815	14 **Si** Silicon 28.086	15 **P** Phosphorus 30.9738	16 **S** Sulphur 32.06	17 **Cl** Chlorine 35.453	18 **Ar** Argon 39.948
19 **K** Potassium 39.098	20 **Ca** Calcium 40.06	21 **Sc** Scandium 44.956	22 **Ti** Titanium 47.90	23 **V** Vanadium 50.941	24 **Cr** Chromium 51.996	25 **Mn** Manganese 54.9380	26 **Fe** Iron 55.847	27 **Co** Cobalt 58.9332	28 **Ni** Nickel 58.70	29 **Cu** Copper 63.546	30 **Zn** Zinc 65.38	31 **Ga** Gallium 69.72	32 **Ge** Germanium 72.59	33 **As** Arsenic 74.9216	34 **Se** Selenium 78.96	35 **Br** Bromine 79.904	36 **Kr** Krypton 83.80
37 **Rb** Rubidium 85.4678	38 **Sr** Strontium 87.62	39 **Y** Yttrium 88.906	40 **Zr** Zirconium 91.22	41 **Nb** Niobium 92.906	42 **Mo** Molybdenum 95.94	43 **Tc** Technetium [97]	44 **Ru** Ruthenium 101.07	45 **Rh** Rhodium 102.905	46 **Pd** Palladium 106.4	47 **Ag** Silver 107.868	48 **Cd** Cadmium 112.40	49 **In** Indium 114.82	50 **Sn** Tin 118.69	51 **Sb** Antimony 121.75	52 **Te** Tellurium 127.75	53 **I** Iodine 126.9045	54 **Xe** Xenon 131.30
55 **Cs** Caesium 132.905	56 **Ba** Barium 137.34	57–71 Lanthanide Series	72 **Hf** Hafnium 178.49	73 **Ta** Tantalum 180.948	74 **W** Tungsten 183.85	75 **Re** Rhenium 186.207	76 **Os** Osmium 190.2	77 **Ir** Iridium 192.22	78 **Pt** Platinum 195.09	79 **Au** Gold 196.9665	80 **Hg** Mercury 200.59	81 **Tl** Thallium 204.37	82 **Pb** Lead 207.2	83 **Bi** Bismuth 208.98	84 **Po** Polonium [209]	85 **At** Astatine [210]	86 **Rn** Radon [222]
87 **Fr** Francium [223]	88 **Ra** Radium [226]	89–103 Actinide Series	104 **Db** Dubnium [261]	105 **Hn**[§] Hahnium [262]	106 **Rf** Rutherfordium [263]	107 **Uns** Unnilseptium [262]	108 **Uno** Unniloctium [265]	109 **Une** Unnilenium [266]									
LANTHANIDE SERIES (rare earth elements)		57 **La** Lanthanum 138.9055	58 **Ce** Cerium 140.12	59 **Pr** Praseodymium 140.9077	60 **Nd** Neodymium 144.24	61 **Pm** Promethium [145]	62 **Sm** Samarium 150.36	63 **Eu** Europium 151.96	64 **Gd** Gadolinium 157.25	65 **Tb** Terbium 158.9254	66 **Dy** Dysprosium 162.50	67 **Ho** Holmium 164.9308	68 **Er** Erbium 167.26	69 **Tm** Thulium 168.9342	70 **Yb** Ytterbium 173.04	71 **Lu** Lutetium 174.97	
ACTINIDE SERIES (radioactive rare earth elements)		89 **Ac** Actinium [227]	90 **Th** Thorium 232.0381	91 **Pa** Protactinium 231.0359	92 **U** Uranium 238.029	93 **Np** Neptunium 237.0482	94 **Pu** Plutonium [244]	95 **Am** Americium [243]	96 **Cm** Curium [247]	97 **Bk** Berkelium [247]	98 **Cf** Californium [251]	99 **Es** Einsteinium [254]	100 **Fm** Fermium [257]	101 **Md** Mendelevium [256]	102 **No** Nobelium [254]	103 **Lr** Lawrencium [256]	

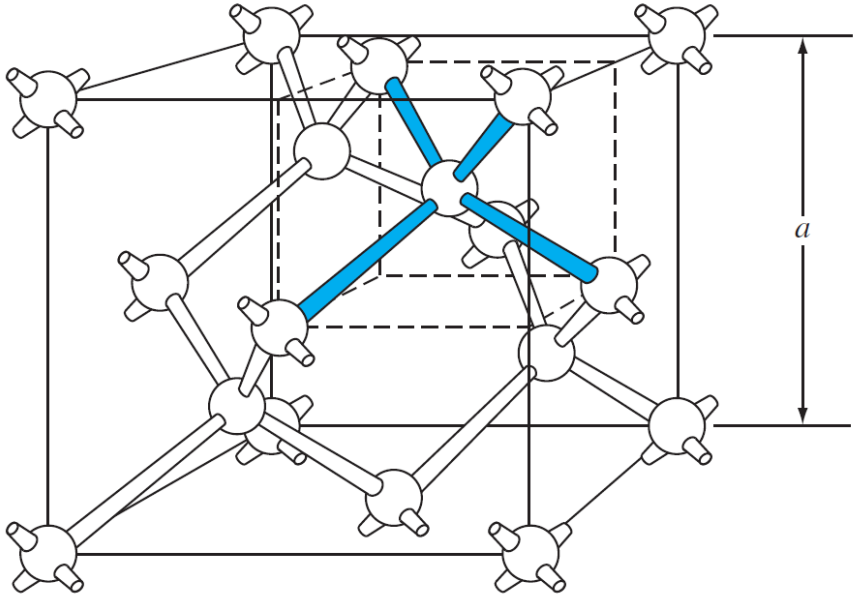
KEY
atomic number — 43
atomic symbol — Tc
name of element — Technetium
relative atomic mass — [97]
(most stable isotope in brackets)

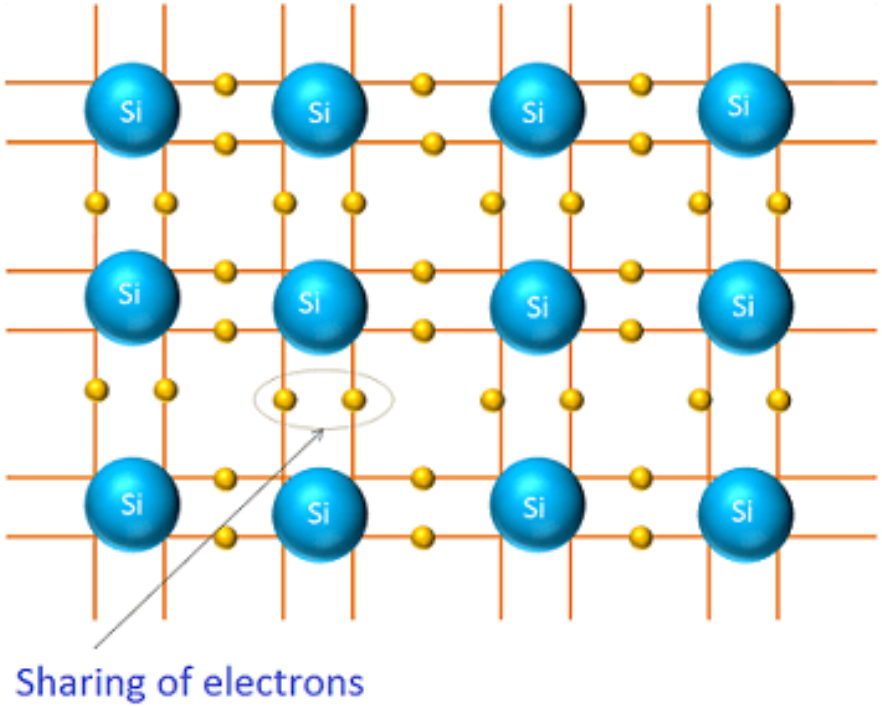
[§]Another proposed name is unnilpentium



2, 8, 4

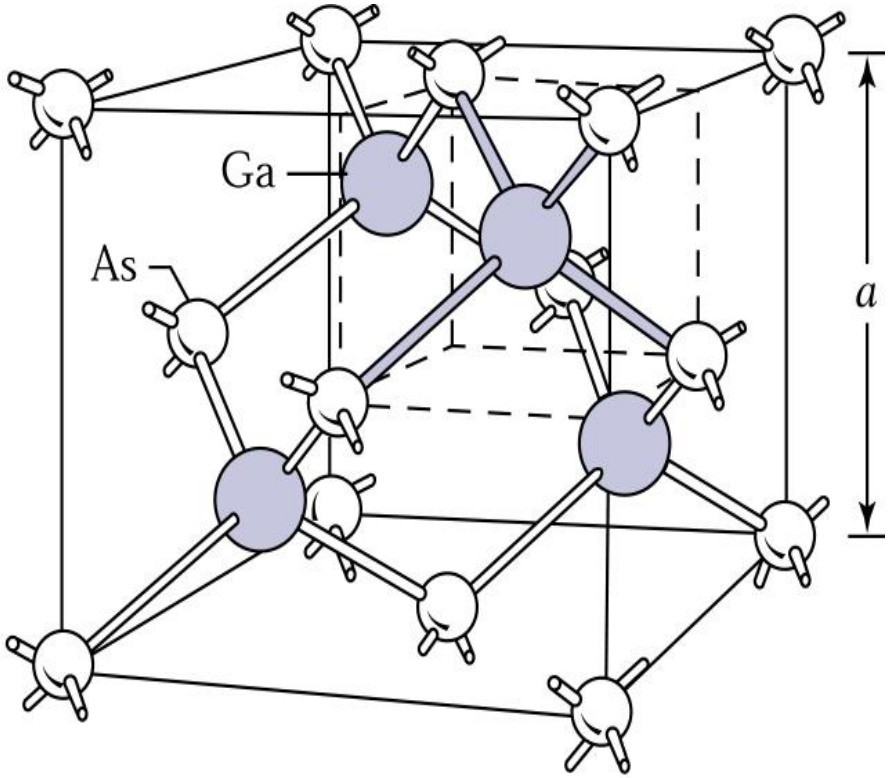
Crystal Structure: Si

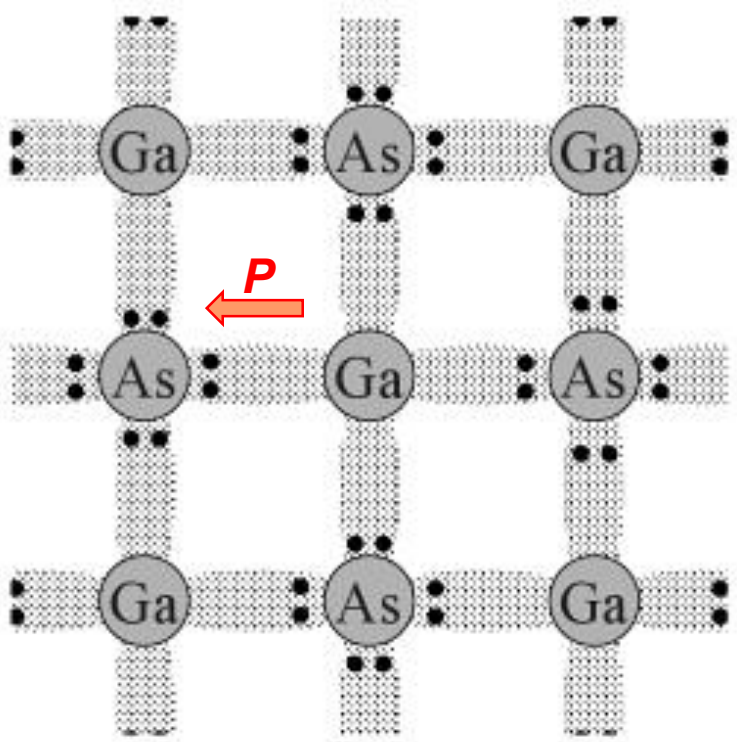




- Diamond Structure – Covalent Bonds.
- Si, Ge.
- Each atom has 4 nearest neighbors.
- When freed from a covalent bond, an electron leaves a hole behind

Crystal Structure: GaAs

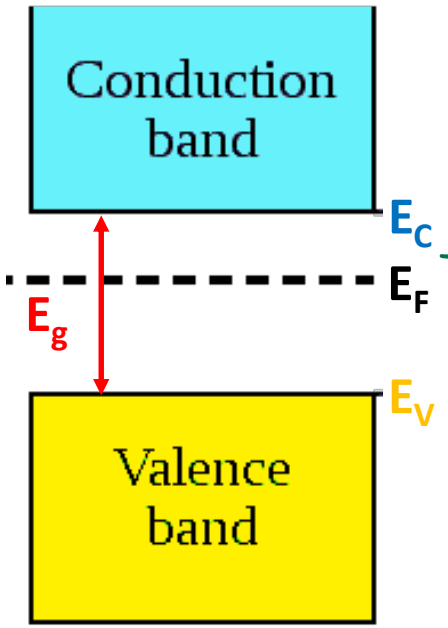




- Zinc-Blende Structure: Covalent + Ionic Bonds
- GaAs, InAs, InP, ZnTe, ZnSe, …

- Ga: group III
- As: group IV

Carrier Density of Semiconductor



- Free Electron Density $n = N_C e^{-\frac{E_C - E_F}{k_B T}}$
- Free Hole Density $p = N_V e^{-\frac{E_F - E_V}{k_B T}}$

E_F: Fermi level

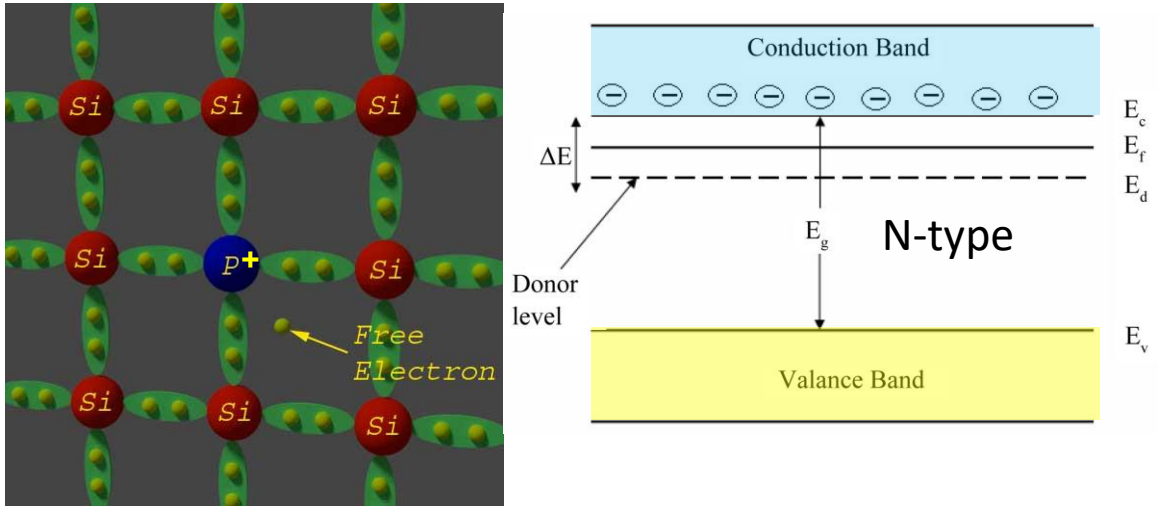
N_c: Effective density of states in conduction band

N_v: Effective density of states in valence band

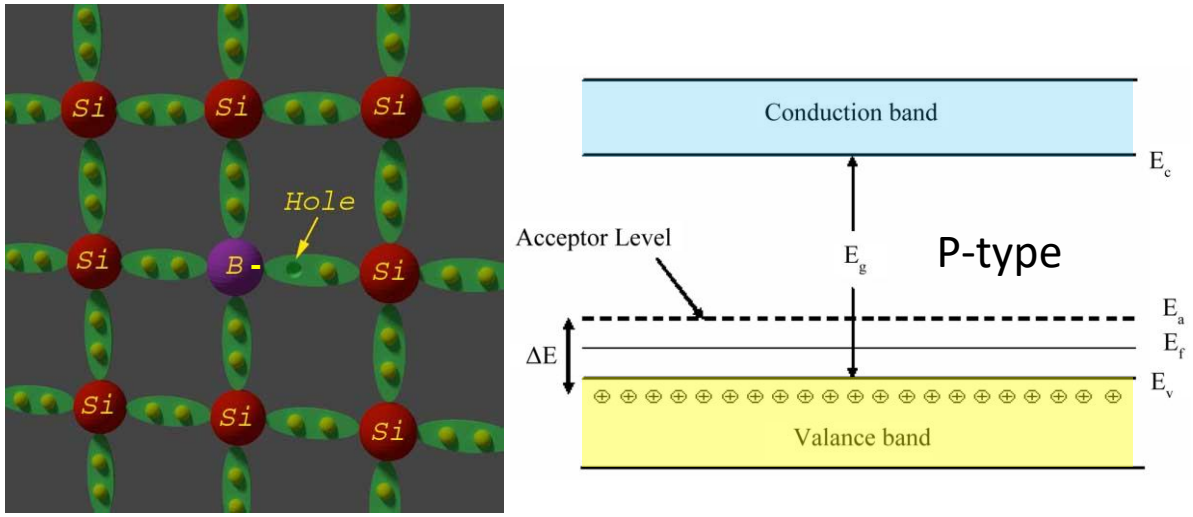
k_B: Boltzmann constant

Acceptor vs Donor

- Intrinsic(extrinsic) semiconductor: a material without(with) impurity atoms



Donor: an impurity easily donate an electron to the conduction band.



Acceptor: an impurity easily donate a hole to the valence band.

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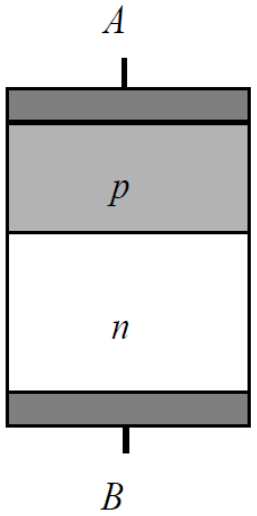
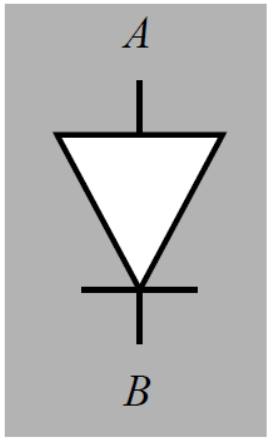
PN Junction (Diode)

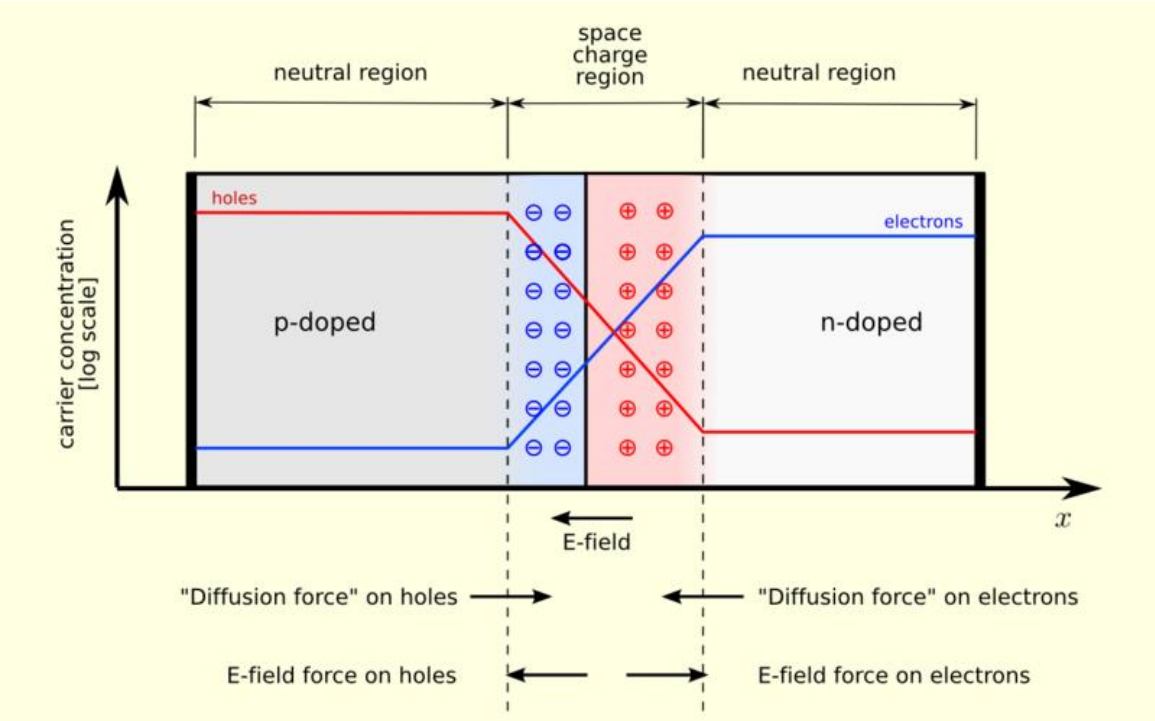


Schematics



Circuit symbol

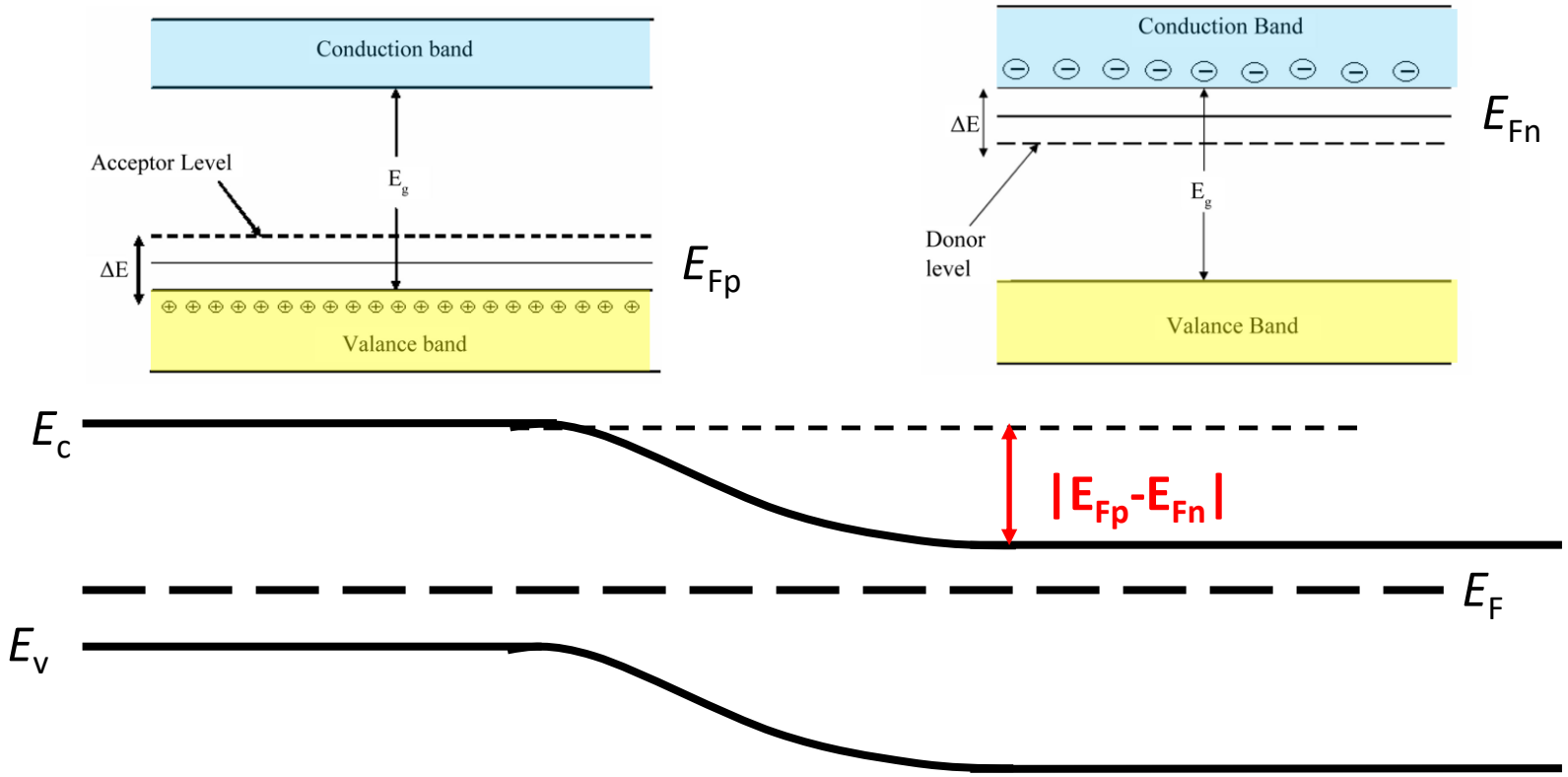
PN Junctions – Equilibrium

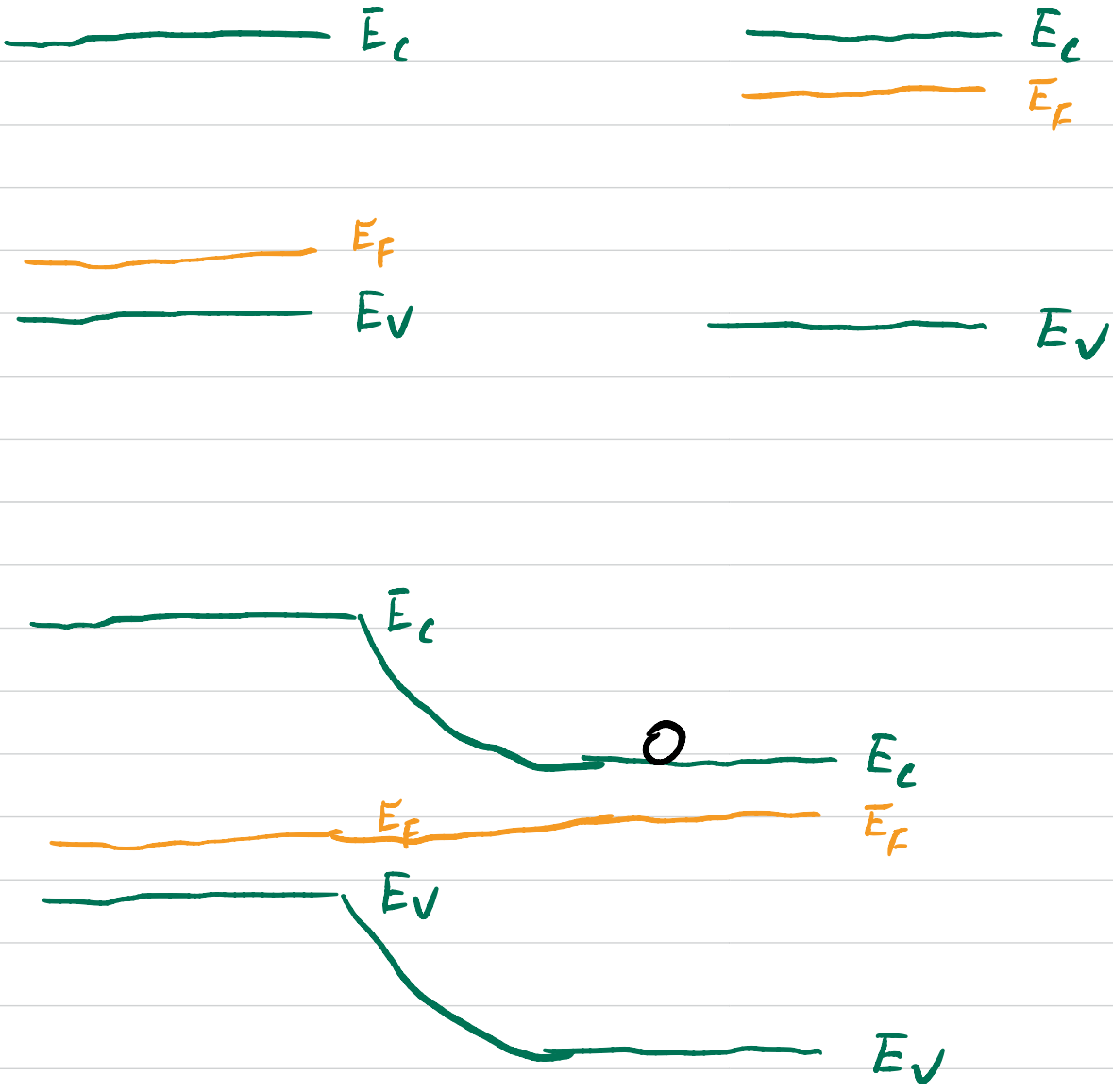


- As free electrons and holes diffuse across the junction, a region of fixed ions is left behind, known as the depletion region.

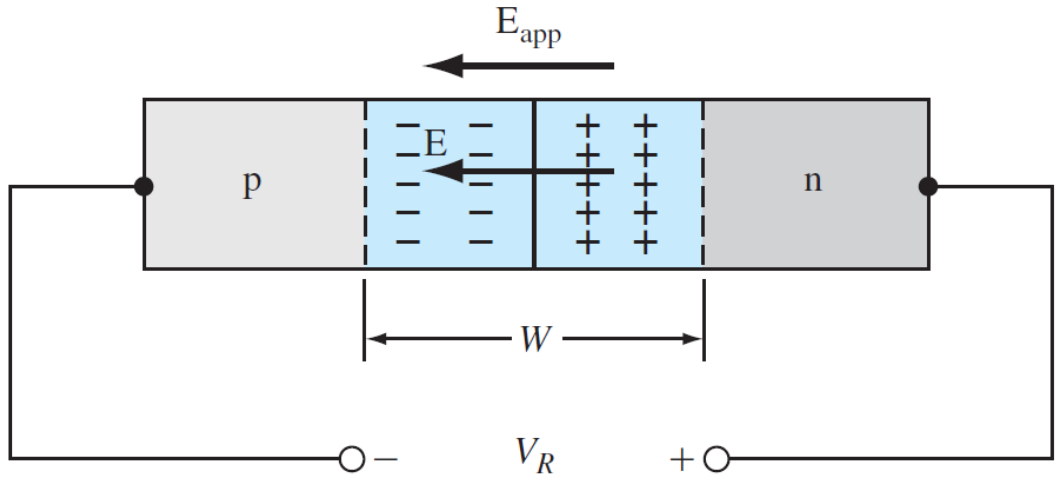
PN Junctions – Equilibrium

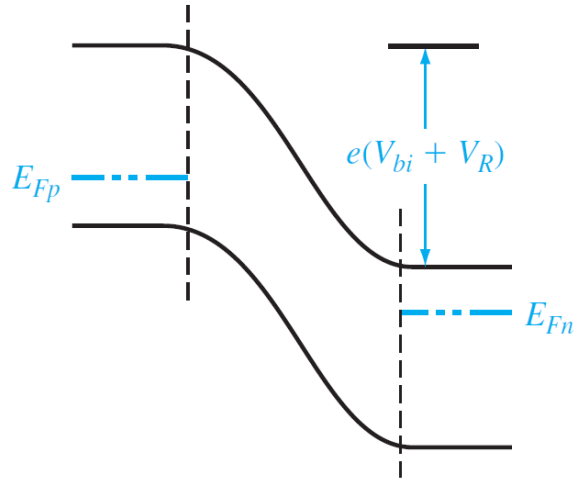
- E_F have to be the same at thermal equilibrium




E_c
E_c
E_f
E_f
E_v
E_v
E_c
E_c
E_f
E_f
E_v
E_v

Current Flow: Reverse Bias

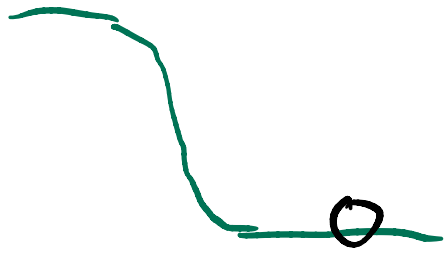




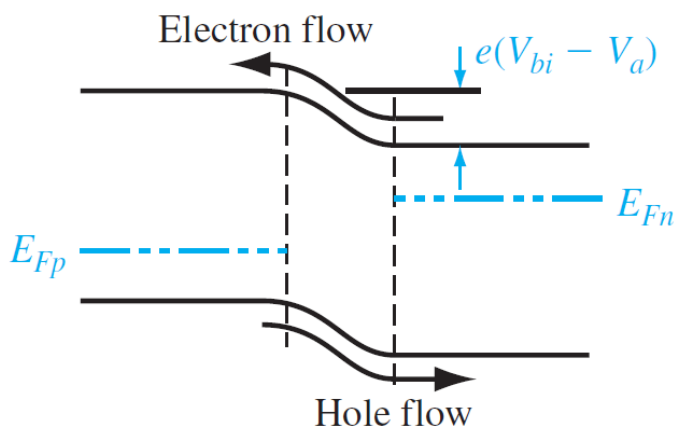
V = 0

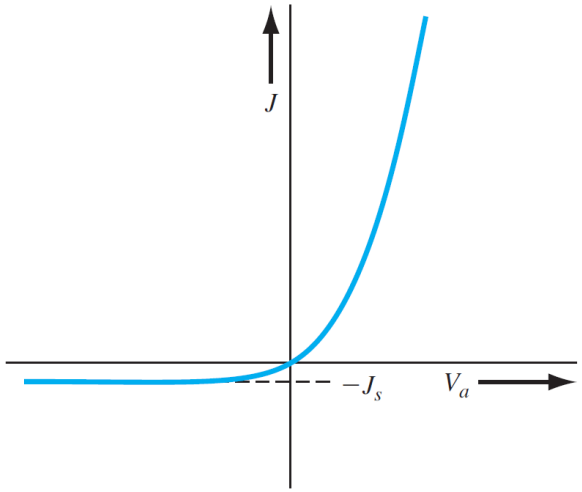
V = V_R

- Reverse bias: the n-type region is connected to a higher potential



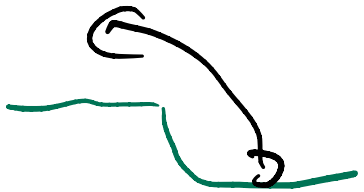
Current Flow: Forward Bias





$V = 0$

- Forward bias causes an exponential increase in the number of carriers which has sufficient energy to overcome the barrier.



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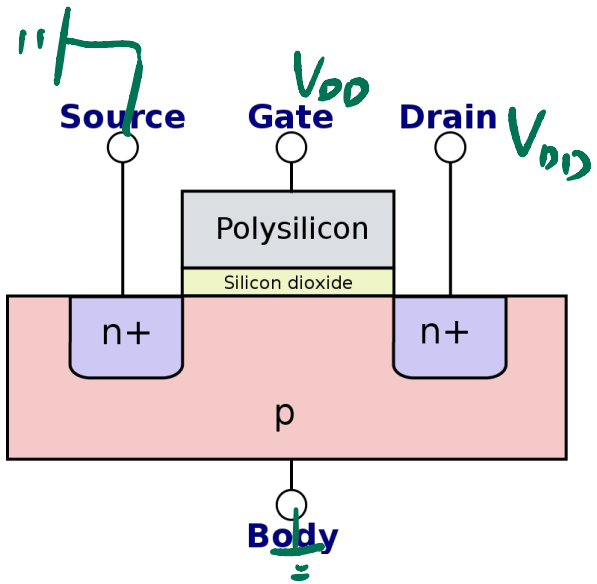
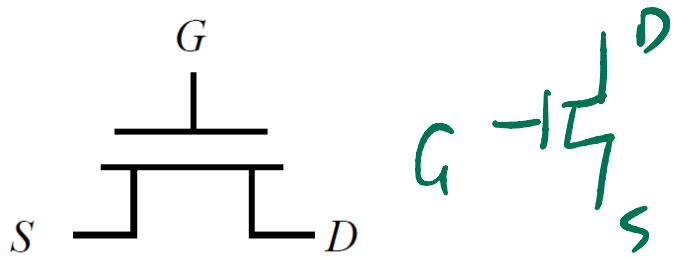
MOSFET & Advanced FET

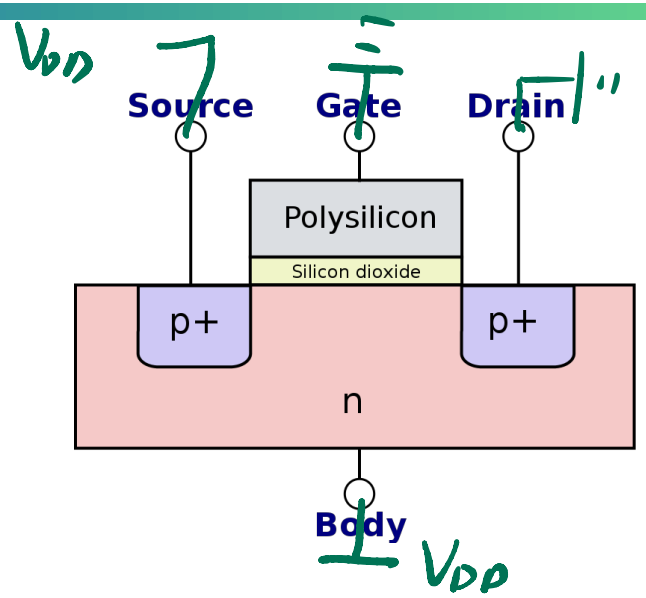
CMOS Inverter

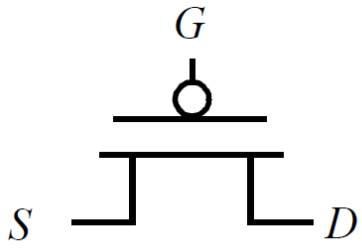
MOSFET





- NMOS
- Body connected to GND

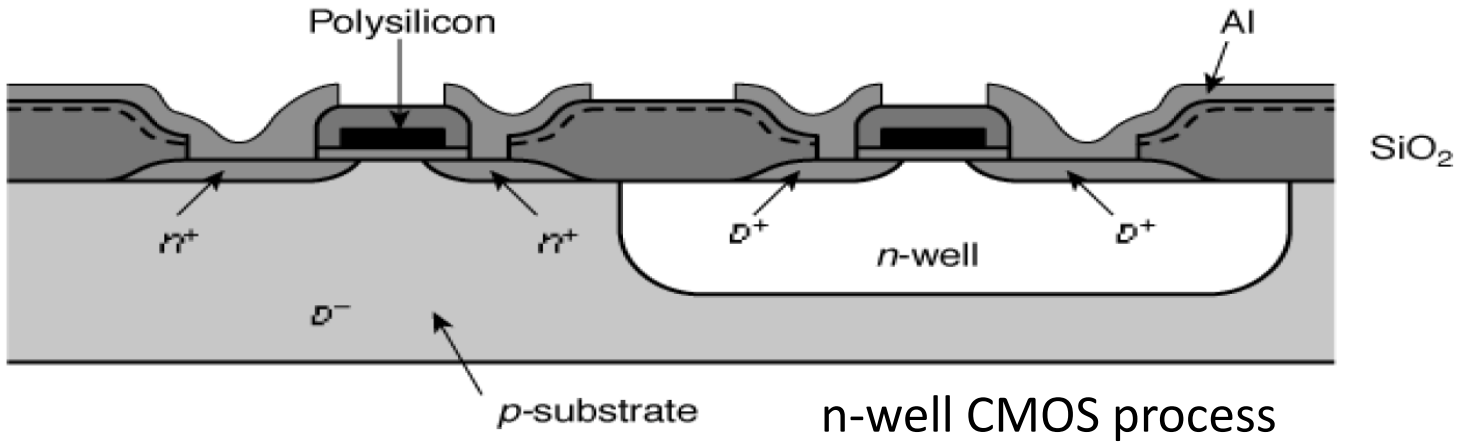




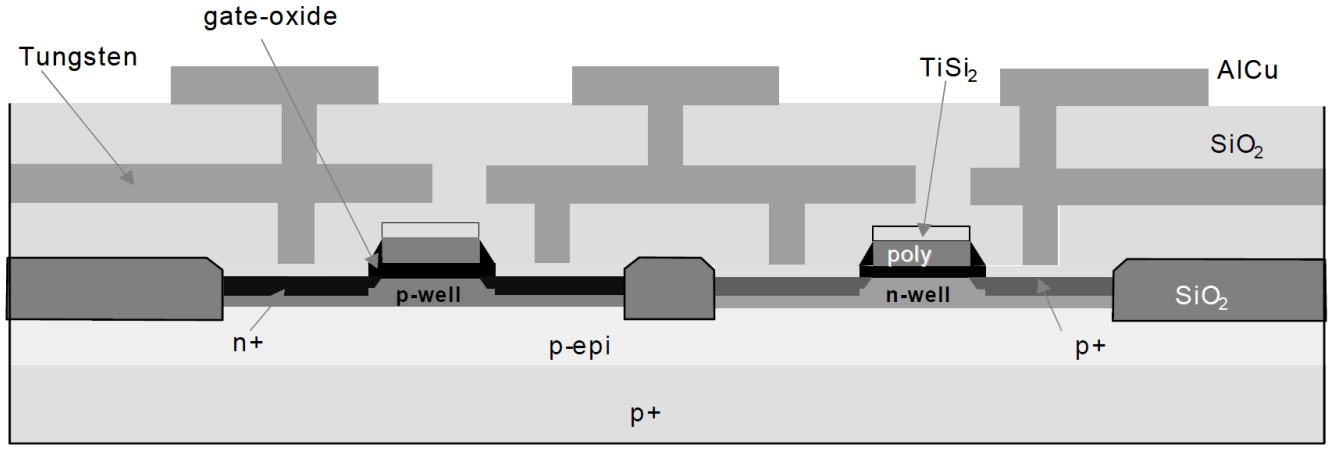
- PMOS
- Body connected to V_{DD}

Complementary MOS (CMOS)

- CMOS process requires that both NMOS and PMOS transistors be built in the same silicon material

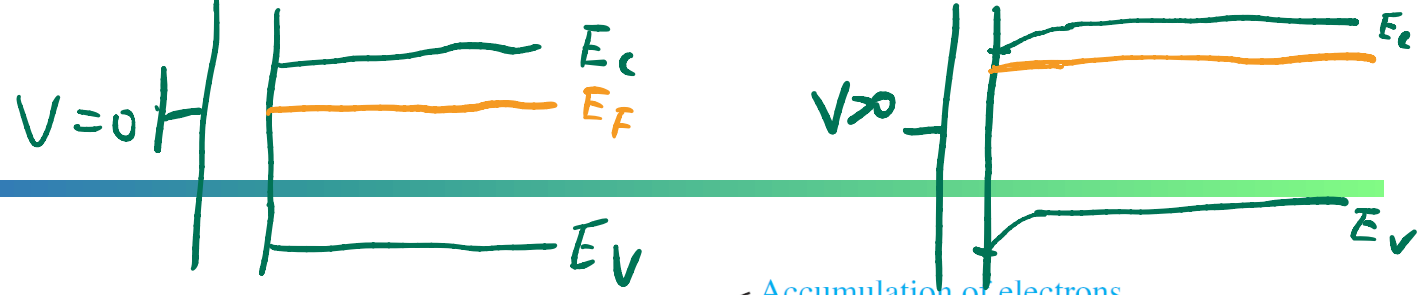


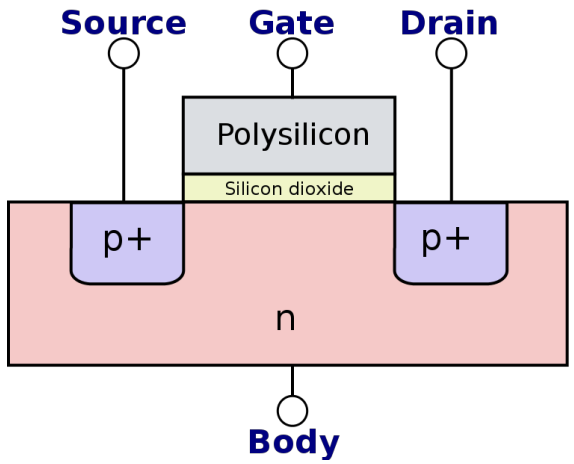
n-well CMOS process

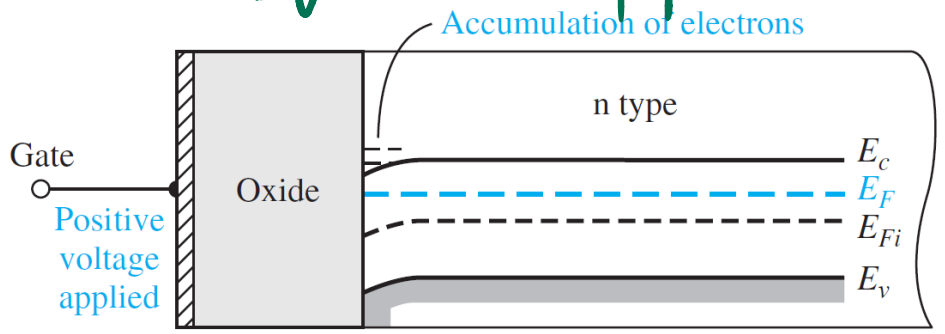


Dual-well CMOS process

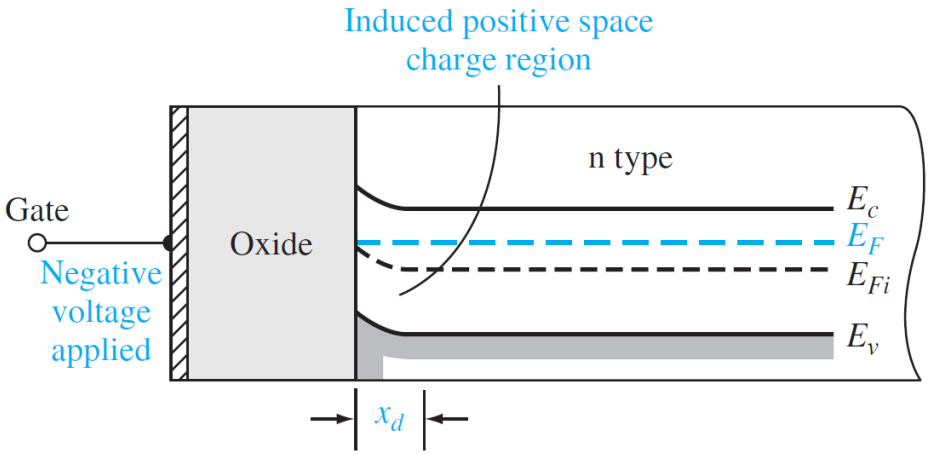
MOSFET under bias



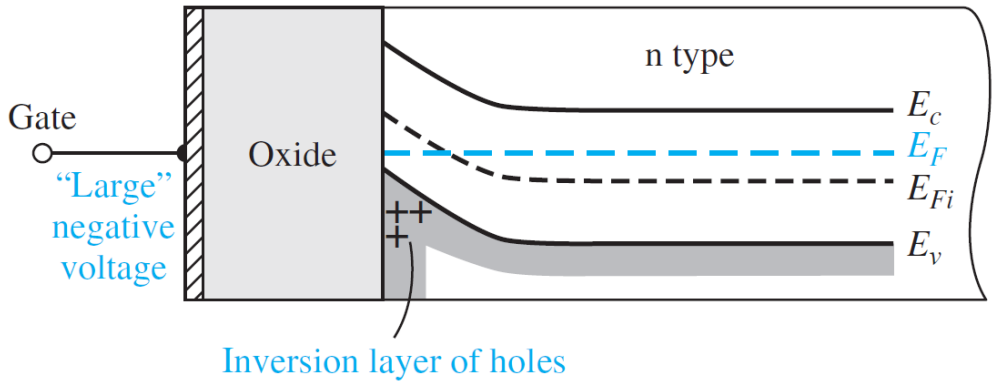




Accumulation

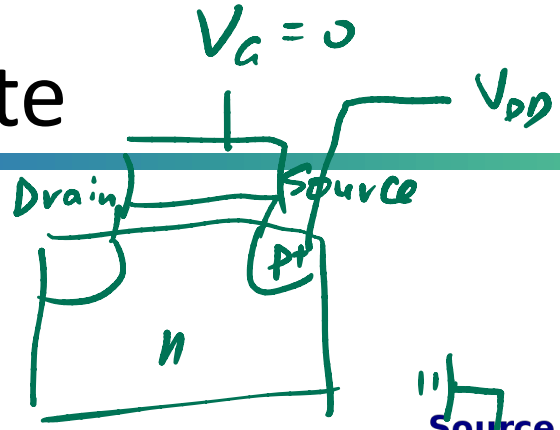


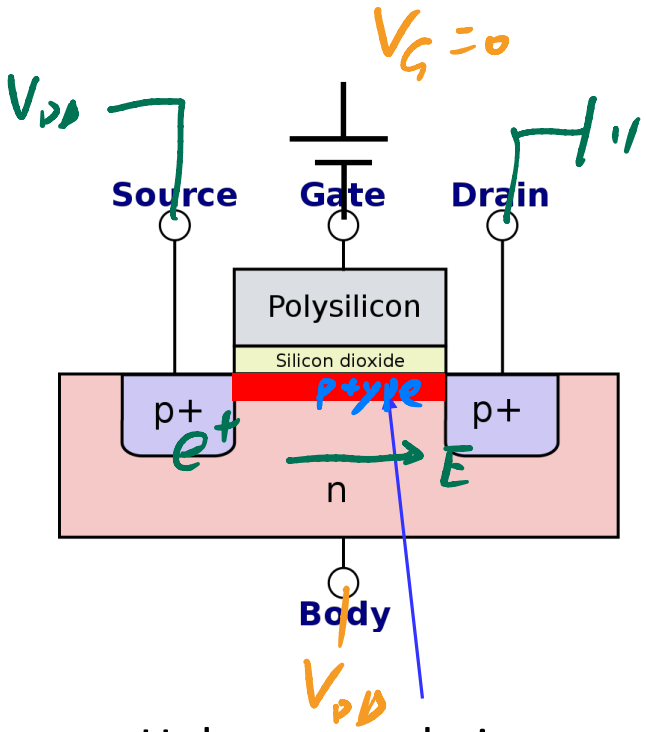
Depletion



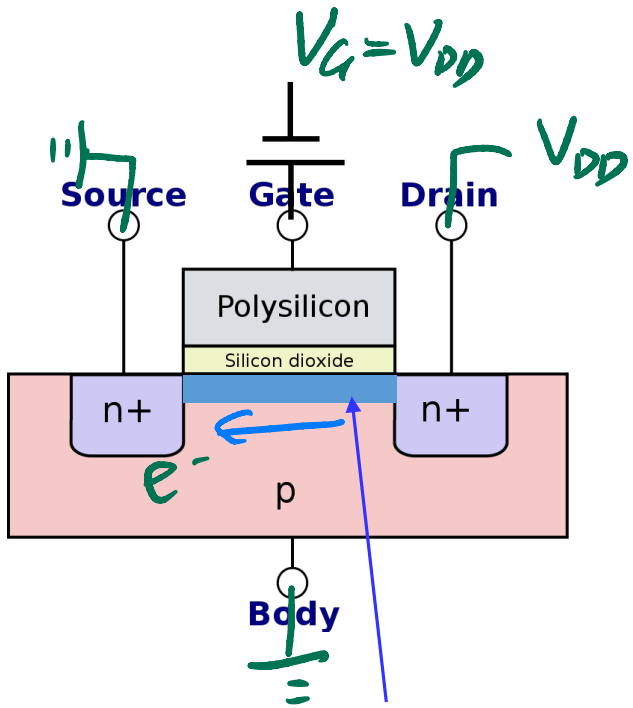
Inversion

MOSFET in the ON state



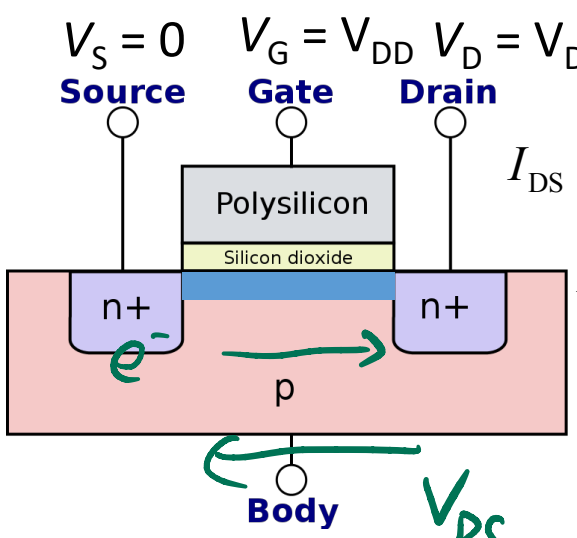


- Hole accumulation
- Hole can flow under $V_{DS} < 0$



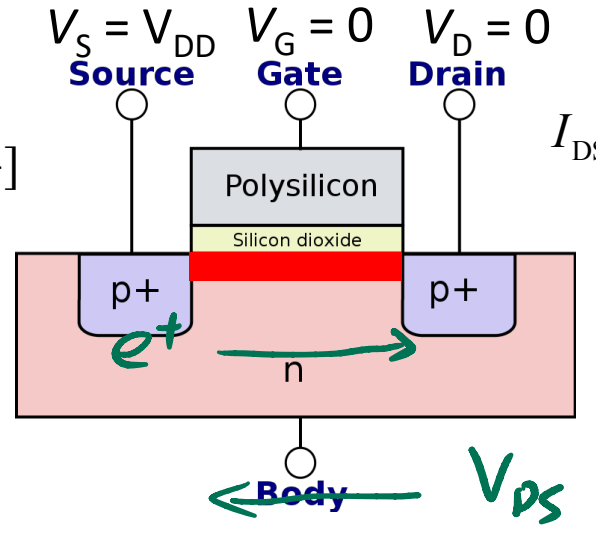
- Electron accumulation
- Electron can flow under $V_{DS} > 0$

MOSFET I-V



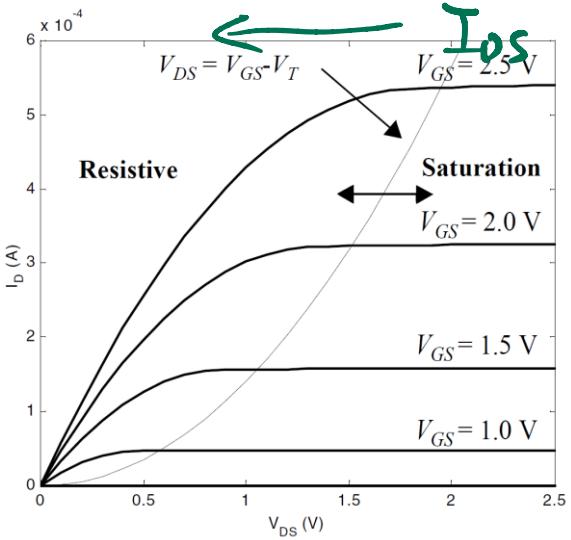
$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

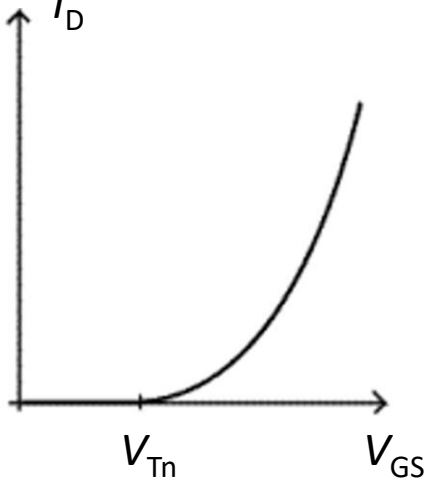
$$I_{DSAT} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

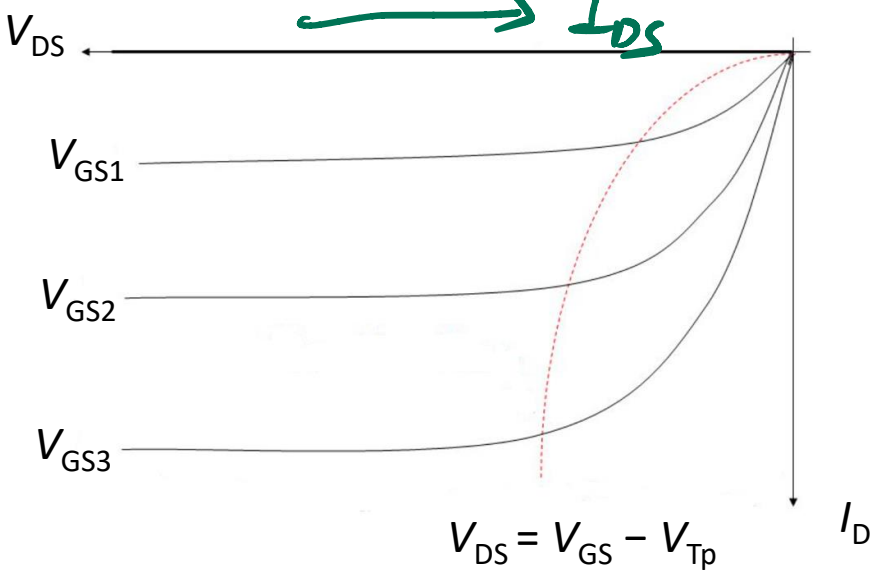


$$I_{DS} = -\mu_p C_{ox} \frac{W}{L}\left[(V_{GS} - V_{Tp})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

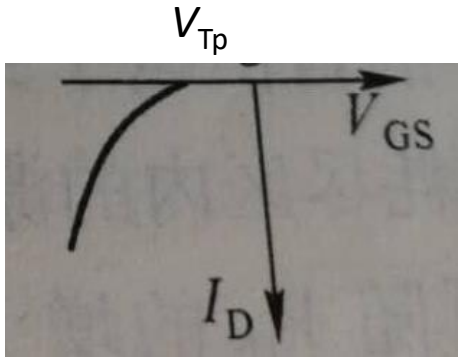
$$I_{DSAT} = -\frac{\mu_p C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{Tp})^2$$



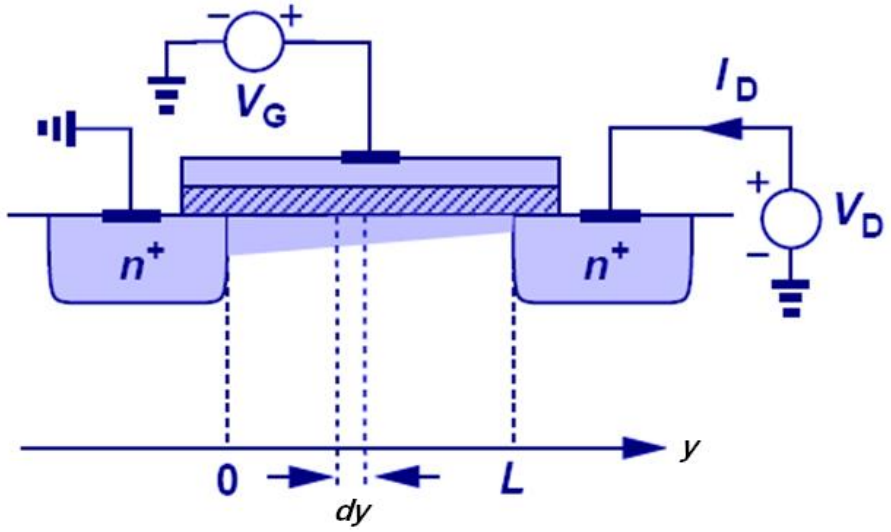




Note $V_{Tp} < 0$



Gradual Channel Model



- Gradual channel approximation: current only flow along the channel length.
- Let $Q_{inv}(y)$ be the total mobile electron charge at the position y of the surface inversion layer.
- $C_{ox} \equiv \varepsilon_{ox}/t_{ox}$: capacitance per unit area presented by the gate oxide

$$Q_{\text{inv}}(y) = C_{\text{ox}}[V_{\text{GS}} - V_{\text{T}} - V(y)]$$

- Drift current at y:

$$J(y) = -nev = -[Q_{\text{inv}}(y) / t_{\text{inv}}(y)] \cdot v(y)$$

$$I(y) = J(y)A(y) = J(y)Wt_{\text{inv}}(y) = -WQ_{\text{inv}}(y)v(y)$$

- Carrier drift velocity at y:

$$v = -\mu_{\text{n}} E = \mu_{\text{n}} dV(y) / dy$$

Gradual Channel Model

- Current Continuity Condition $I(y) \equiv I_{DS}$

$$I_{DS} = WQ_{\text{inv}}(y)v(y) = WQ_{\text{inv}}(y)\mu_n \frac{dV(y)}{dy} \quad \Rightarrow \quad I_{DS} = \mu_n WC_{ox}[V_{GS} - V_T - V(y)]dV(y)/dy$$

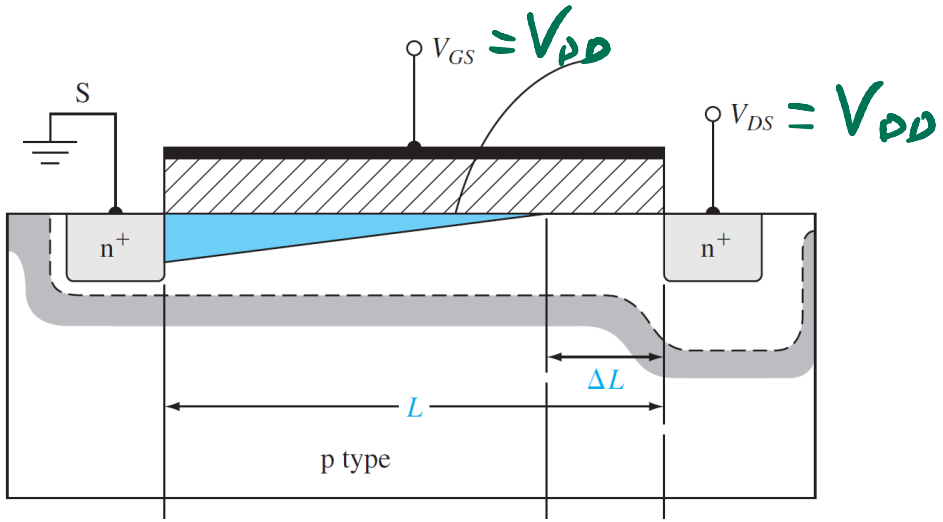
- Integrating from source to drain:

$$\int_0^L I_{DS}\,dy = \int_0^{V_{DS}} \mu_n WC_{ox}[V_{GS} - V_T - V(y)]dV(y)$$

- MOSFET Drain Current Equation ($V_{DS} < V_{GS} - V_T$)

$$I_{\text{DS}} = \mu_{\text{n}} C_{\text{ox}} \frac{W}{L}[(V_{\text{GS}} - V_{\text{T}})V_{\text{DS}} - \frac{V_{\text{DS}}^2}{2}]$$

What Happens when $V_{DS} = V_{GS} - V_T$?



$$Q_{inv}(L) = C_{ox}[V_{GS} - V_T - V(L)] = 0$$

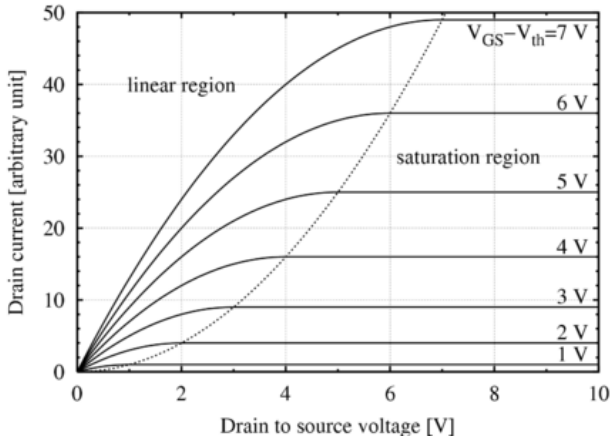
No inversion
(Pinch off)

- The free electrons in the channel are swept into the drain under the E field in the depletion region.
- The current does not increase anymore.

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$$

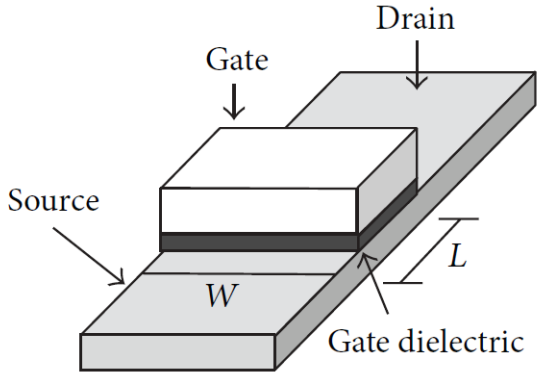
$$V_{DS} = V_{GS} - V_T$$

$$I_{DSAT} = \frac{\mu_n C_{ox}}{2} \frac{W}{L}(V_{GS} - V_T)^2$$

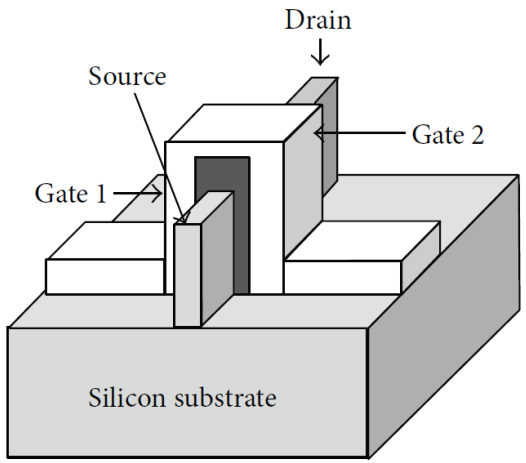


I_D is independent of V_{DS}

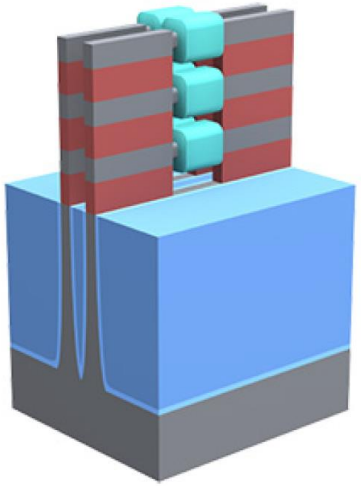
FinFET: 2D to 3D transistor



MOSFET



Trigate FinFET

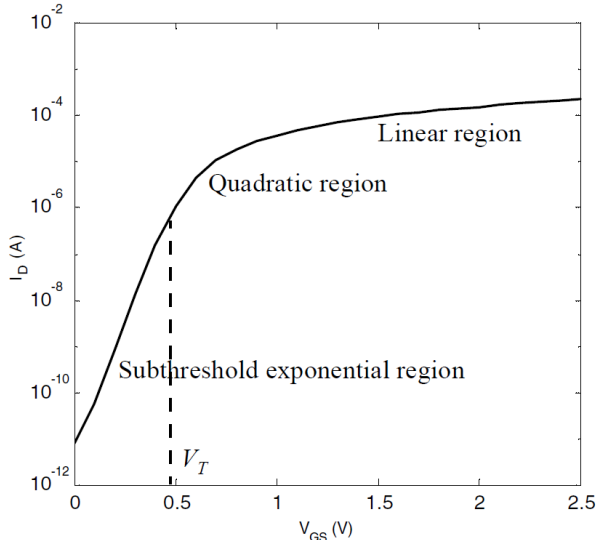


Gate all around (GAA) FinFET

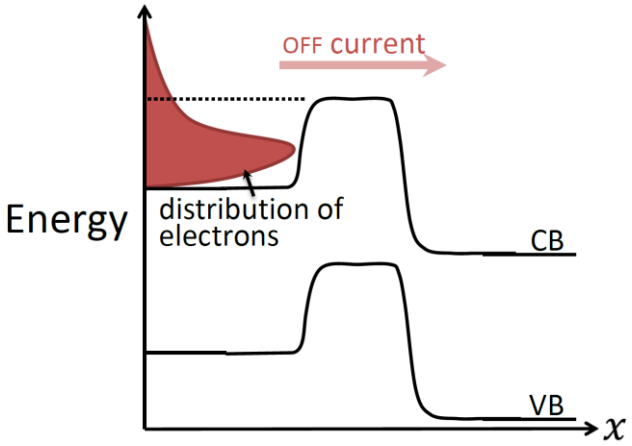
- A fin field-effect transistor (FinFET) is a multigate device built on a substrate where the gate is placed on two, three, or four sides of the channel or wrapped around the channel.
- It is the basis for modern nanoelectronic semiconductor device fabrication. Microchips utilizing FinFET gates first became commercialized in the first half of the 2010s, and became the dominant gate design at 14 nm, 10 nm and 7 nm process nodes.

- 2004, Samsung, 90 nm DRAM.
- 2011, Intel, 22 nm Tri-Gate FinFET used in Ivy Bridge microarchitecture.
- 2013, SK Hynix, 16 nm process
- 2017, TSMC, 7 nm process
- 2018, Samsung 5 nm

Subthreshold conduction

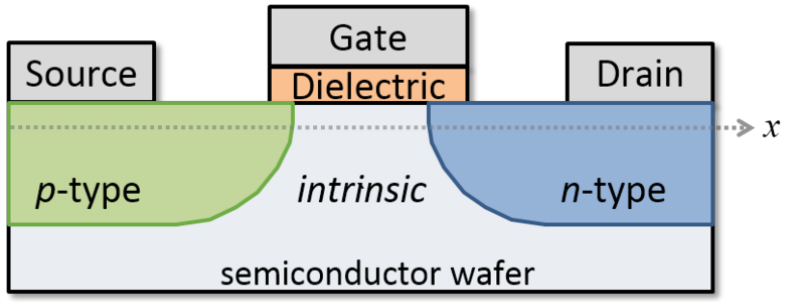


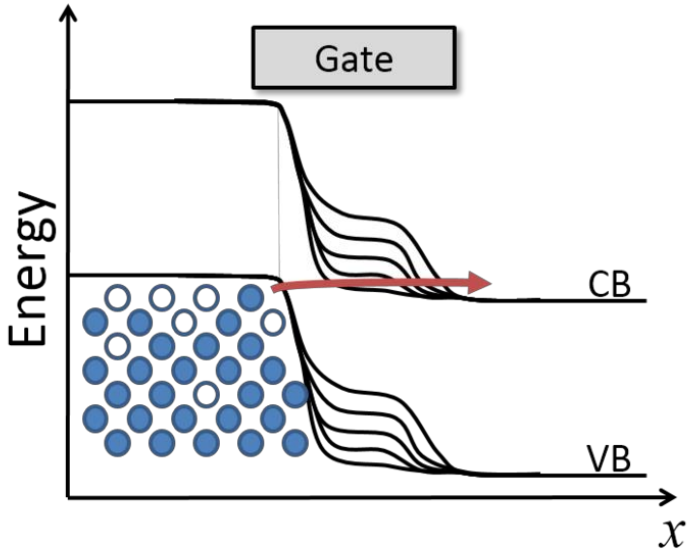
$$S = n\left(\frac{kT}{q}\right)\ln(10)$$



- The onset of strong inversion means that ample carriers are available for conduction, but by no means implies that no current at all can flow for $V_{GS} < V_T$.
- We would prefer the current drop as fast as possible once the V_{GS} falls below V_T. The slope factor S (mV/decade), which measures by how much V_{GS} has to be reduced for I_D to drop by a factor of 10.
- An ideal transistor has n = 1 and $(kT/q)\ln(10)$ evaluates to 60 mV/decade at room temperature. This value is limited by the thermal distribution of electrons (Boltzmann tyranny).

TFET

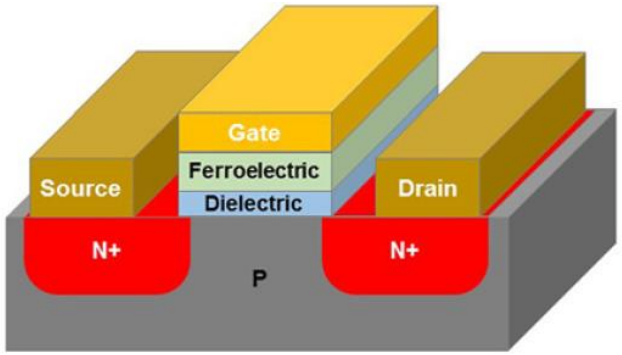


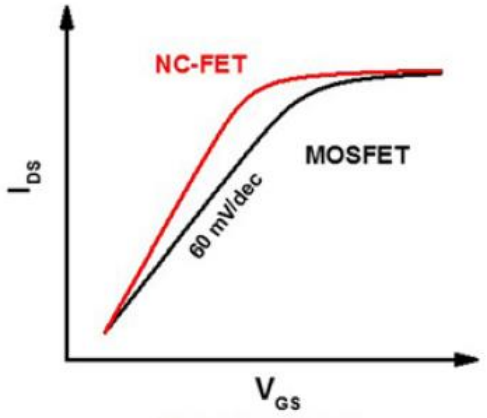


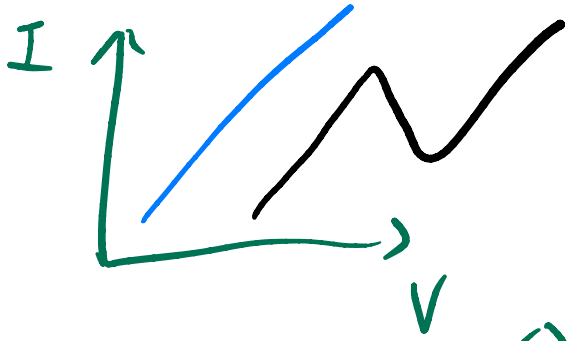
- The basic tunneling FET (TFET) structure is similar to a MOSFET except that the source and drain terminals of a TFET are doped of opposite types
- At sufficient gate bias, the conduction band of the intrinsic region aligns with the valence band of the P region. Electrons from the valence band of the p-type region tunnel into the conduction band of the intrinsic region and current can flow across the device.
- As the gate bias is reduced, the bands becomes misaligned and current can no longer flow.
- TFETs switch by modulating quantum tunneling through a barrier, thus they are not limited to 60 mV/decade of current at room temperature.

Negative capacitance FET

$R \cdot \frac{dV}{dI}$







$C = \frac{dQ}{dV}$

- A negative capacitance field-effect transistor (NC-FET) adds a thin-layer of ferroelectric (FE) material to the existing gate oxide of a MOSFET.
- By parallelly connecting FE layer and semiconductor channel, the change of surface potential $d\Psi_S$ can be larger than change of gate bias dV_G, making it possible to break the limitation of Boltzmann distribution.

Content

Semiconductor

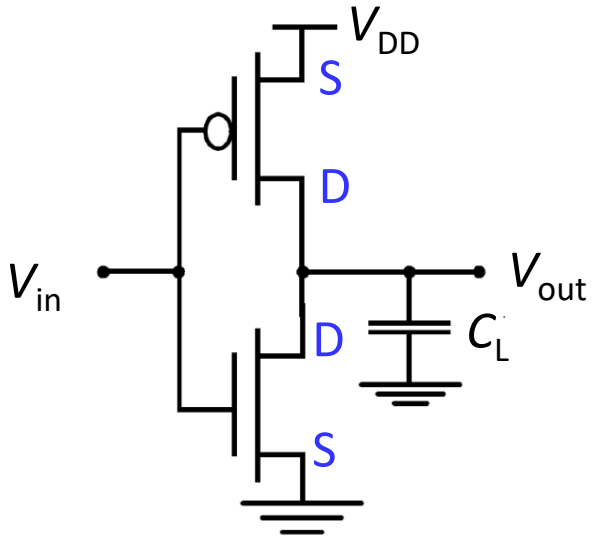
PN Junction

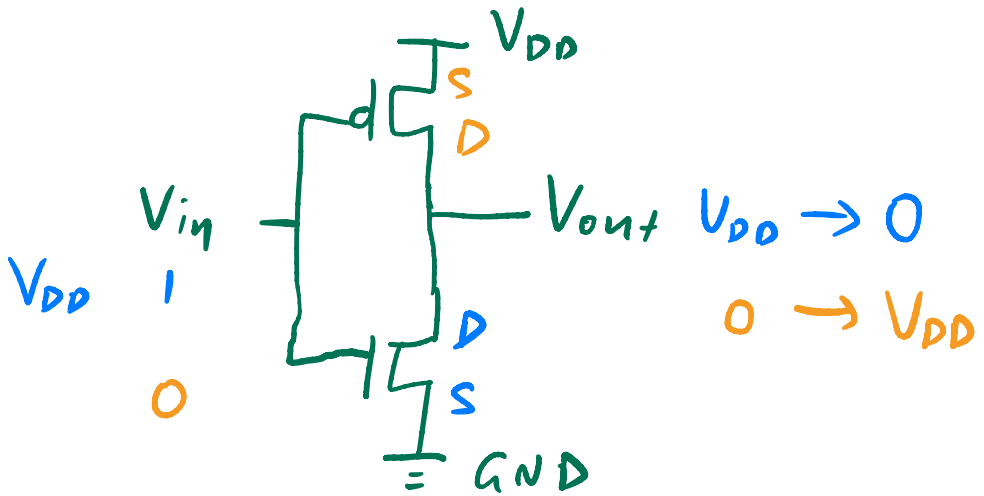
MOSFET

CMOS Inverter

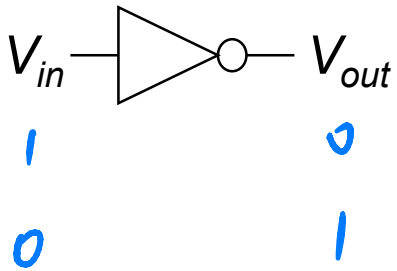
The CMOS Inverter

Schematic

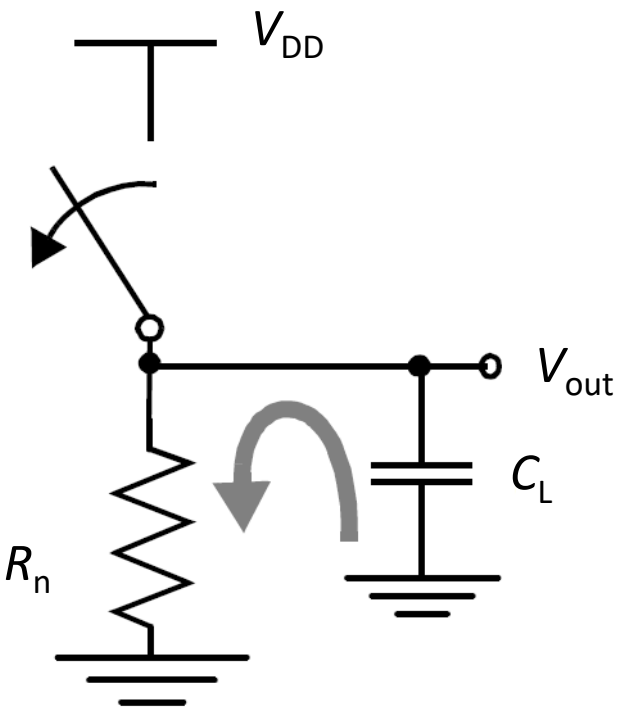




Symbol

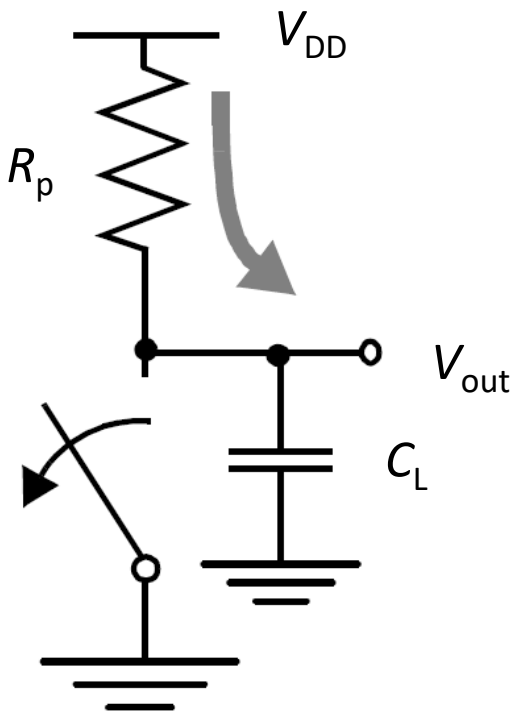


The CMOS Inverter



$V_{in} = V_{DD}$

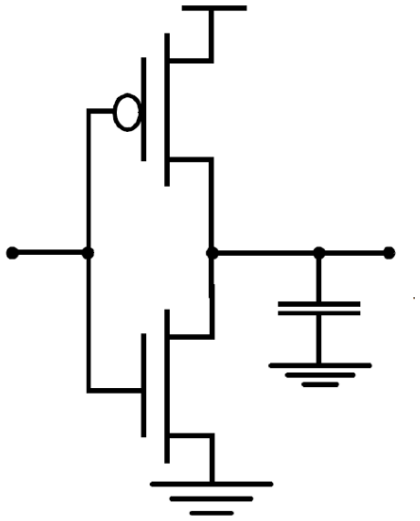
V_{out}: High-to-Low

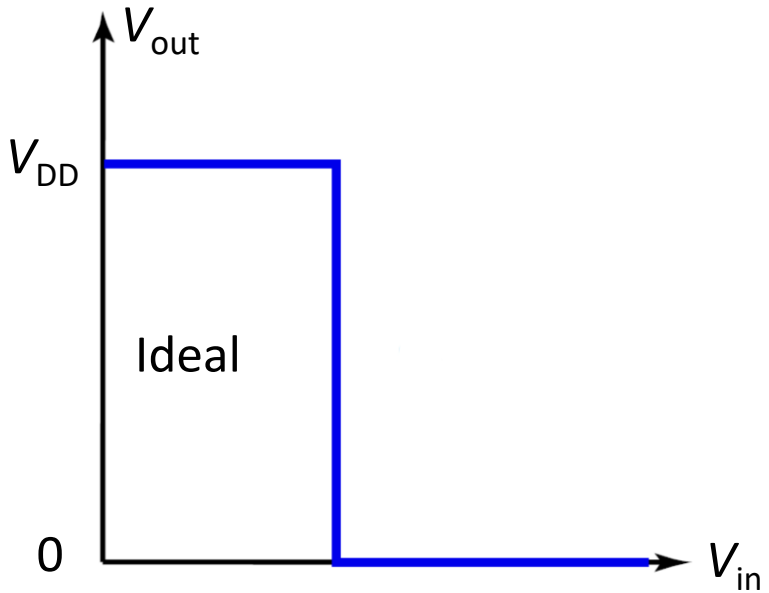


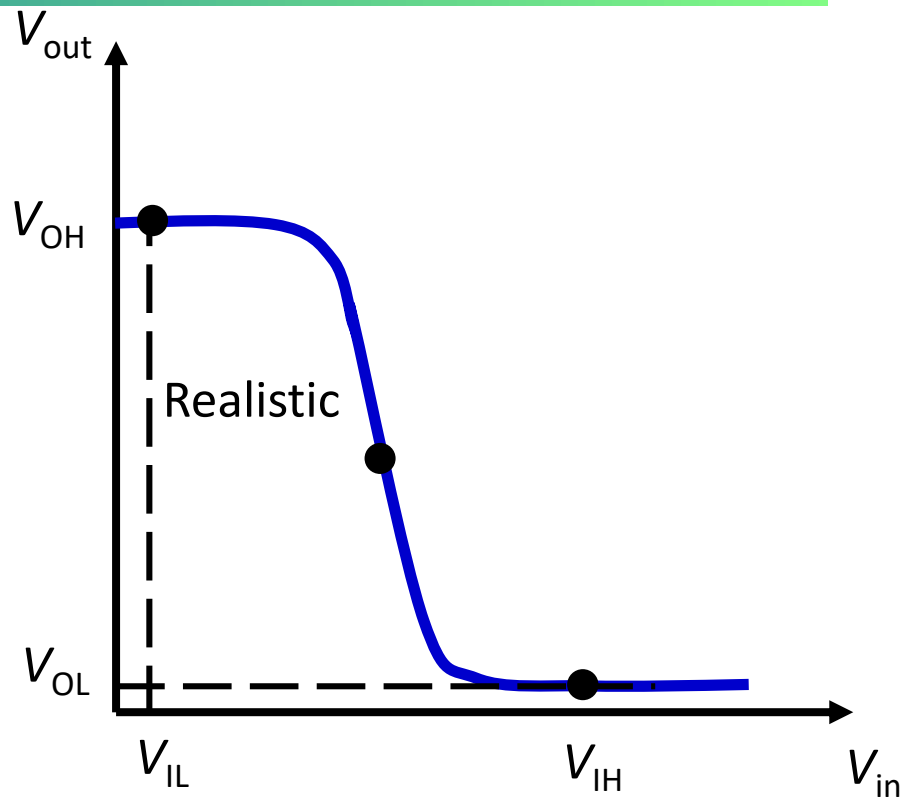
$V_{in} = 0$

V_{out}: Low-to-High

Inverter Voltage-Transfer Characteristic (VTC)







Recommand Reading

[1] Chapter 1, 4-11 of Semiconductor physics and devices basic principles, 4th, Neamen

[2] Introduction to quantum mechanics 2th, David J. Griffiths

[3] Solid State physics, Neil W. Ashcroft, N. David Mermin

[4] Introduction to Solid State Physics, Charles Kittel

[5] The Oxford Solid State Basics, Steven H. Simon

[6] Semiconductor physics and devices, Neamen

[7] 半导体物理学, 刘恩科

[8] Circuit analysis

[9] Digital Fundamentals, Thomas L Floyd

[10] Digital Integrated Circuits, A design Perspective, Rabaey

[11] Design of Analog CMOS Integrated Circuits, Behzad Razavi