ShanghaiTech University

EE 115B: Digital Circuits

Fall 2022

Lecture 15

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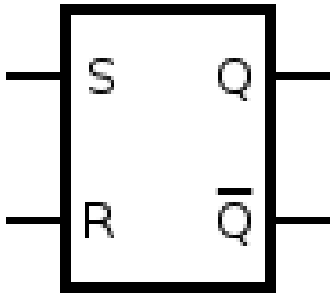
Basic SR latch

- Characteristic table (alternate)



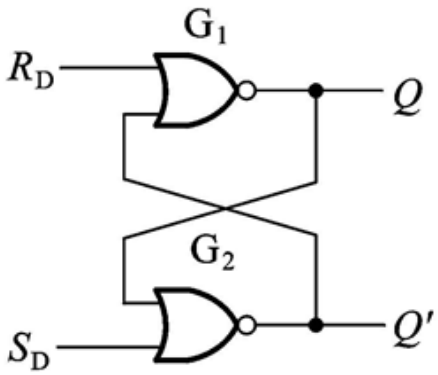
S	R	Q	$\overline{Q}$
0	0	**Latched**	
0	1	0	1
1	0	1	0
1	1	Metastable	

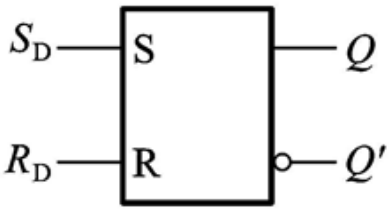
Source: https://en.wikibooks.org/wiki/Digital_Circuits/Latches

- S and R are active high signals.

Basic SR latch

- Characteristic table (alternate)



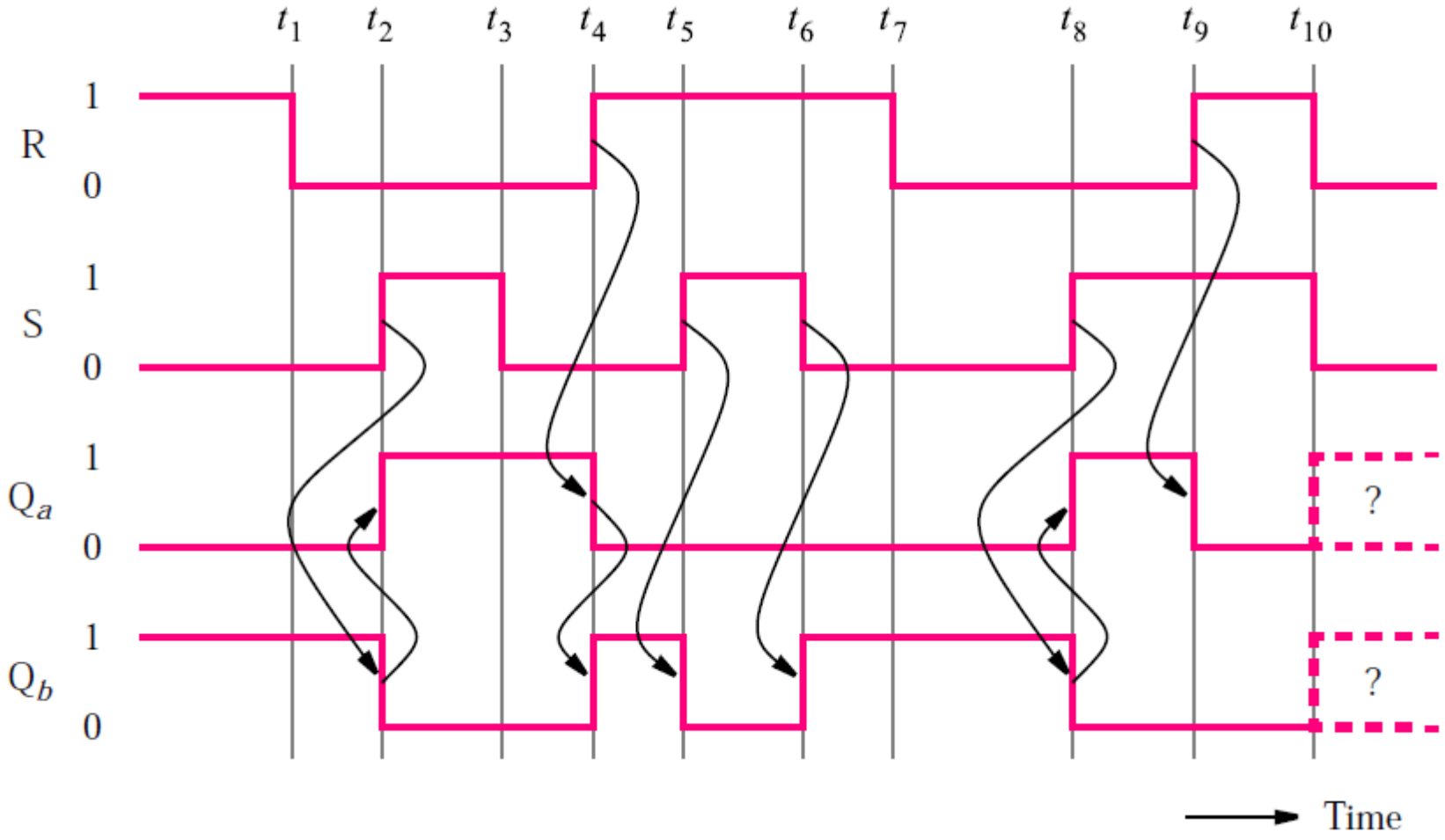


S_D	R_D	Q	Q^*
0	0	0	0
0	0	1	1
1	0	0	1
1	0	1	1
0	1	0	0
0	1	1	0
1	1	0	0①
1	1	1	0①

① S_D、R_D 的 1 状态同时消失后状态不定。

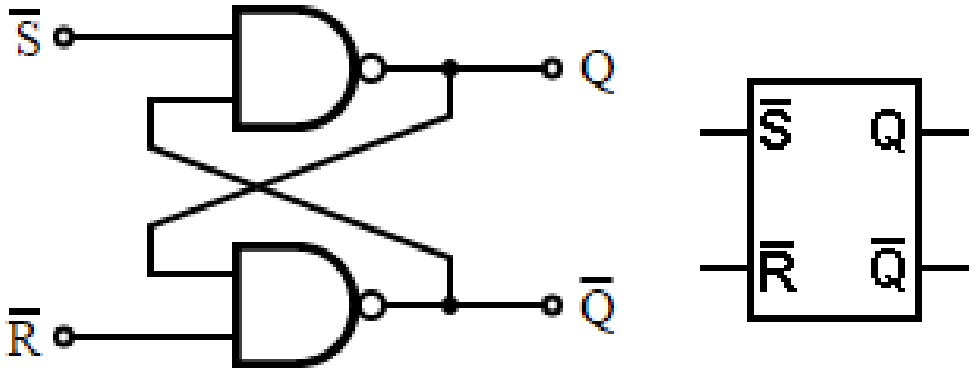
Basic SR latch

- Timing diagram (assume no propagation delay)



Alternate basic SR latch

- Implementation: NAND gates
- Set and reset are active low signals.
- Left to right: circuit, circuit symbol, and characteristic table



Source: https://en.wikipedia.org/wiki/Flip-flop_(electronics)

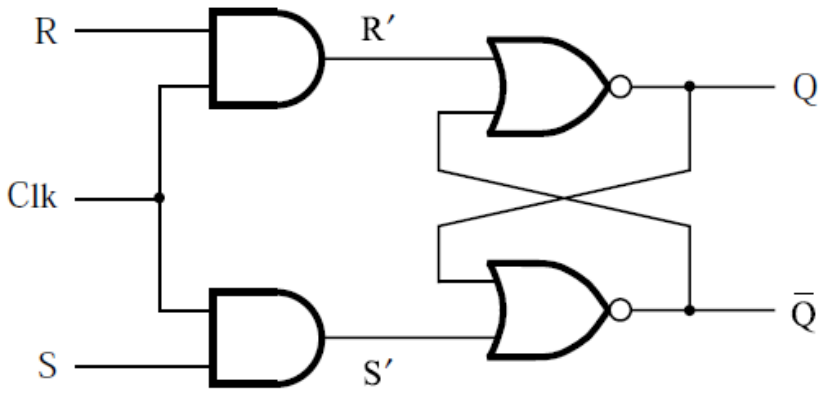
$\overline{SR}$ latch operation		
$\overline{S}$	$\overline{R}$	Action
0	0	Not allowed
0	1	Q = 1
1	0	Q = 0
1	1	No change

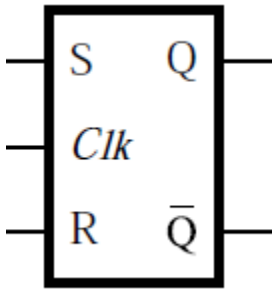
Gated SR latch

- Gated SR latch
  - Add a signal to control the time when the set and reset signals change values
- Two implementations
  - NOR gates
  - NAND gates

Gated SR latch with NOR gates

- Control signal: Clk
  - Clk=0, disabled: latched
  - Clk=1, enabled: basic SR latch
  - Left to right: circuit, circuit symbol, and characteristic table

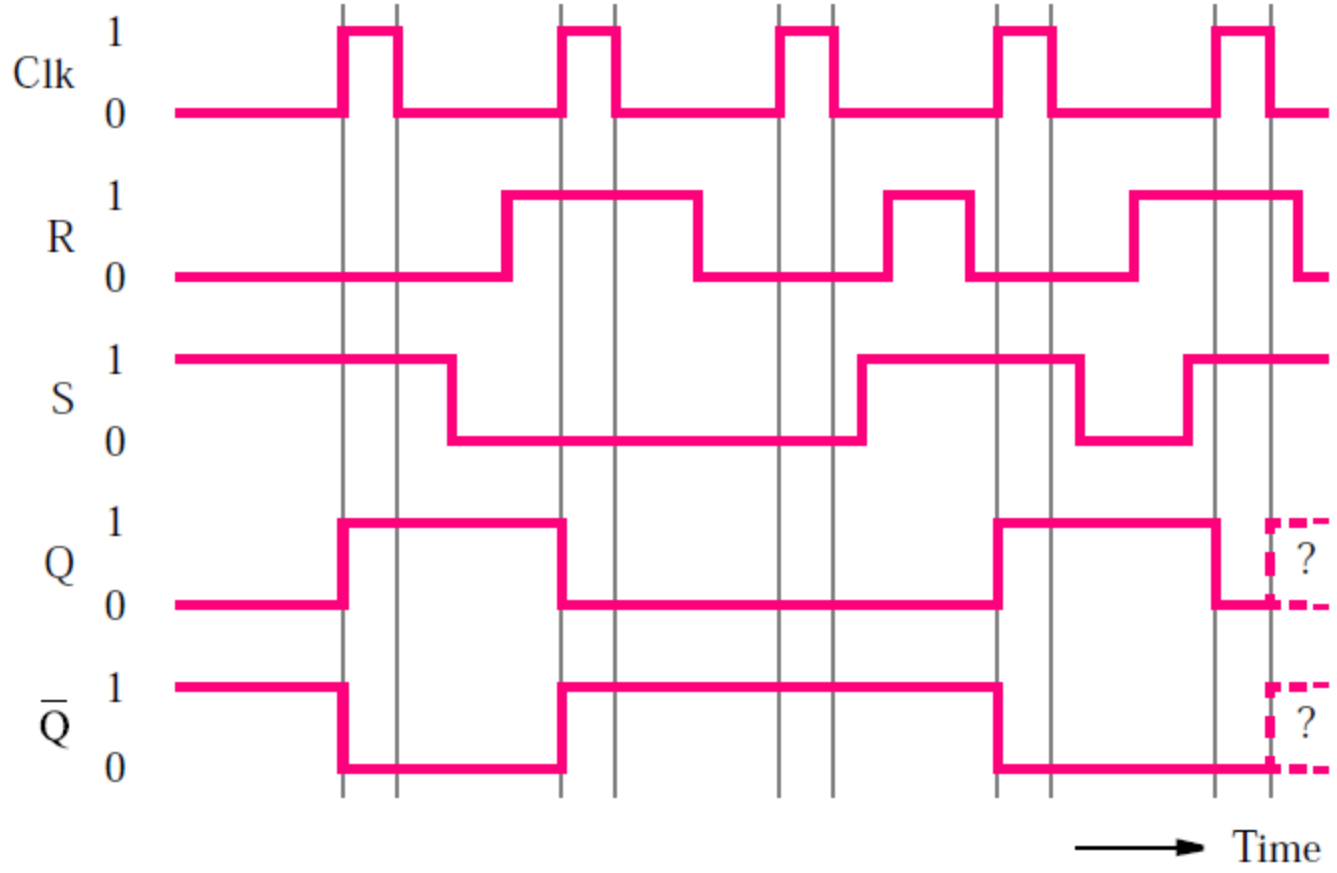




Clk	S	R	Q(*t* + 1)
0	x	x	Q(*t*) (no change)
1	0	0	Q(*t*) (no change)
1	0	1	0
1	1	0	1
1	1	1	x

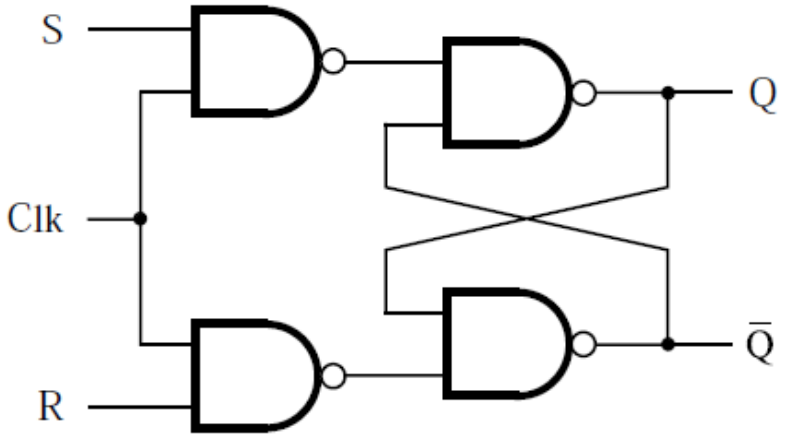
Gated SR latch with NOR gates

- Timing diagram



Gated SR latch with NAND gates

- Circuit



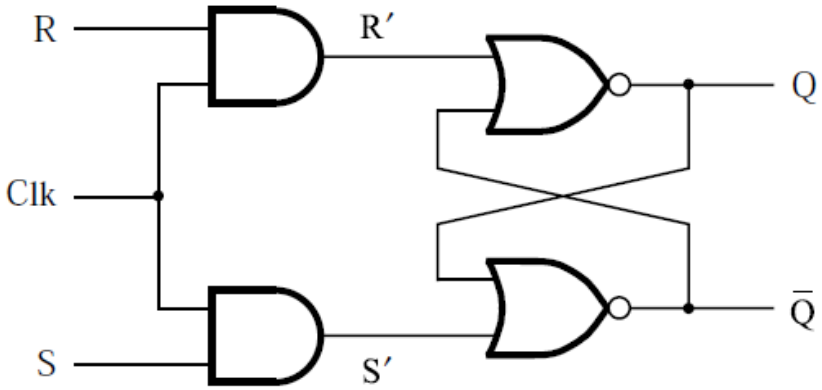
- Same circuit symbol and characteristic table

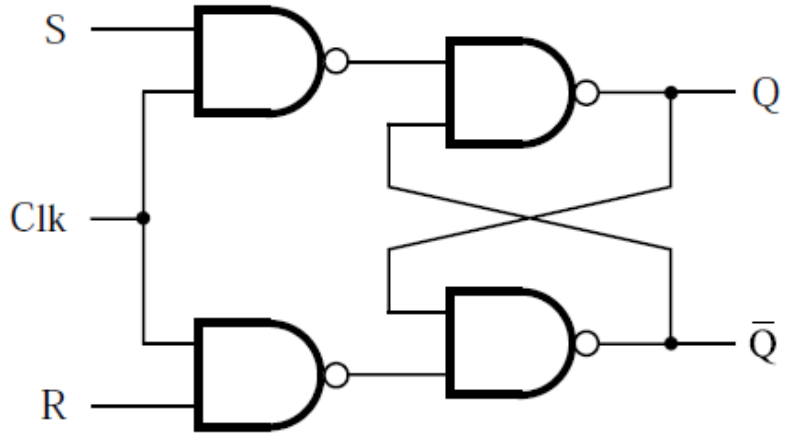
Clk	S	R	Q^+	Comments
0	×	×	Q	No change, typically stable states $Q = 0$, $\overline{Q} = 1$ or $Q = 1$, $\overline{Q} = 0$
1	0	0	Q	No change, typically stable states $Q = 0$, $\overline{Q} = 1$ or $Q = 1$, $\overline{Q} = 0$
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	×	Avoid this setting

Source: http://ecse.bd.psu.edu/cse271/memelem.pdf

Summary: gated SR latch

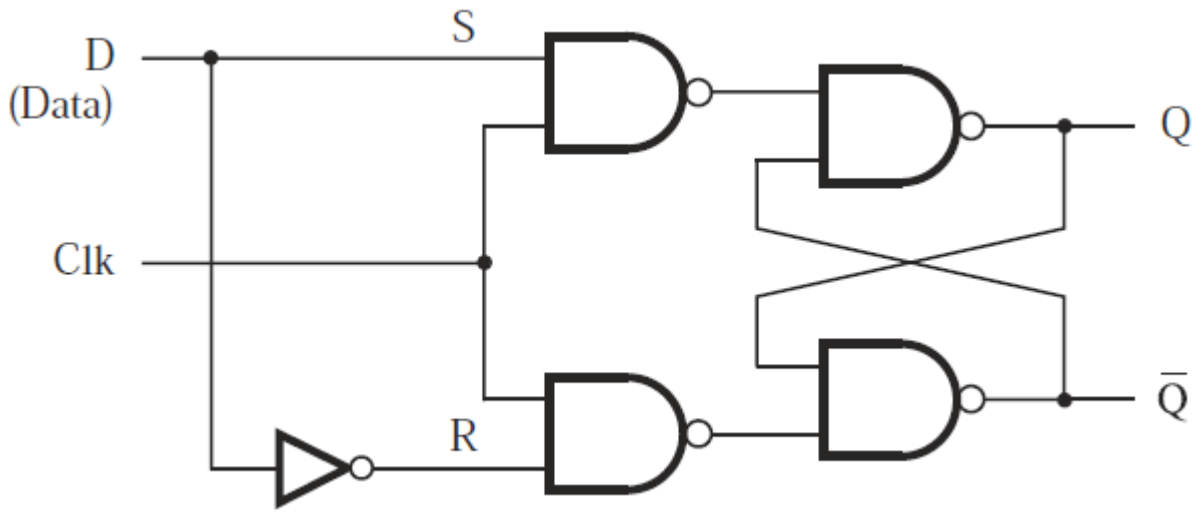
- Two implementations
  - NOR gates
  - NAND gates
    - Preferred (requires fewer transistors)





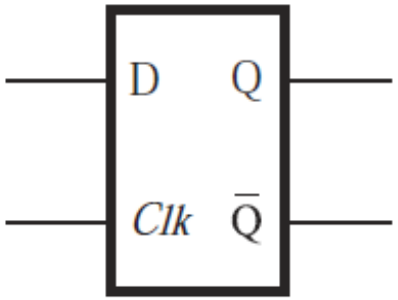
Gated D latch

- Only one input: D (data)
- Functionality
  - Clk=1: output (Q) follows input (D)
  - Clk=0: Q holds its previous value
- Circuit



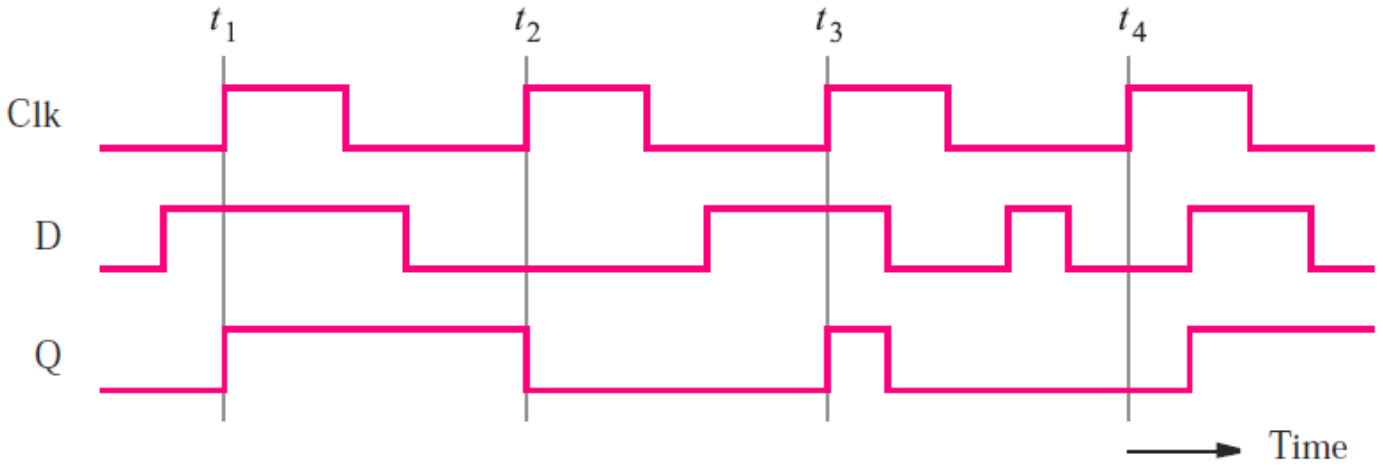
Gated D latch

- Circuit symbol and characteristic table



Clk	D	Q(t + 1)
0	x	Q(t)
1	0	0
1	1	1

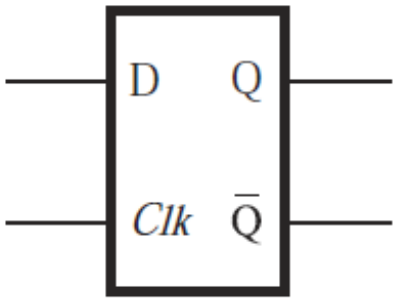
- Timing diagram



Level sensitive circuits

- Level sensitive circuits
  - Circuit output is controlled by clock level
  - Circuit output keeps changing according to inputs when clock is active
  - Circuit output value may change multiple times when clock is active
- Examples
  - Gated SR latch
  - Gated D latch
  - Clock is active high: Clk=1

VHDL code for gated D latch



Clk	D	Q(t + 1)
0	x	Q(t)
1	0	0
1	1	1

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY latch IS
    PORT ( D, Clk  : IN   STD_LOGIC ;
           Q       : OUT  STD_LOGIC) ;
END latch ;

ARCHITECTURE Behavior OF latch IS
BEGIN
    PROCESS ( D, Clk )
    BEGIN
        IF Clk = '1' THEN
            Q <= D ;
        END IF ;
    END PROCESS ;
END Behavior ;
```