ShanghaiTech University

EE 115B: Digital Circuits

Fall 2022

Final Exam, December 27, 2022

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Student ID: _____ Name in Chinese: _____

1. Short questions. (16 points. 2 points each.)
   (1) Convert $(25.625)_{10}$ to binary.
   (2) Convert $(45)_{16}$ to BCD.
   (3) Determine the odd parity bit for 10111010.
   (4) (True or False) The XNOR gate is also called the equivalence gate.
   (5) (True or False) For any combination of inputs, the sum of all minterms is 0.
   (6) What does "VHDL" stand for?
   (7) What does "FPGA" stand for?
   (8) (True or False) CASE statements can only appear in PROCESS blocks.
2. Develop the minimum SOP and POS expressions with the don't cares using Karnaugh map. (20 points. 10 points each.)
   $$\boldsymbol{Y(A,B,C,D) = \sum m(1,6,7,9,10) + D(2,3,11,13)}$$
3. (20 points.) Consider a circuit with three inputs and one output. The output is 1 if the number of the inputs taking the value of 1 is odd.
   (1) Define the logic variables and build the truth table (8 points).
   (2) Determine four equivalent expressions for the output: AND-OR, NAND, AND-OR-Invert (AOI), and NOR. (12 points. 3 points each.)
4. (15 points.) Consider the counter shown in Fig. 1. Note that the flip-flops are D flip-flops.

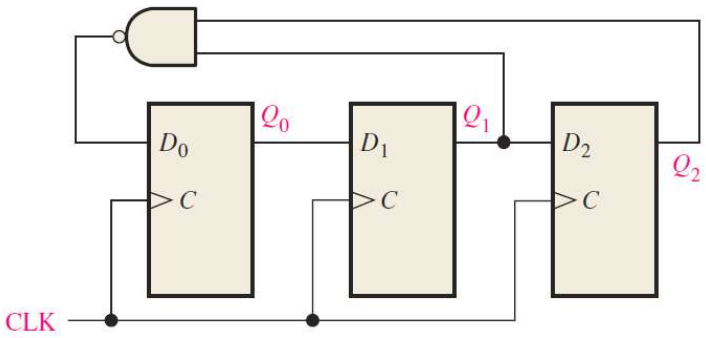

Fig. 1: A counter.

   (1) (True or False) This counter is asynchronous. **You need to justify your answer.** (3 points.)

(2) Sketch the timing diagram of Q_2, Q_1, and Q_0. Analyze the binary sequence of this counter. Assume that the initial states are $Q_0=Q_1=Q_2=0$. The count is represented by "$Q_2Q_1Q_0$" with Q_2 as the MSB and Q_0 as the LSB. (10 points.)
(3) Determine the modulus of this counter. (2 points.)

5. (29 points.) Consider the state diagram shown in Fig. 2. The input is "w" and the output is "z".

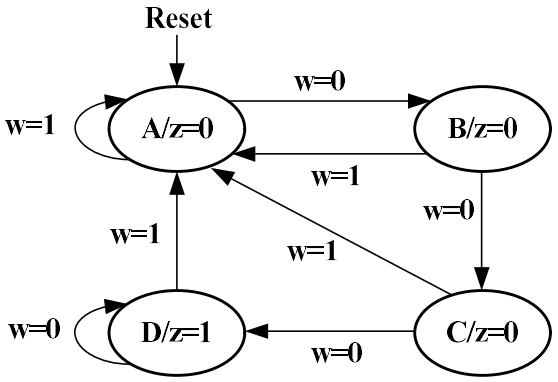

Fig. 2: A state diagram.

(1) (True or False) This is a Mealy-type finite state machine. **You need to justify your answer.** (3 points.)
(2) Convert the state diagram to a state table. (5 points.)
(3) Convert the state table developed in step (2) to a state-assigned table using the following configurations. The present state variables are "y_2y_1". The next state variables are "Y_2Y_1". The state assignment is "00" for A, "11" for B, "01" for C, and "10" for D. (5 points.)
(4) Based on the state-assigned table developed in step (3), determine the minimum SOP expressions for the output "z" and the next state variables "Y_1" and "Y_2". (12 points. 4 points each.)
(5) Design a state assignment using the one-hot encoding scheme. You only need to assign a code to each of the four states. (4 points.)

State	A	B	C	D
One-hot code				