ShanghaiTech University

EE 115B: Digital Circuits

Fall 2022

Lecture 9

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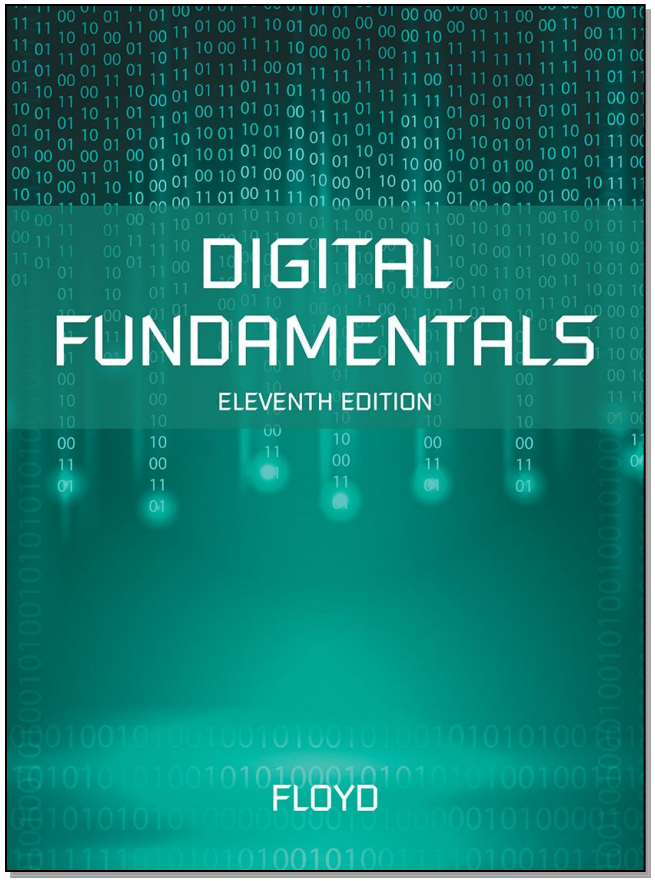
Digital Fundamentals

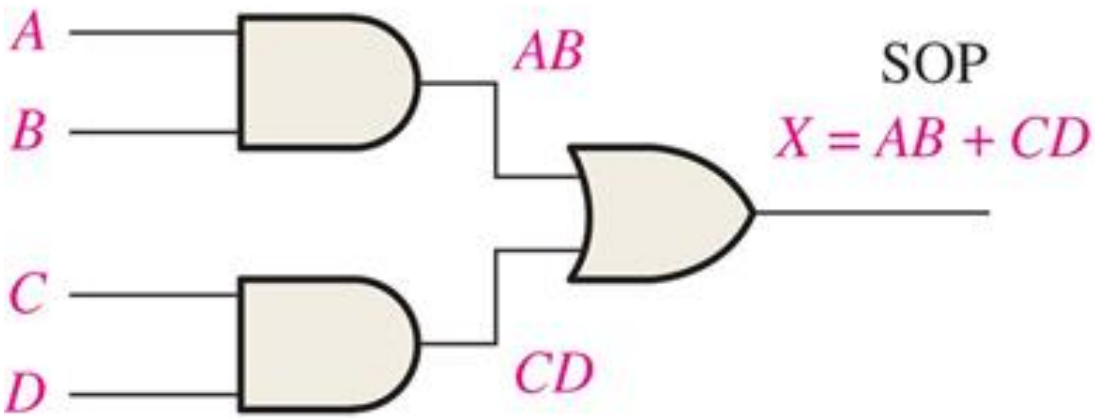
ELEVENTH EDITION



CHAPTER 5

Combinational Logic Analysis

AND-OR logic for SOP expressions



(a) Logic diagram (ANSI standard distinctive shape symbols)

FIGURE 5-1 An example of AND-OR logic.

AND-OR-Invert (AOI) logic for POS expressions

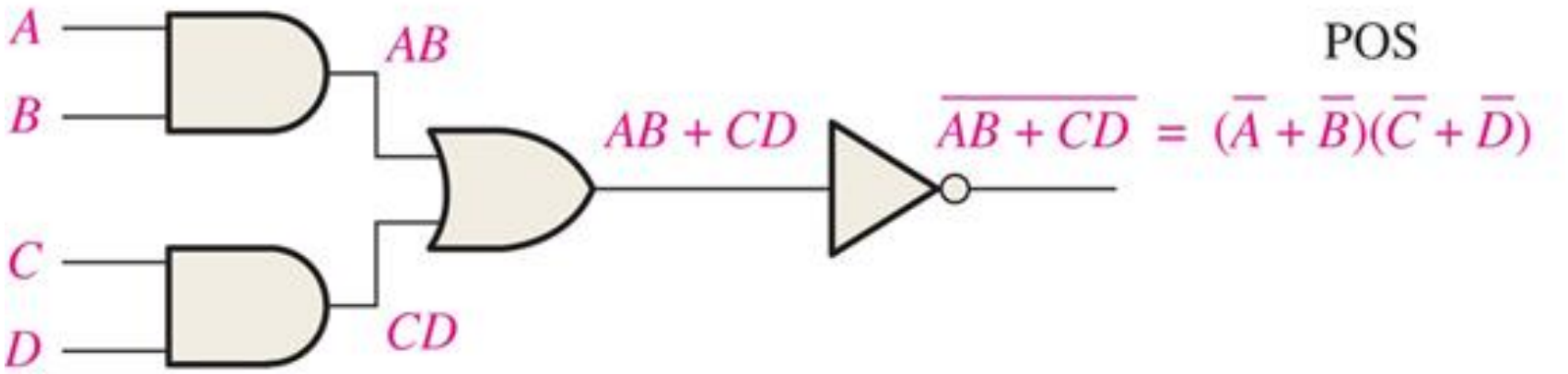


FIGURE 5-3 An AND-OR-Invert circuit produces a POS output.

$$X = (\overline{A} + \overline{B})(\overline{C} + \overline{D}) = (\overline{AB})(\overline{CD}) = \overline{\overline{(\overline{AB})(\overline{CD})}} = \overline{\overline{AB} + \overline{CD}} = \overline{AB + CD}$$

Implementing combinational logic: From a Boolean expression

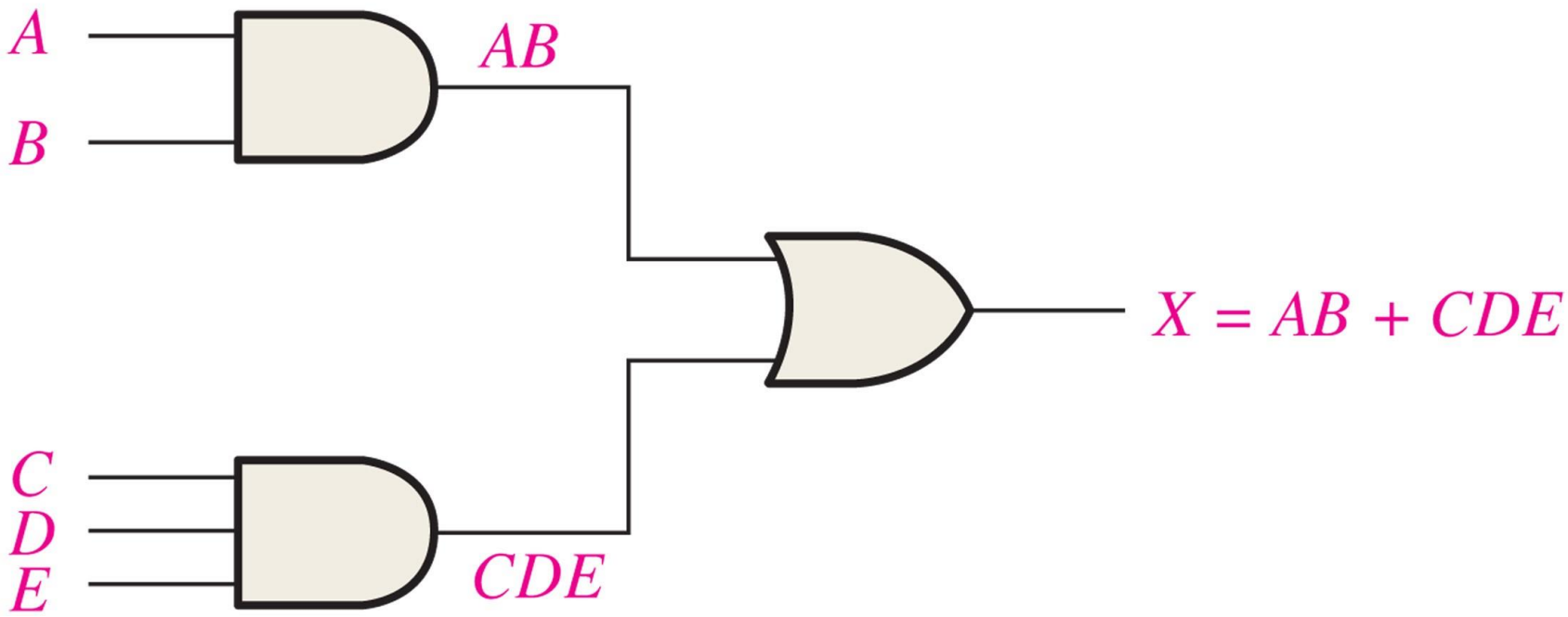


FIGURE 5-9 Logic circuit for $X = AB + CDE$.

Implementing combinational logic: From a truth table

TABLE 5–3

Inputs			Output	
A	B	C	X	Product Term
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\overline{A}BC$
1	0	0	1	$A\overline{B}\,\overline{C}$
1	0	1	0	
1	1	0	0	
1	1	1	0	

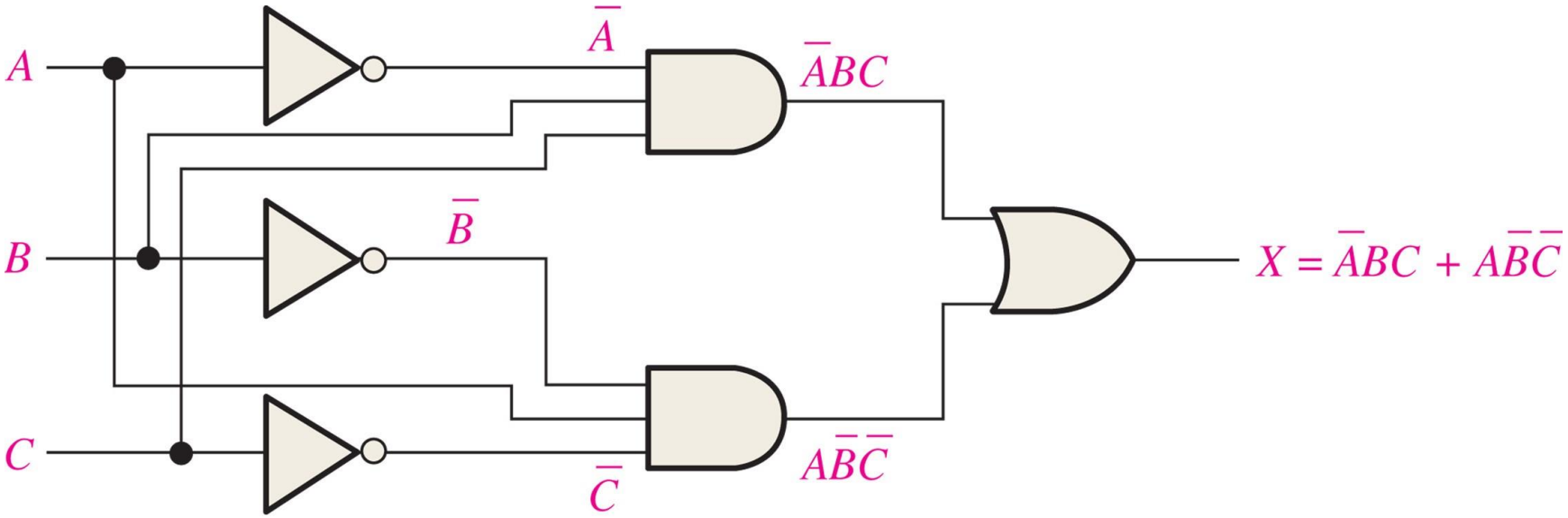
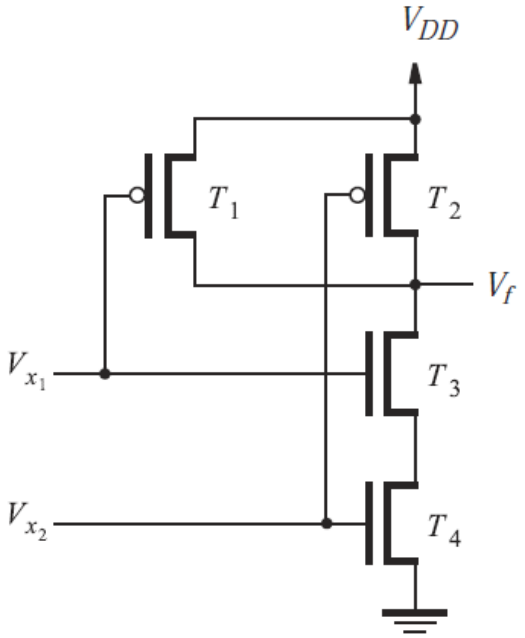


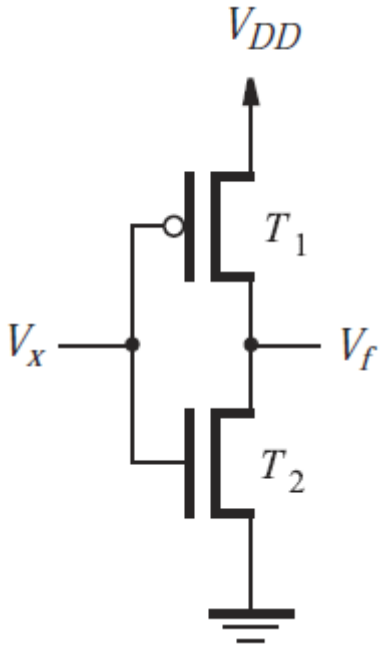
FIGURE 5-11 Logic circuit for $X = \bar{A}BC + ABC$.

NAND-only and NOR-only circuits

- CMOS implementations
  - 2-input AND/OR gate (6 transistors)
  - 2-input NAND/NOR gate (4 transistors)
  - NOT gate (2 transistors)



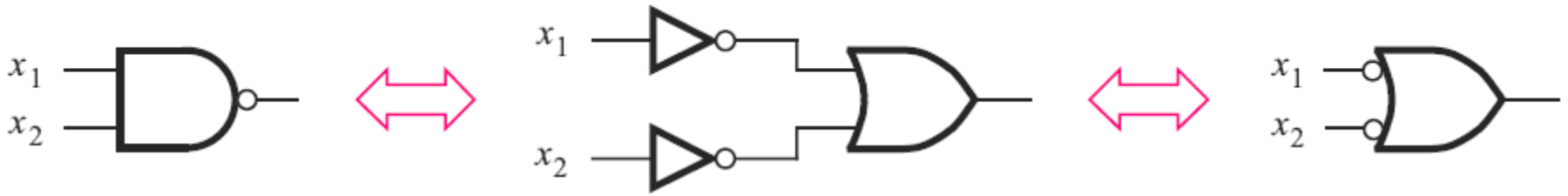
NAND



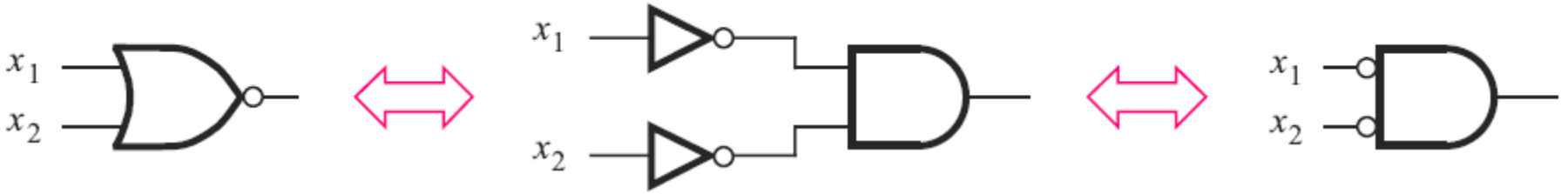
NOT

NAND-only and NOR-only circuits

- NAND and NOR gates (two symbols)



(a) $\overline{x_1 x_2} = \bar{x}_1 + \bar{x}_2$



(b) $\overline{x_1 + x_2} = \bar{x}_1 \bar{x}_2$

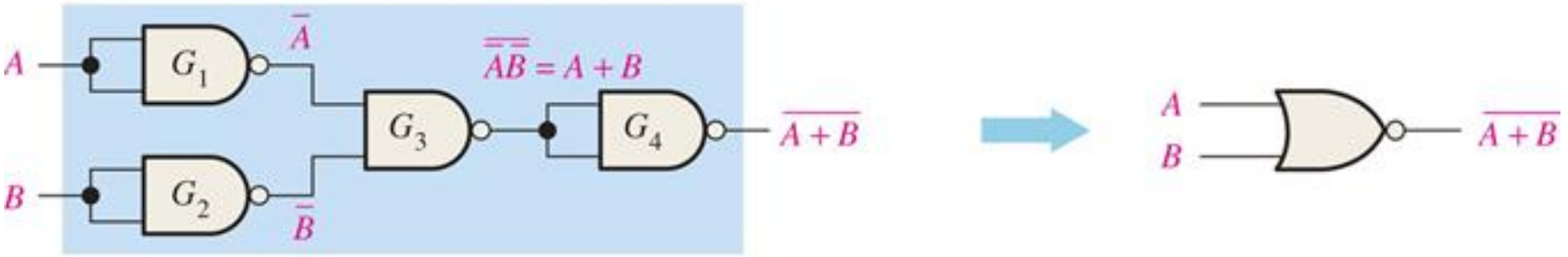
FIGURE 5-18 Universal application of NAND gates.

(a) One NAND gate used as an inverter

(b) Two NAND gates used as an AND gate

FIGURE 5-18 Universal application of NAND gates.

(c) Three NAND gates used as an OR gate



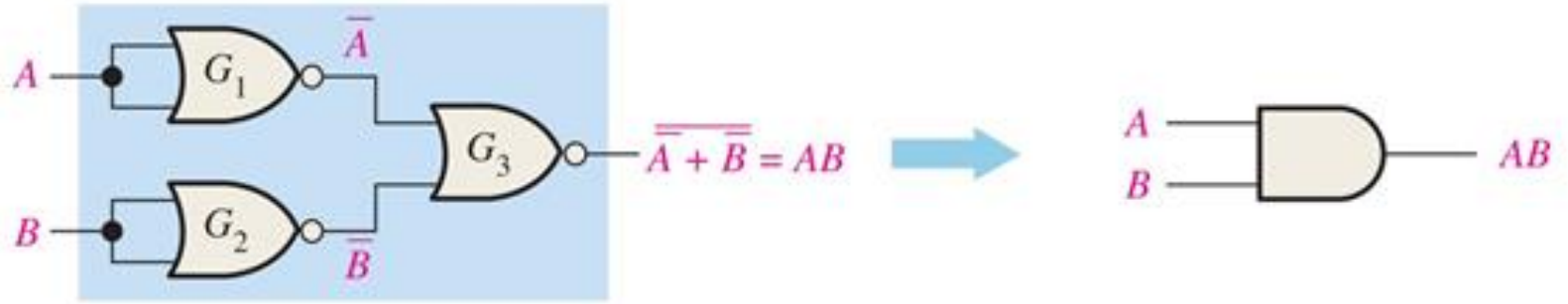
(d) Four NAND gates used as a NOR gate

FIGURE 5-19 Universal application of NOR gates.

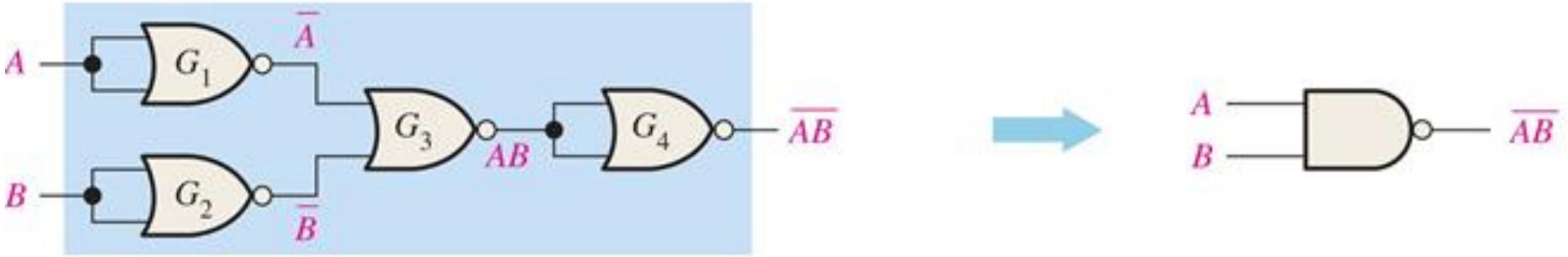
(a) One NOR gate used as an inverter

(b) Two NOR gates used as an OR gate

FIGURE 5-19 Universal application of NOR gates.



(c) Three NOR gates used as an AND gate



(d) Four NOR gates used as a NAND gate

NAND-only logic

【例 2.9.1】 试用 2 输入端与非门产生如下的逻辑函数

$$Y = AC + BC' \qquad (2.9.4)$$

解： 为了全部用 2 输入端与非门实现这个电路，就必须将式(2.9.4)变换成全部由两变量与非运算组成的形式。为此，利用摩根定理将式(2.9.4)变换为

$$\begin{aligned} Y &= AC + BC' \\ &= ((AC + BC')')' \\ &= ((AC)'(BC')')' \end{aligned}$$

根据上式就得到了图 2.9.4 的电路。 (2.9.5)

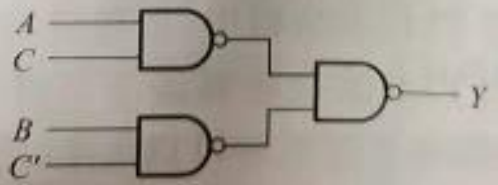


图 2.9.4 按照式(2.9.5)接成的逻辑电路

输入端C’应为：C级联NAND

NOR-only logic

【例 2.9.2】 试用 2 输入端或非门产生式(2.9.4)给出的逻辑函数。

解： 为了全部用 2 输入端或非门实现这个电路，则需要将式(2.9.4)变换成全部由两变量或非运算组成的形式。为此，用摩根定理将式(2.9.4)变换为

$$\begin{aligned} Y &= AC+BC' \\ &= ((AC)'(BC')')' \\ &= ((A'+C')(B'+C))' \\ &= (B'C'+A'C)' \\ &= ((B+C)'+(A+C')')' \end{aligned} \tag{2.9.6}$$

按照式(2.9.6)接成的逻辑电路如图 2.9.5 所示。

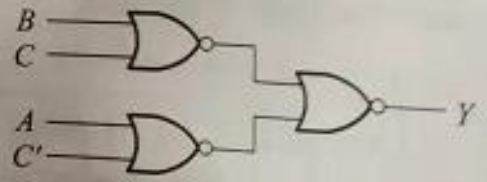
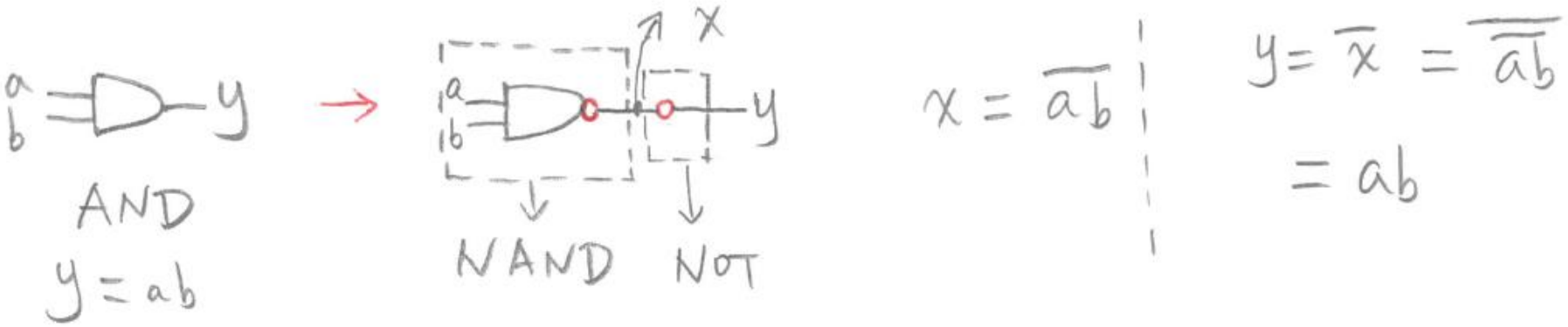


图 2.9.5 按照式(2.9.6)接成的逻辑电路

Boolean relationship for steps 3 and 4: AB+A'C+BC=AB+A'C

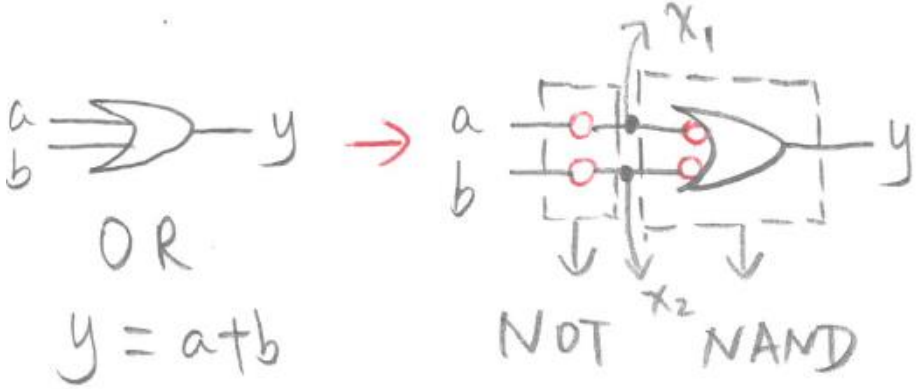
Convert AND to NAND

- General rules
  - Logic function (circuit functionality) should NOT be changed after conversions
  - A bubble means an inverter (NOT)
  - Add bubbles in pairs
- Convert AND to NAND



Convert OR/NOT to NAND

- Convert OR to NAND



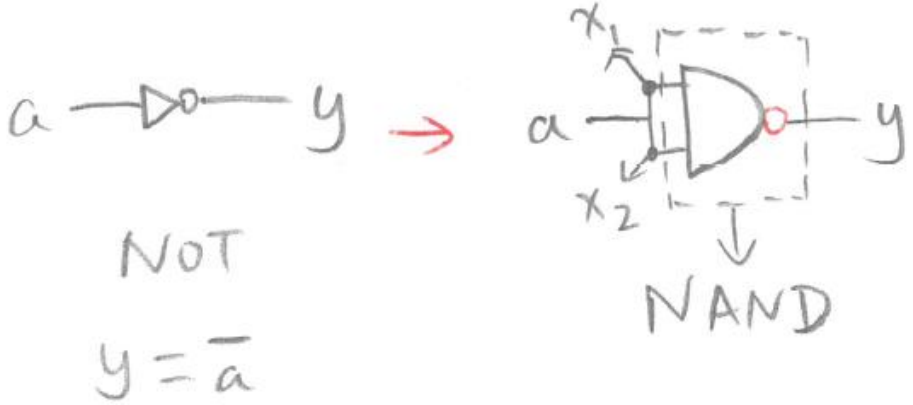
$x_1 = \bar{a}$

$x_2 = \bar{b}$

$y = \overline{x_1 x_2} = \overline{\bar{a}\,\bar{b}}$

$= a + b$

- Convert NOT to NAND



$x_1 = a$

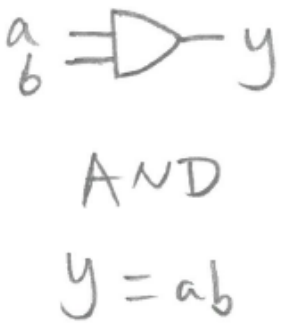
$x_2 = a$

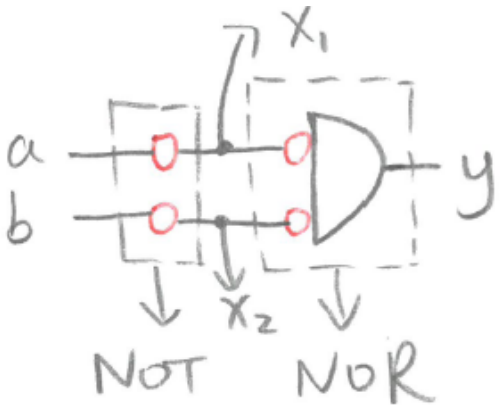
$y = \overline{x_1 x_2} = \overline{a\,a}$

$= \bar{a}$

Convert AND to NOR

- General rules
  - Logic function (circuit functionality) should NOT be changed after conversions
  - A bubble means an inverter (NOT)
  - Add bubbles in pairs
- Convert AND to NOR





$x_1 = \bar{a}$

$x_2 = \bar{b}$

$y = \overline{x_1 + x_2}$

$= \overline{\bar{a} + \bar{b}}$

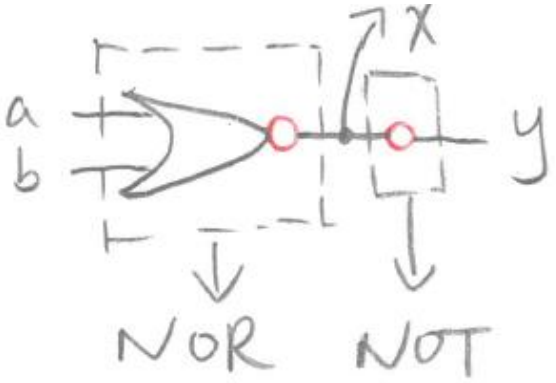
$= ab$

Convert OR/NOT to NOR

- Convert OR to NOR

OR

$y = a + b$



$x = \overline{a+b}$

$y = \bar{x}$

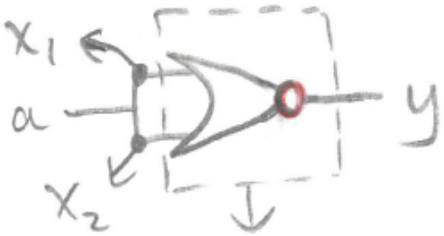
$= \overline{\overline{a+b}}$

$= a+b$

- Convert NOT to NOR

NOT

$y = \bar{a}$



NOR

$x_1 = a$

$x_2 = a$

$y = \overline{x_1 + x_2}$

$= \overline{a+a}$

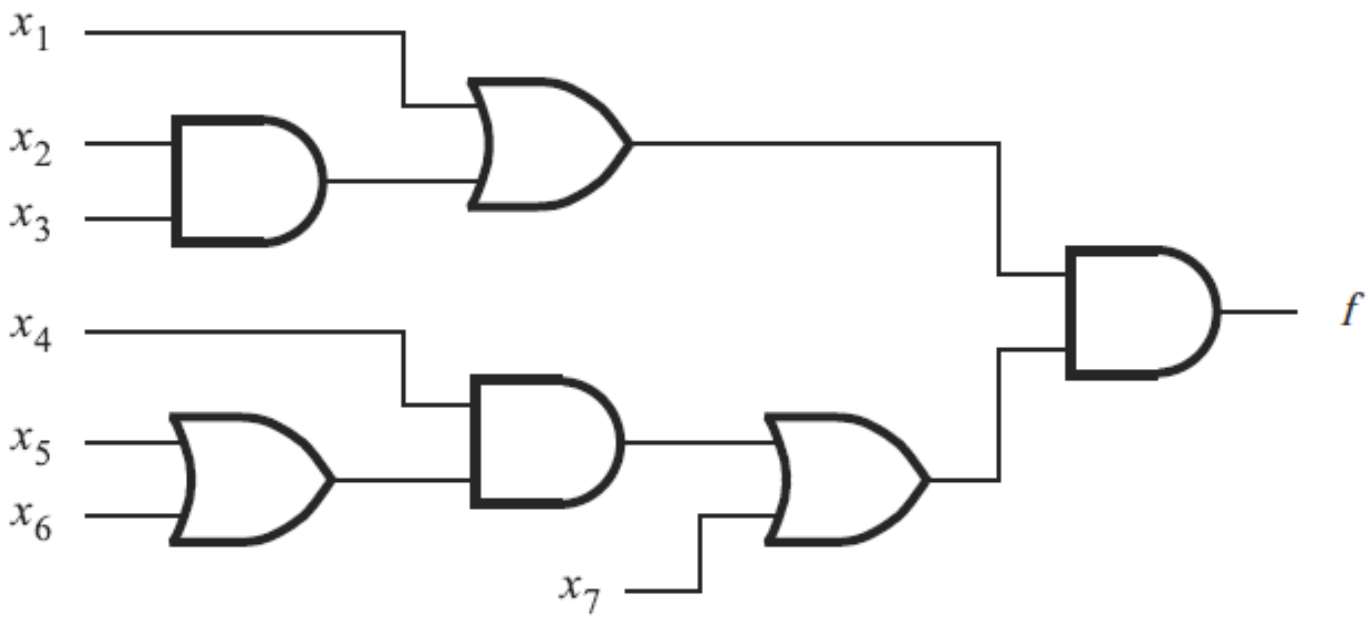
$= \bar{a}$

Convert circuits with AND/OR/NOT to NAND-only or NOR-only circuits

- Convert AND/OR to NAND (NOR if NOR-only) by adding bubbles
- If necessary, add bubbles to keep logic function unchanged
- Convert single bubbles to NAND/NOR

NAND-only

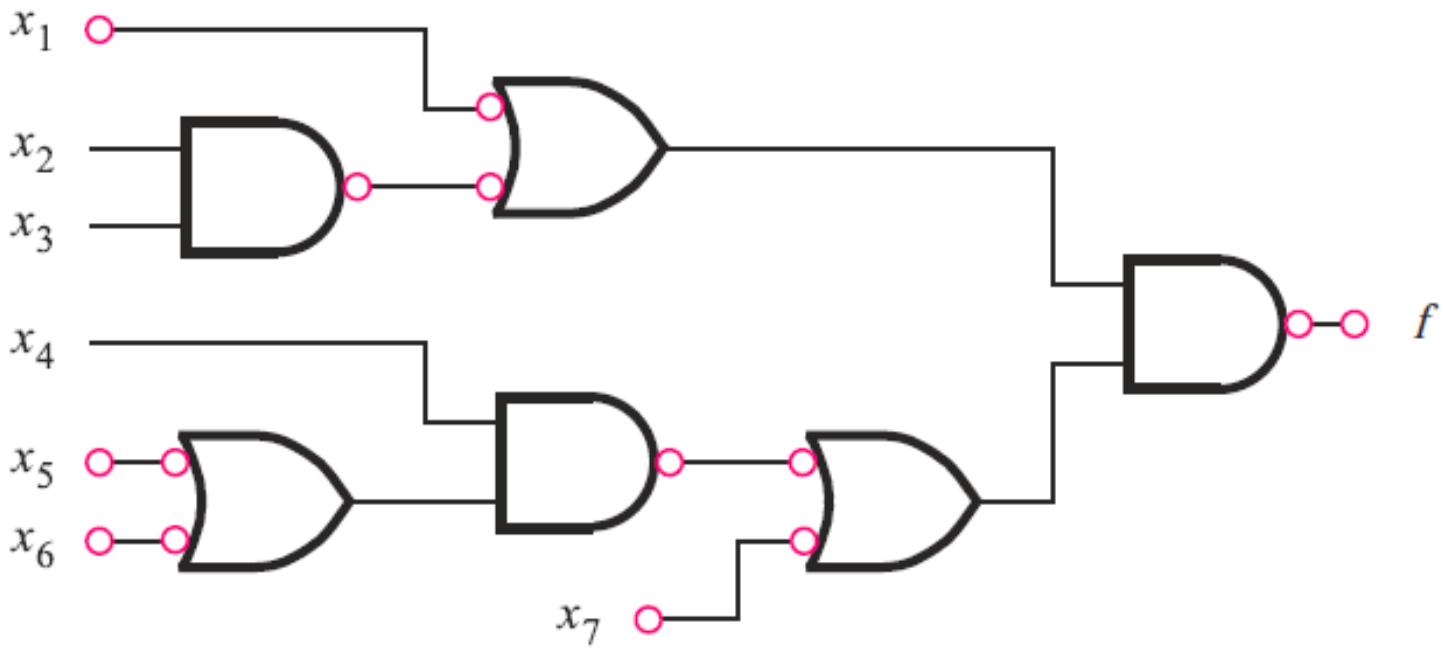
- Example



(a) Circuit with AND and OR gates

NAND-only

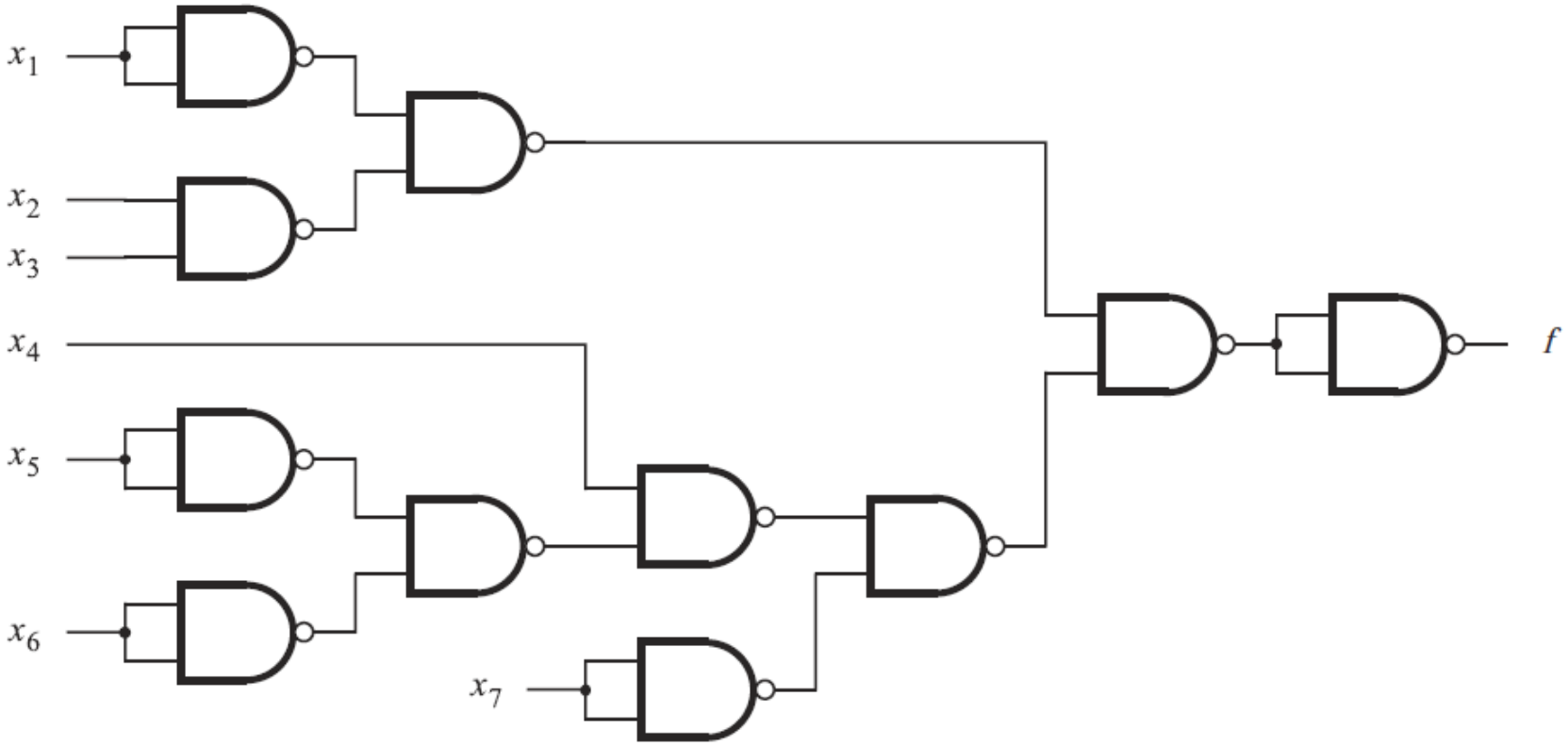
- Convert AND/OR to NAND, add bubbles



(b) Inversions needed to convert to NANDs

NAND-only

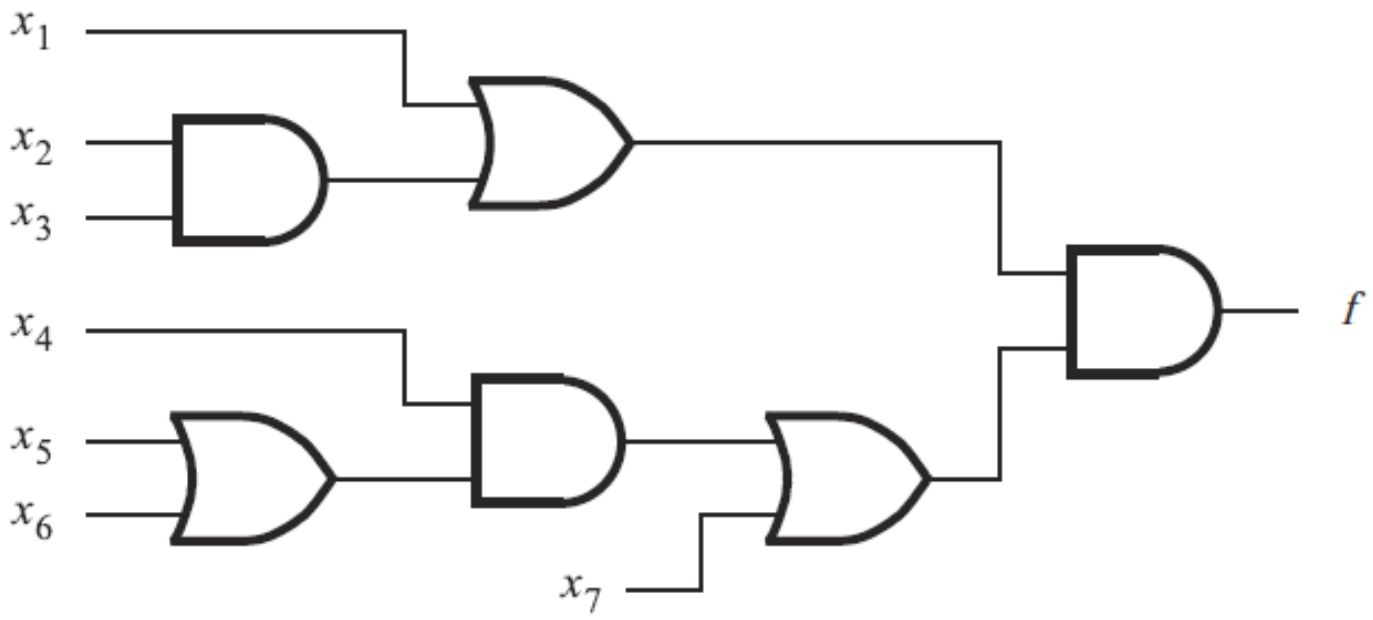
- Convert single bubbles to NAND



(c) NAND-gate circuit

NOR-only

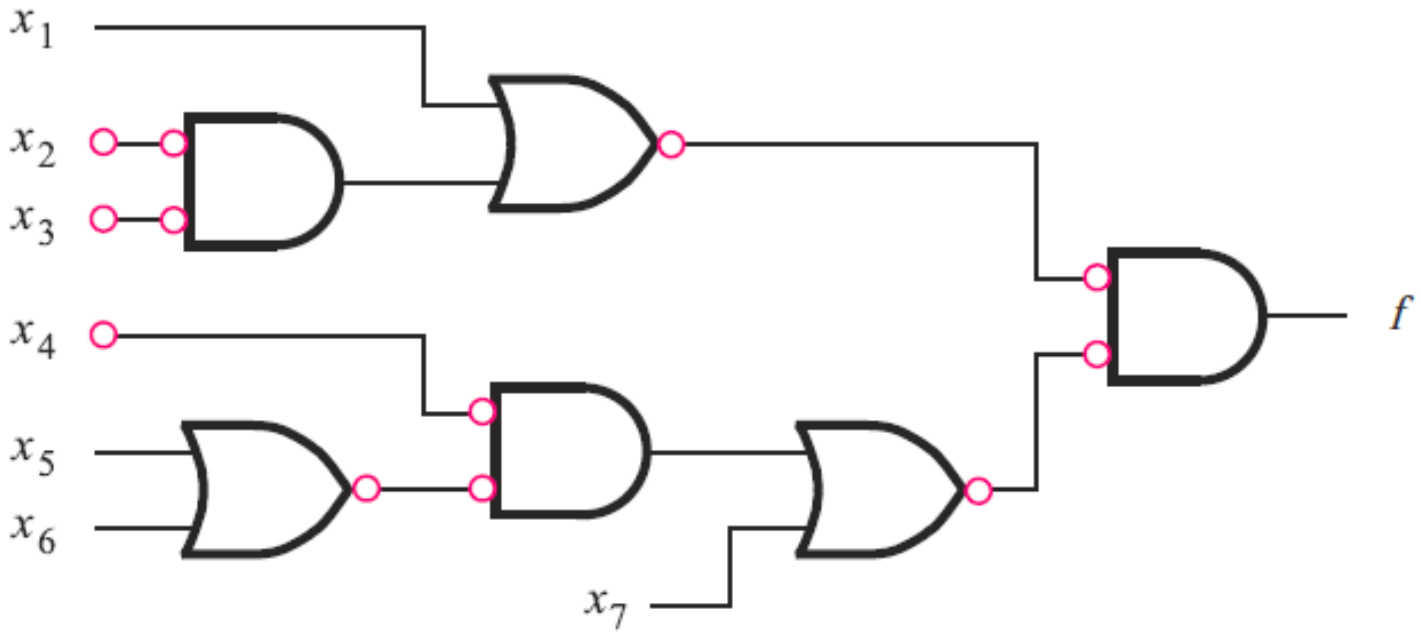
- Example



(a) Circuit with AND and OR gates

NOR-only

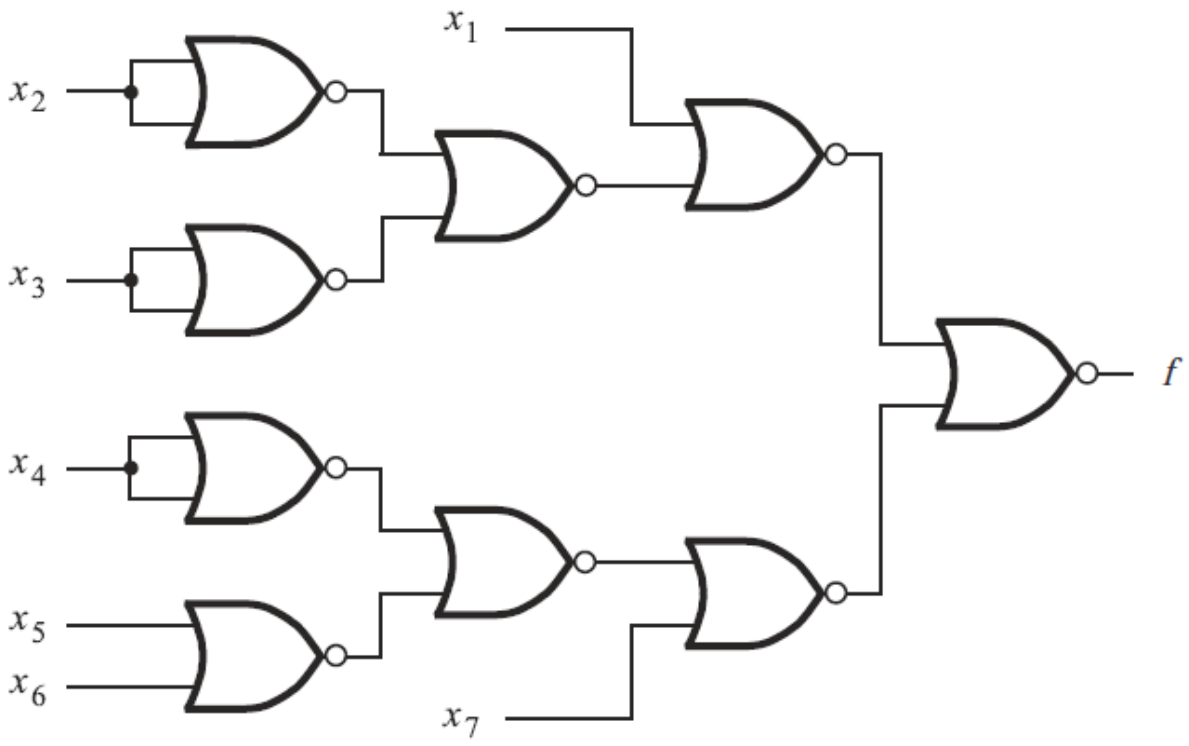
- Convert AND/OR to NOR, add bubbles



(a) Inversions needed to convert to NORs

NOR-only

- Convert single bubbles to NOR



(b) NOR-gate circuit