Student Name: _____
Student Number: _____
School: _____
Year of Entrance: _____

ShanghaiTech University Final Examination Cover Sheet

Academic Year : 2021 to 2022
Term: 2
Teaching School: School of Information Science and Technology
Instructor: zhuzhifeng,lijuan
Course Name: Digital Circuits
Course Number: EE115B.01

Exam Instructions for Students:

1. All examination rules must be strictly observed during the entire exam, and any form of cheating is prohibited.

2. Other than allowable materials, students taking closed-book tests must place their books, notes, tablets and any other electronic devices in places designated by the examiners.

3.Students taking open-book tests may use allowable materials authorized by the examiners. They must complete the exam independently without discussion with each other or exchange of materials.

For Marker's Use:

Section	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Total
Marks																	
Recheck																	

Marker's Signature: **Reviewer's Signature:**
Date: **Date:**

1. Perform the following calculations (4 points, 2 points each)

a) The number in 2's complement form is 11111011111, write down its decimal value.

b) Expand the 2's complement 1111001 to 10 bits.

2. Proof the following two statements are equivalent (5 points)

a) The 2's complement is obtained by adding 1 to the 1's complement.

b) To go from the 2's complement form back to true binary, take the 1's complement of the 2's complement number and add 1 to the least significant bit.

3. Draw the circuit diagram (using MOSFET) of the 3-input AND gate. (3 points)

4. Which of the following statements are correct? (3 points)
(a) N-type semiconductor has excessive electrons
(b) N-type semiconductor has excessive holes
(c) A donor atom moves E_F higher
(d) A donor atom moves E_F lower

5. Proof AB+A'C+BCD=AB+A'C. Karnaugh map and truth table are not allowed. (5 points)

6. Draw the circuit of the logic expression A'BC+AB'C+ABC', using only two input AND and NAND gates. (5 points)

7. For the traffic light example discussed in the lecture note 7-Combinational Logic Analysis-publish.pdf, define light on is 0 and light off is 1. For the normal state, define the output as 1. For the problematic state, define the output as 0. Redesign the circuit using only NAND gate. (6 points)

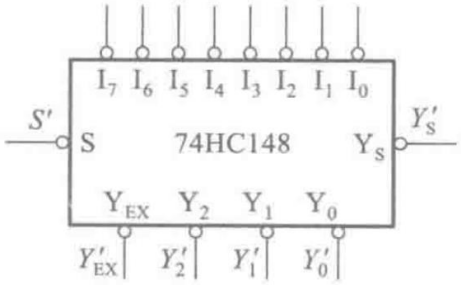
a) Write down the truth table (2 points)
b) Write down the Boolean expression (2 points)
c) Design the circuit using only NAND gates. (2 points)

8. Design the full adder by circling 0 in the Karnaugh map (6 points)

a) Write down the truth table (2 points)
b) Draw the Karnaugh map and simplify the expression (2 points)
c) Draw the circuit (2 points)

9. The truth table and functionality table of the priority encoder 74HC148 are shown below. Use two 74HC148 to construct a 16-4 encoder. Define the inputs as I_{15}' to I_0', the outputs as Z_3' to Z_0', i.e., active LOW. (7 points)

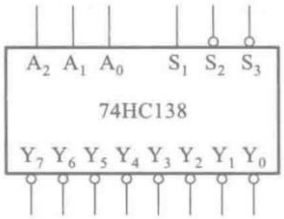
输入									输出				
S'	I'_0	I'_1	I'_2	I'_3	I'_4	I'_5	I'_6	I'_7	Y'_2	Y'_1	Y'_0	Y'_S	Y'_{EX}
1	×	×	×	×	×	×	×	×	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1
0	×	×	×	×	×	×	×	0	0	0	0	1	0
0	×	×	×	×	×	×	0	1	0	0	1	1	0
0	×	×	×	×	×	0	1	1	0	1	0	1	0
0	×	×	×	×	0	1	1	1	0	1	1	1	0
0	×	×	×	0	1	1	1	1	1	0	0	1	0
0	×	×	0	1	1	1	1	1	1	0	1	1	0
0	×	0	1	1	1	1	1	1	1	1	0	1	0
0	0	1	1	1	1	1	1	1	1	1	1	1	0



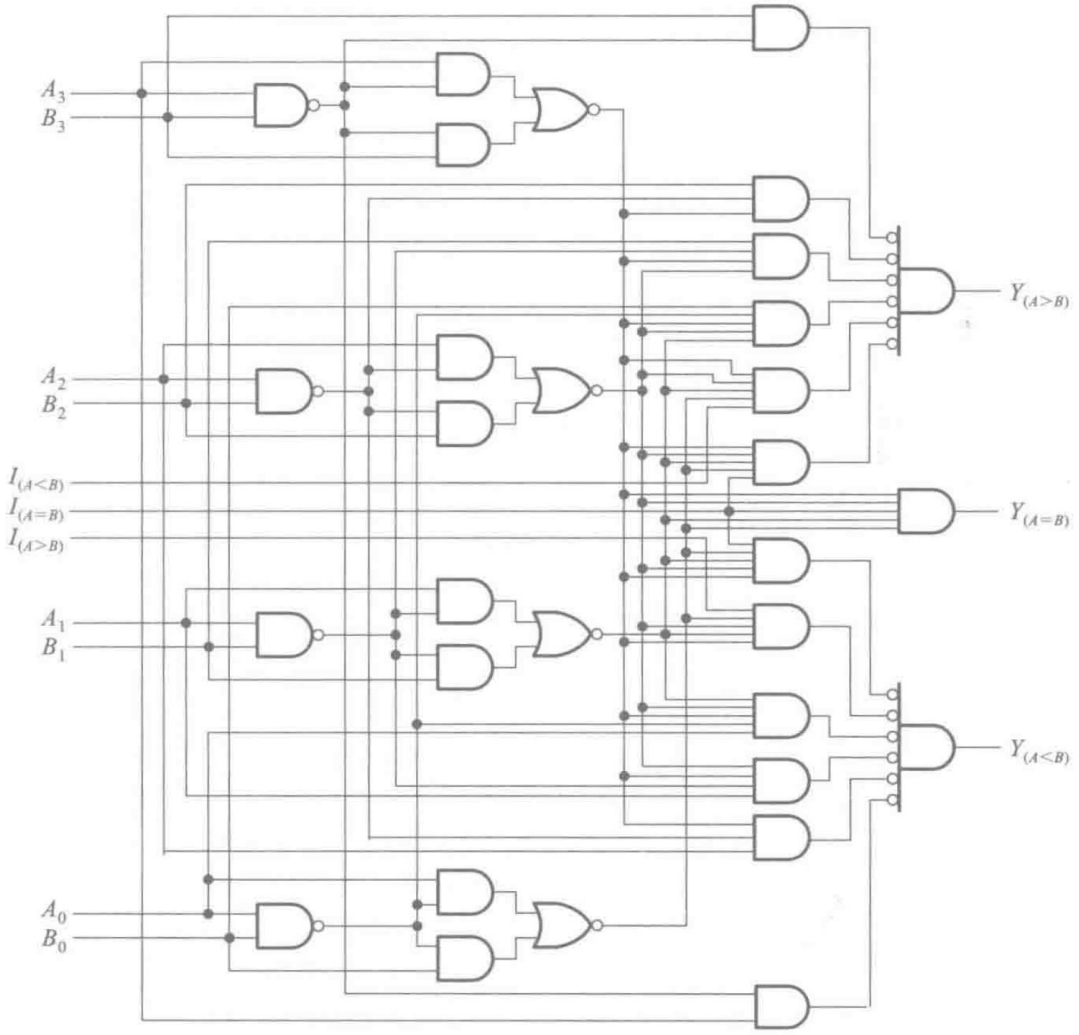
Y'_S	Y'_{EX}	状态
1	1	不工作
0	1	工作，但无输入
1	0	工作，且有输入
0	0	不可能出现

10. The truth table and chip diagram of the decoder 74HC138 are shown below. Use two 74HC138 to construct a 4-16 decoder. Define the inputs as A_3 to A_0, the outputs as Y_{15}' to Y_0'(7 points)

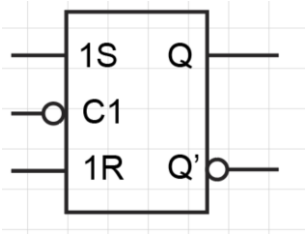
输入					输出							
S_1	$S_2'+S_3'$	A_2	A_1	A_0	Y_0'	Y_1'	Y_2'	Y_3'	Y_4'	Y_5'	Y_6'	Y_7'
0	×	×	×	×	1	1	1	1	1	1	1	1
×	1	×	×	×	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1	1	1
1	0	1	0	0	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	0



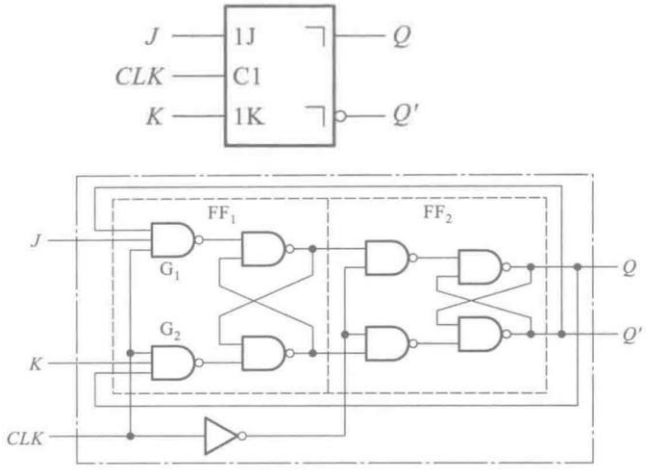
11. For the 4 bit comparator shown below, write down the expression of Y(A>B), Y(A=B) and Y(A<B). (7 points)

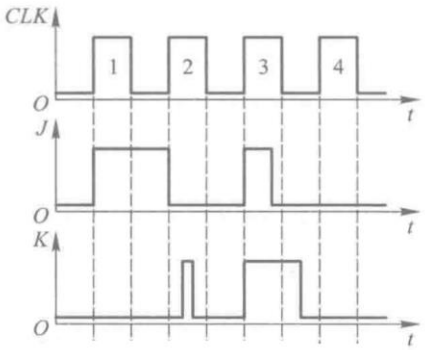


12. Draw the circuit implementation of the following SR latch using logic gates (not MOSFET). (7 points)



13. For the JK FF shown below, plot the wave diagram of *Q* and *Q*'. Assume the initial Q and the output of the master stage are 0. (7 points)



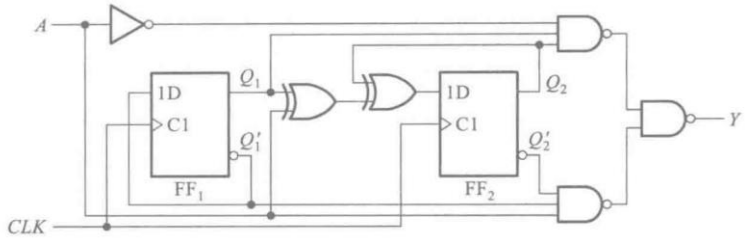


14. For the circuit shown below (12 points, 4 points each)

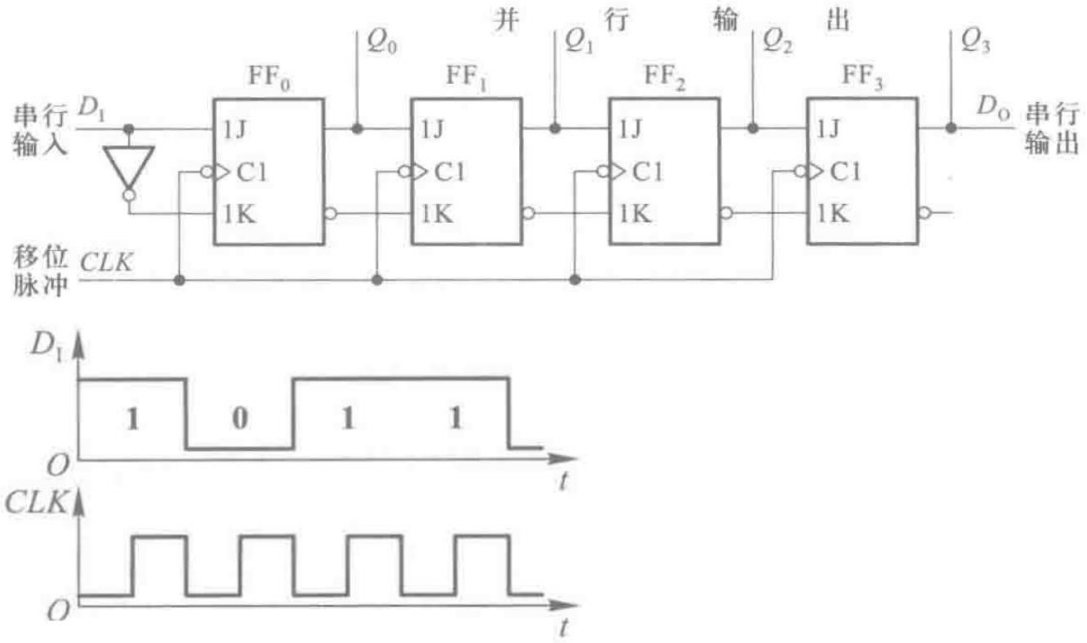
a) Write down the 驱动方程、状态方程、输出方程

b) Plot the truth table

c) Plot the state diagram (状态转换图)



15. Plot the wave diagram of Q3, Q2, Q1, Q0. Assume the initial state is 0000. (7 points)

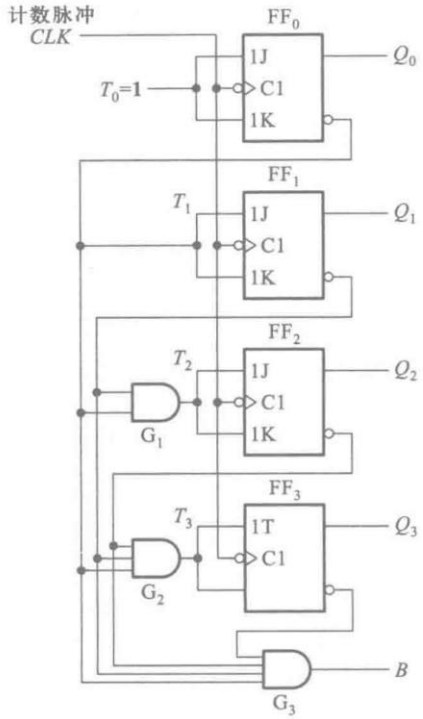


16. For the circuit shown below (9 points, 3 points each)

a) Write down the 驱动方程、状态方程、输出方程.

b) Plot the truth table.

c) Does the state change at rising edge or falling edge of CLK?



Ref. 1
Truth table of D and T FF

D	Q	Q^*
0	0	0
0	1	0
1	0	1
1	1	1

T	Q	Q^*
0	0	0
0	1	1
1	0	1
1	1	0