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Location: SIST,1D-106

Time: Tuesday 8:15-9:55 (Single Week) & Friday 8:15-9:55 (Weekly)

学年学期: 2021-2022学年2学期 切换学期

节次/周次	星期一	星期二	星期三	星期四	星期五
第一节 8:15 - 9:00		数字电路(EE115B.01)			数字电路(EE115B.01)
第二节 9:10 - 9:55		(单1-15,信息学院1D-106)			(1-15,信息学院1D-106)
第三节 10:15 - 11:00					
第四节 11:10 - 11:55					

Teachers

- Course Instructor: Zhifeng Zhu(祝智峰)

Office: SIST, 3-334

Email: zhuzhf@shanghaitech.edu.cn

Tel&Wechat: 15221986634

Office Hour: Friday 10 am to 12 pm (via email appointment)

Homepage: https://sist.shanghaitech.edu.cn/2020/0707/c7499a53852/page.htm

- Experiment Course Instructor: Juan Li (李娟)

Office: SIST, 1B-204

Email: lijuan1@shanghaitech.edu.cn

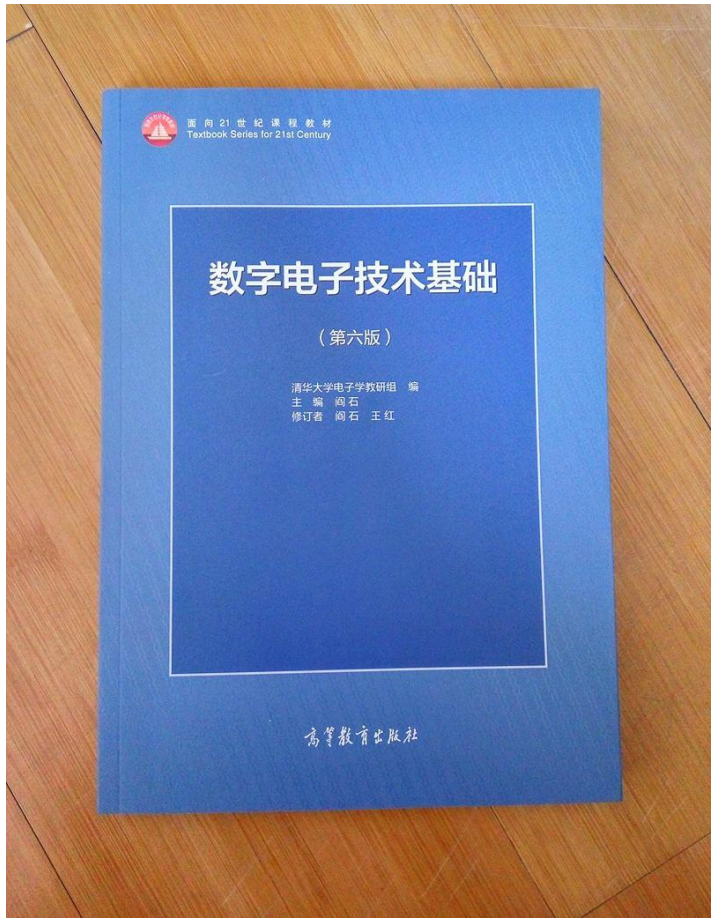
Tel: 20685262

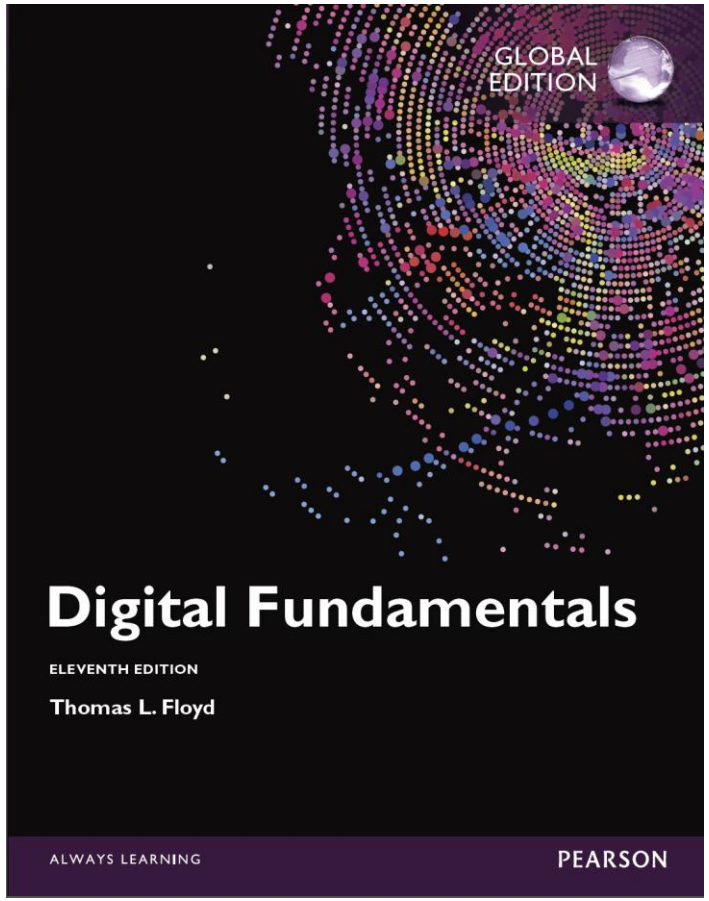
- Teaching Assistant

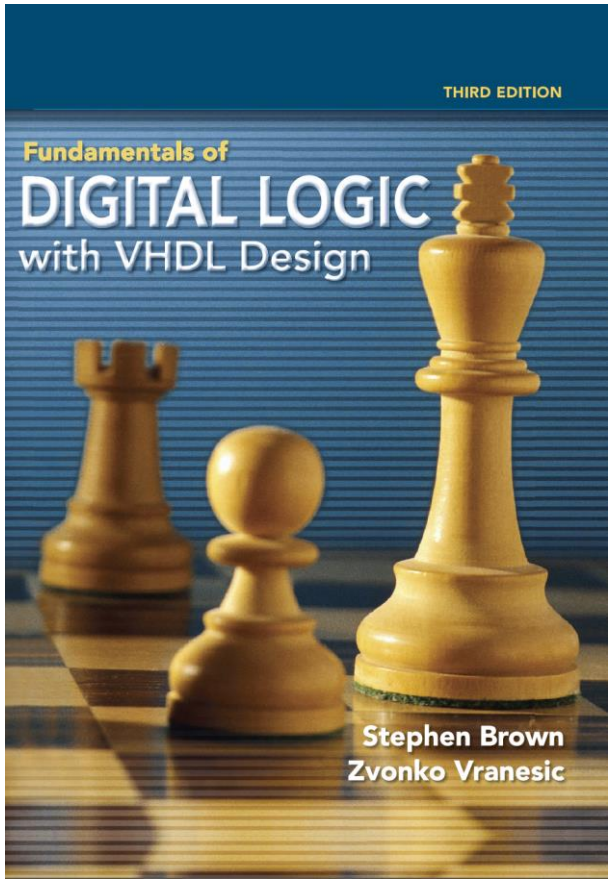
Yue Xin(辛玥): xinyue@shanghaitech.edu.cn

Zhengde Xu(徐正德): xuzhd@shanghaitech.edu.cn

Books


面向21世纪课程教材
Textbook Series for 21st Century
数字电子技术基础
（第六版）
清华大学电子学教研组 编
主 编 阎石
修订者 阎石 王红
高等教育出版社


GLOBAL EDITION
Digital Fundamentals
ELEVENTH EDITION
Thomas L. Floyd
ALWAYS LEARNING
PEARSON


THIRD EDITION
Fundamentals of
DIGITAL LOGIC
with VHDL Design
Stephen Brown
Zvonko Vranesic

Resources

BB system

- Publish all lecture materials
- Submit homeworks

Wechat group

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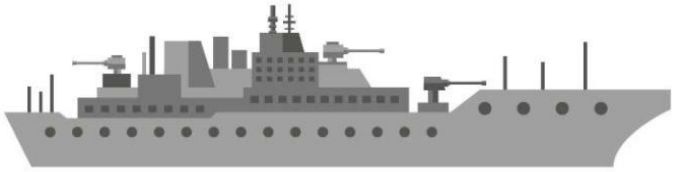
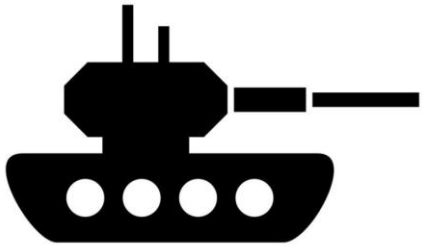
Electronics

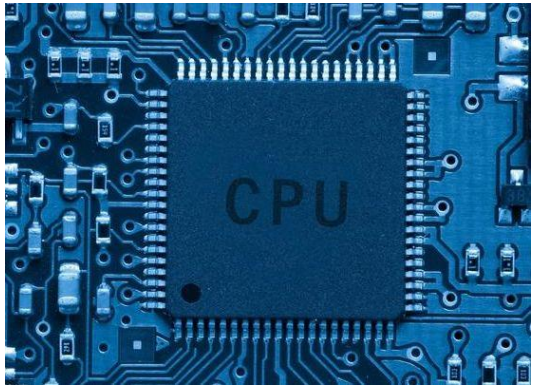






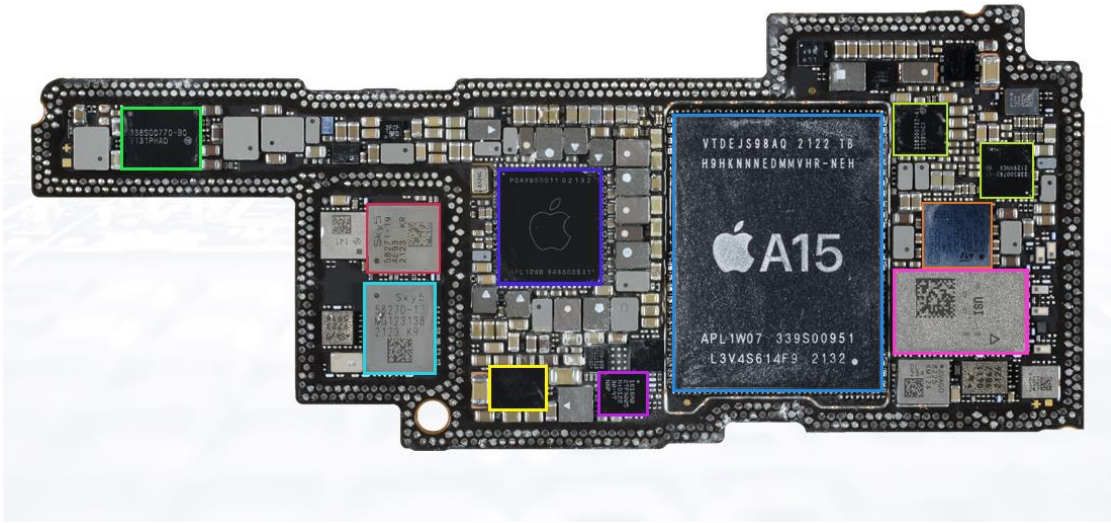

IC is the heart of all electronics



iPhone 13 Pro Teardown

Apple APL1W07 A15 Bionic PoP
(A15 AP + SK hynix 6GB LPDDR4X SDRAM)

Texas Instruments TPS65657B0 Display Power Supply

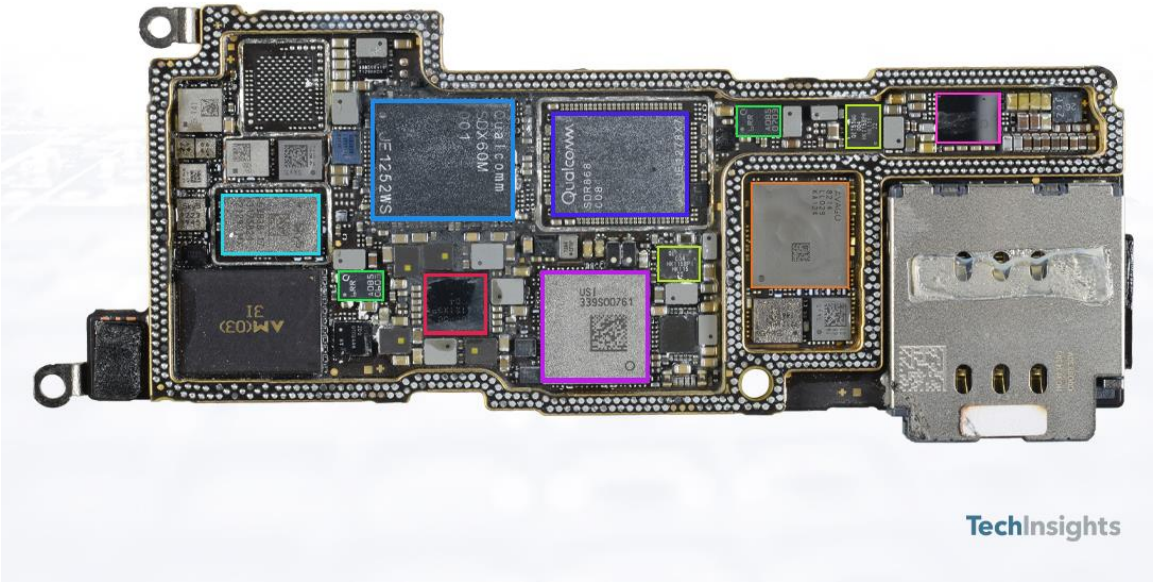


Qualcomm Snapdragon X60 5G Modem

Qualcomm RF Transceiver

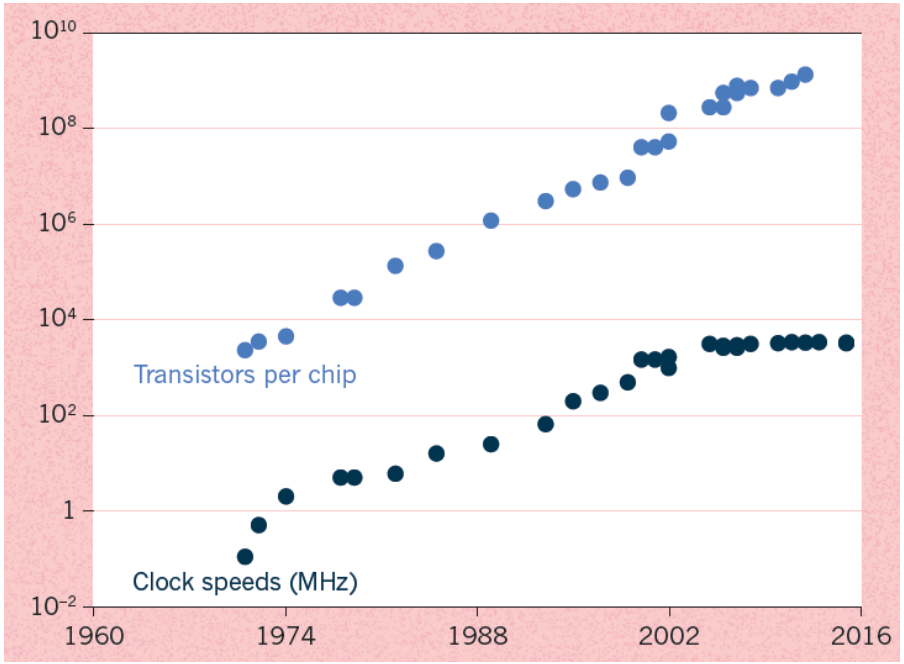
USI Wi-Fi/BT Wireless Combo Module

Broadcom Wireless Charging Receiver IC



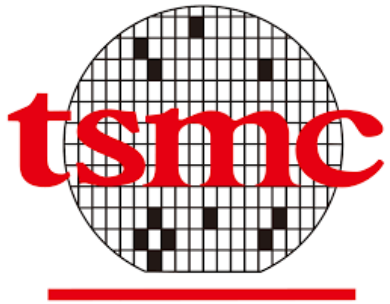
Moore's law

- The number of transistors on a microprocessor chip will double every two years.



Why Moore's law works very well in the past

- Manufacturers, material suppliers, apparatus-makers work together to launch the roadmap for the next year. ITRS
- Only a few types of chips are required, so that they can be sold in bulk quantities, which gives manufacturers enough cash to upgrade the equipment (many billions of dollars), e.g., photolithography.



CPU

GPU

Memory

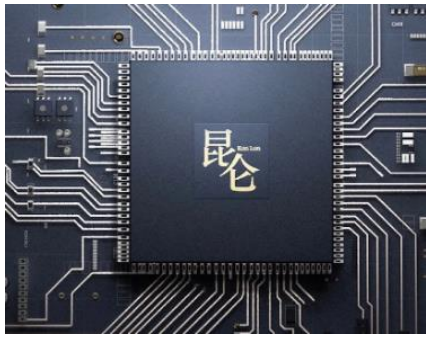
Why Moore's law not working now

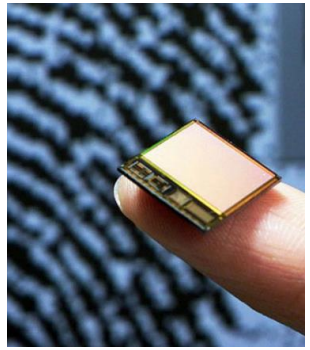
- Heating becomes problem as electrons move faster through a smaller device (e.g., 90 nm).
  - Stop increase "clock rate".
  - Multiprocessor. But it requires the task can be parallelized.
  - New materials which generate less heat, e.g., spintronic devices utilizing pure spin current generate zero heat.

$$\Delta x \Delta p \geq \frac{\hbar}{2}$$

- Small size down to 2-3 nanometer, quantum uncertainties make transistors unreliable.
  - Go 3D. Currently only works with memory chips. If microprocessors are stacked, they becomes hotter.
  - Invent "in-memory computing" devices e.g., using spintronics.

- Economic issues: Too many types of chips, manufacturers don't have enough profit to continue upgrade.





What's the future – More than Moore

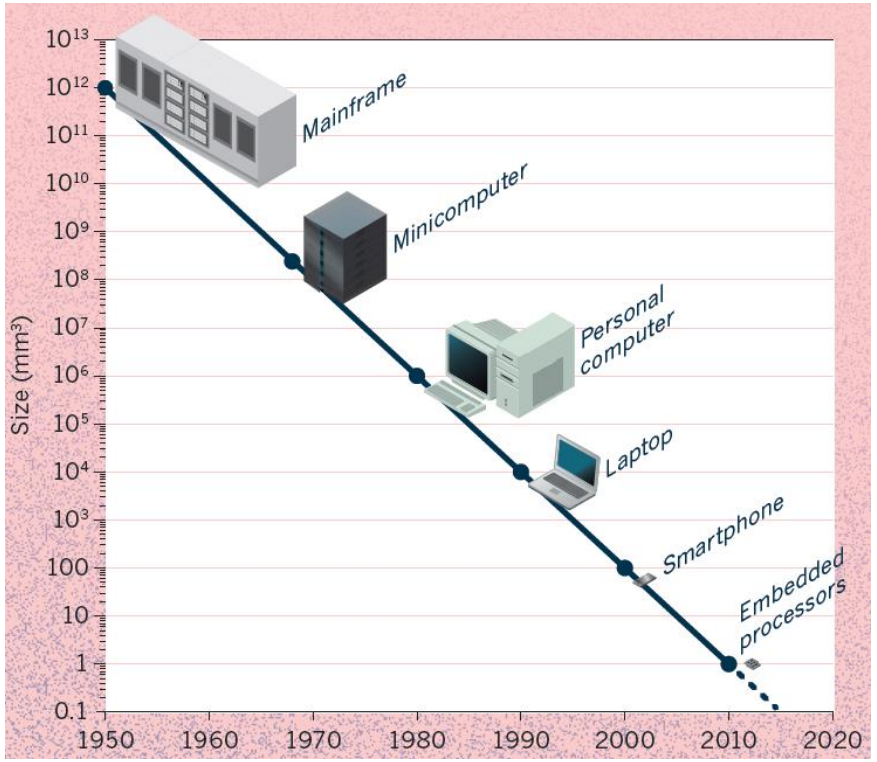
- **Functional devices**
  - Smart phones, tablets
  - Smart watches
  - Other wearable devices

These devices have very different requirements compared to servers, e.g., long battery power, better connectivity, security.

- **Neuromorphic computing**

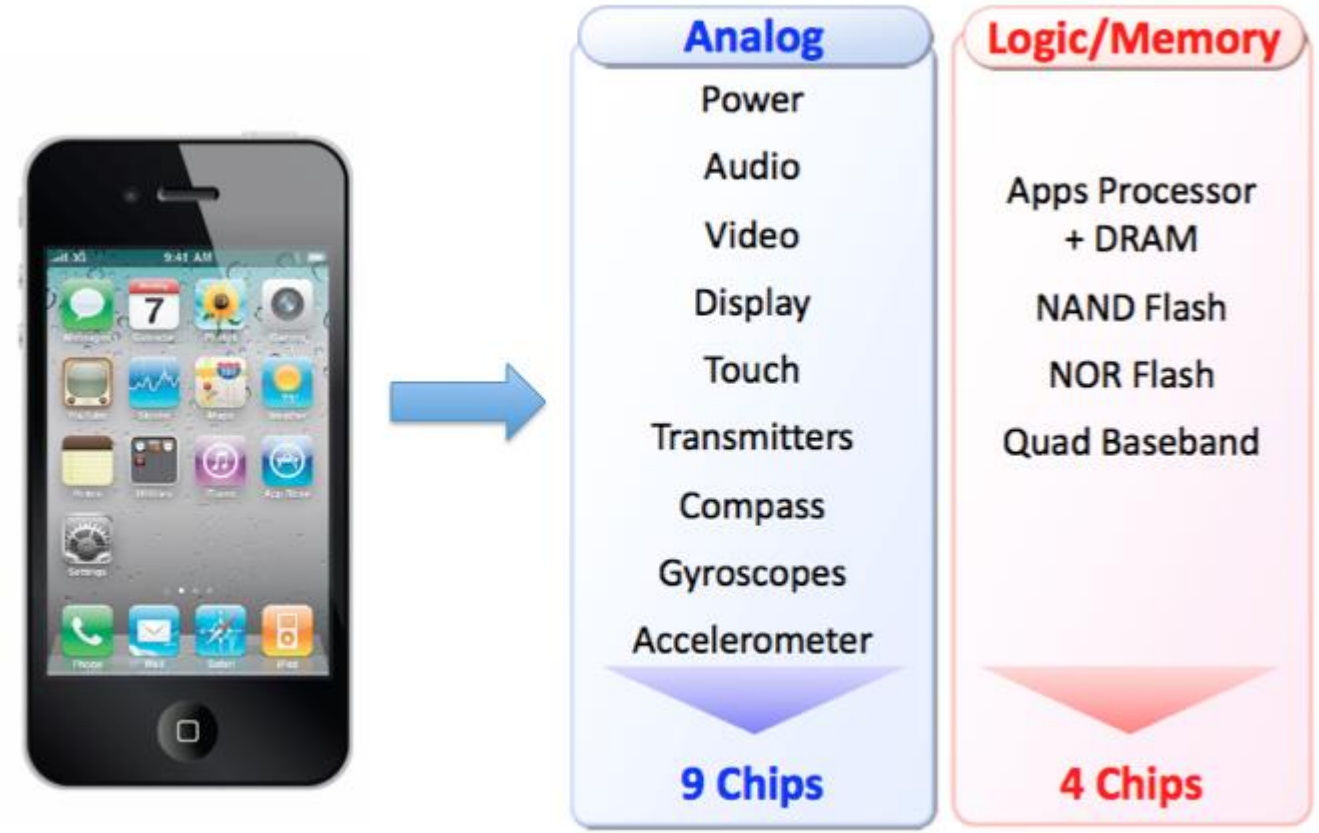
Processing information like our brain.

- **Quantum computing**
  - It can solve many formidable tasks for current computers.
  - Scaling issue doesn't matter.

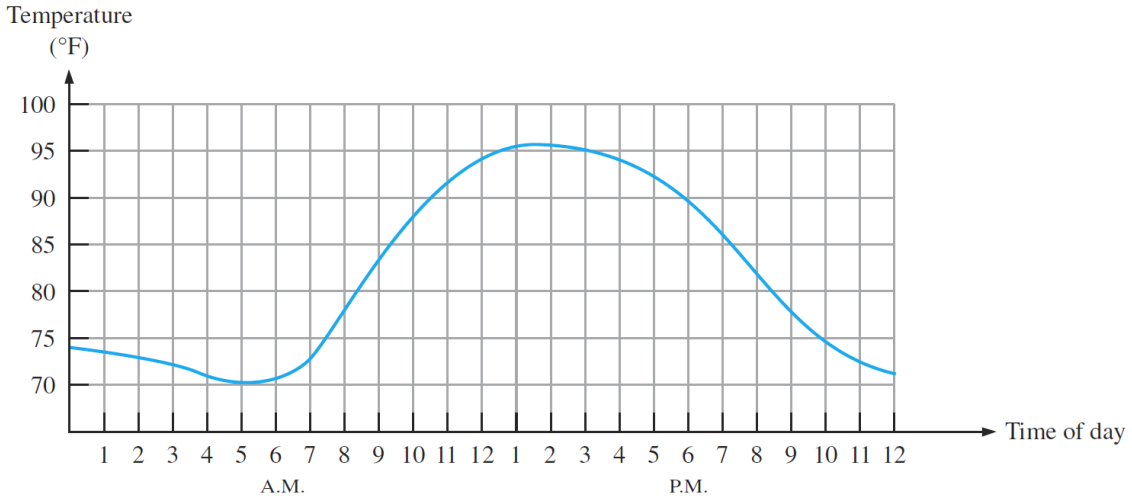


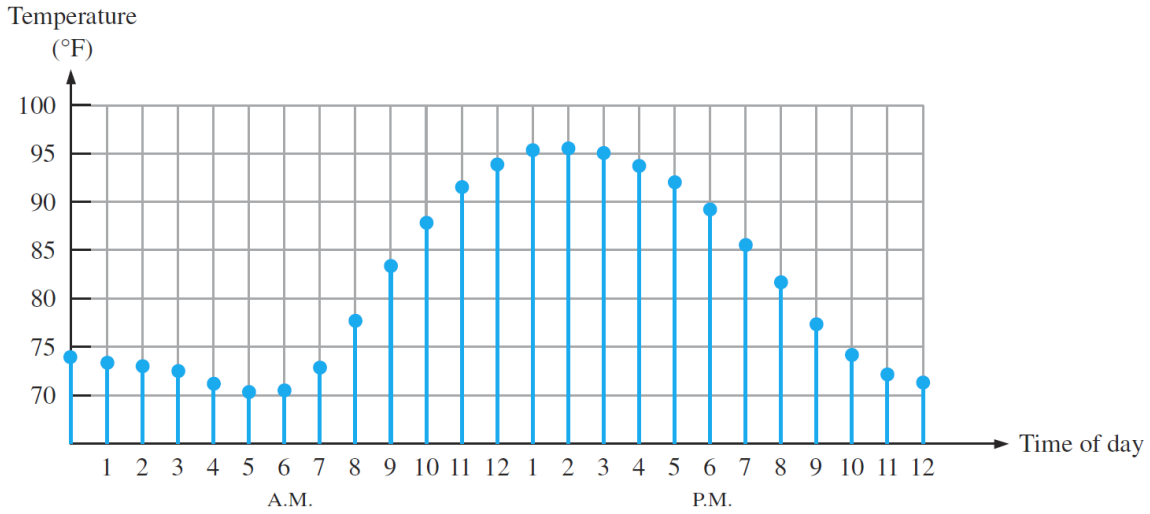
A new class of machine emerged every ten years

Analog chips vs digital chips



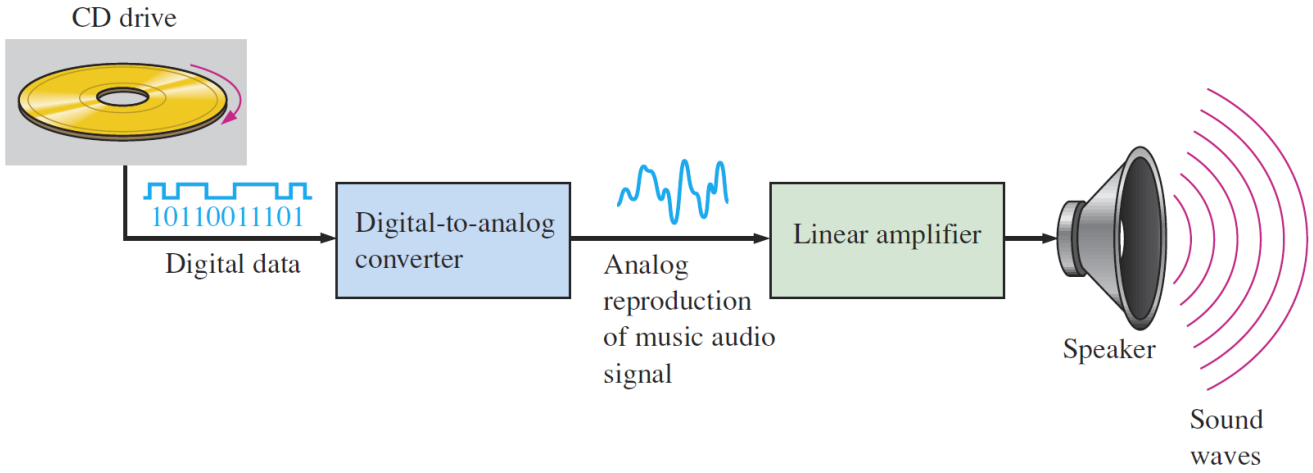
Digital and analog quantities





- Analog(digital) quantity has continuous(discrete) values.
- Digital data has the advantage in processing, transmission, storage and noise tolerance.

A System Using Digital and Analog Methods



- Music in digital form is stored on the CD.
- This digital data is converted into an analog signal which is an electrical reproduction of the original music.

The position of this course

- EE111: Electric Circuits

- 量子力学
- 固体物理
- 半导体物理
- 微电子器件（EE120）

- EE115A: Analog Circuits
- EE115B: Digital Circuits

- EE112: Analog Integrated Circuits
- EE113: Digital Integrated Circuits I

材料专业
固体电子
微电子专业
集成电路
微固学院
→ 电子科学与技术

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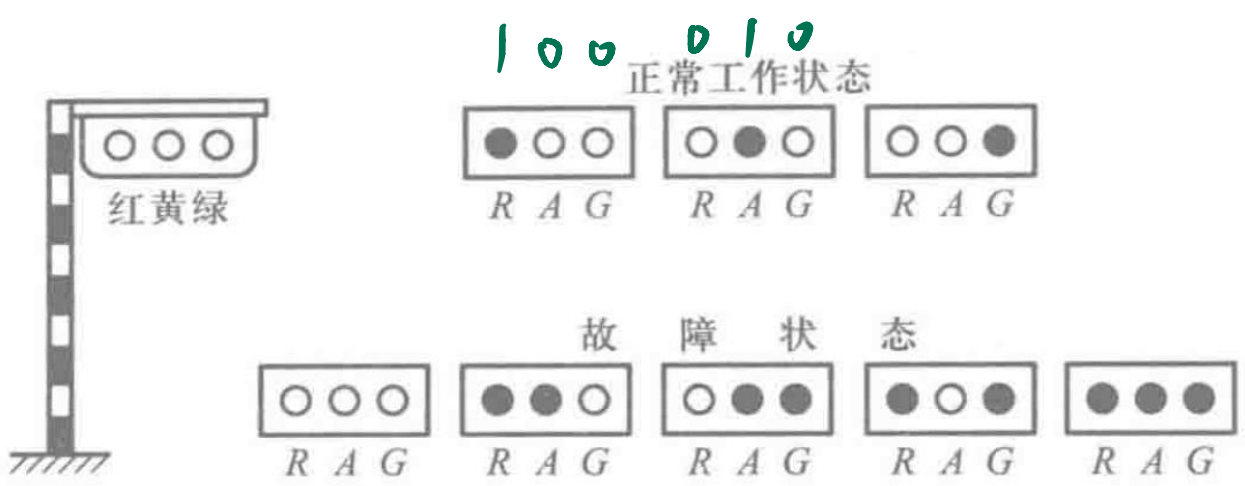
Chapter 1: Number Systems, Coding

568.23_{10} 101.110_{2} 3204_{8} $CA57_{16}$

Decimal Binary Octal Hexadecimal



Chapter 2: Logic Gates

NOT gate (Inverter)

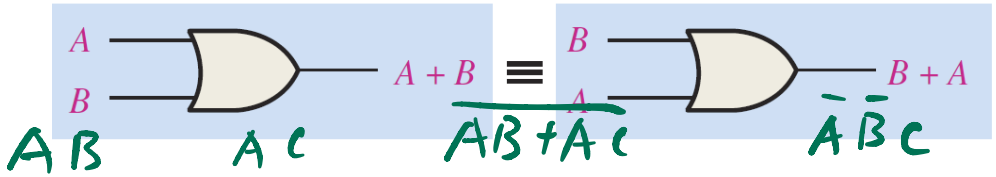
AND gate

OR gate

Chapter 3: Boolean Algebra

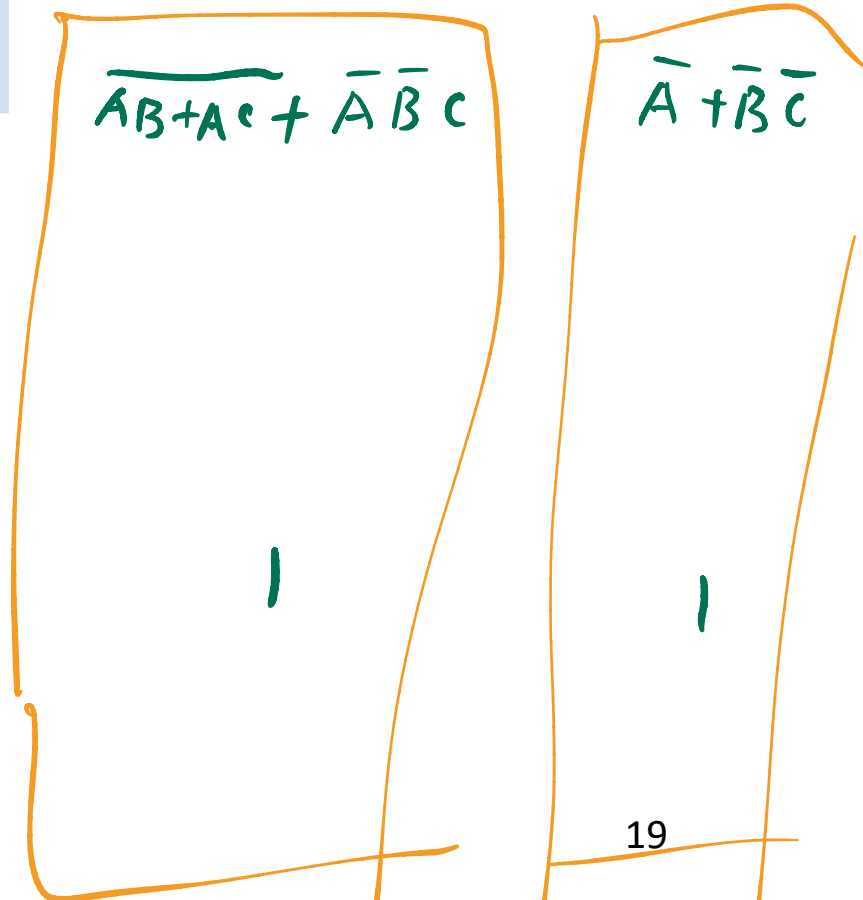
- In the 1850s, George Boole developed a mathematical system for formulating logic statements with symbols (Boolean algebra).

$A + B = B + A$



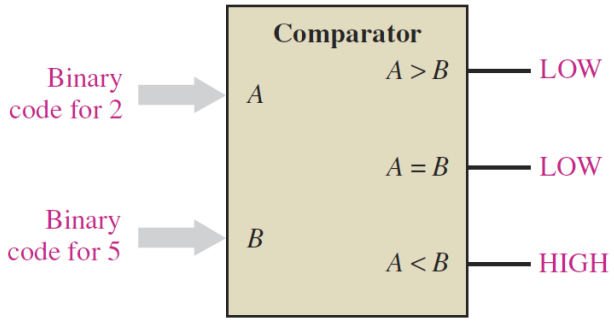
A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

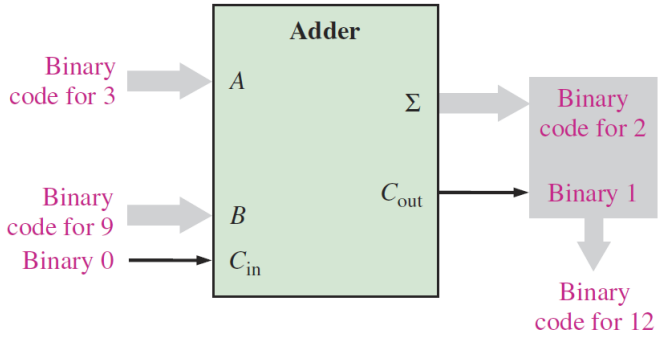
$$\overline{AB + AC} + \overline{A}\,\overline{B}C \equiv \overline{A} + \overline{B}\,\overline{C}$$



Chapter 4: Combinational Logic

- The output only dependent on the present input

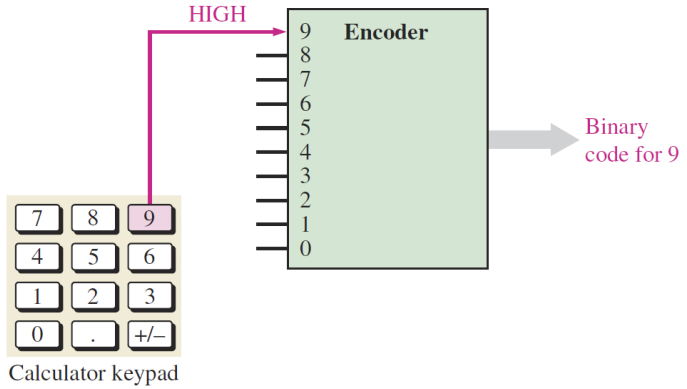


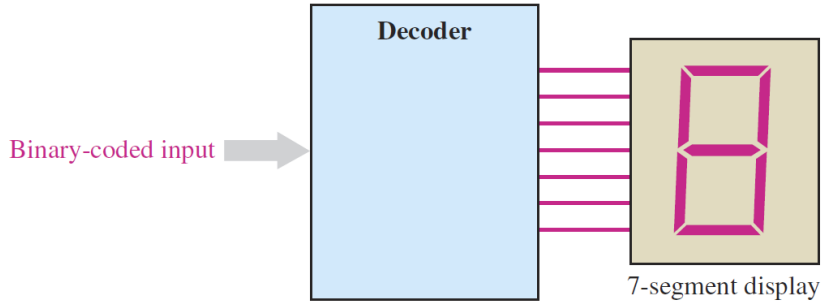


Subtraction

Multiplication

Division…

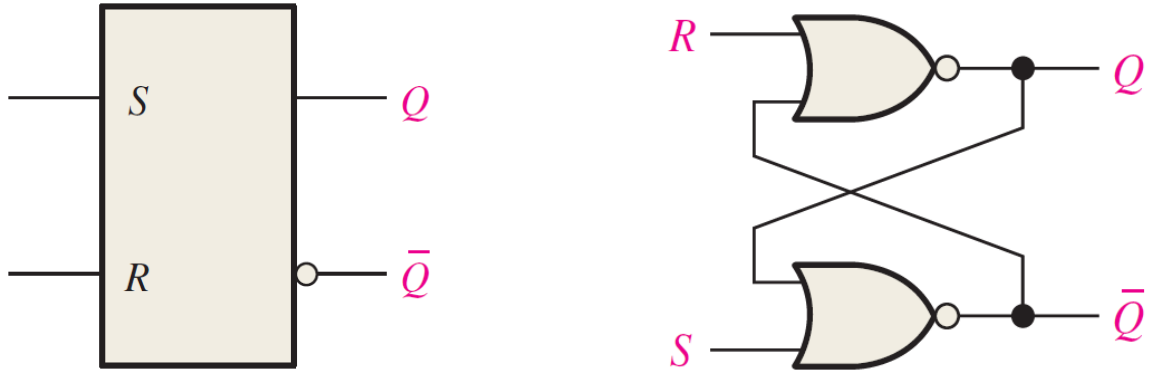




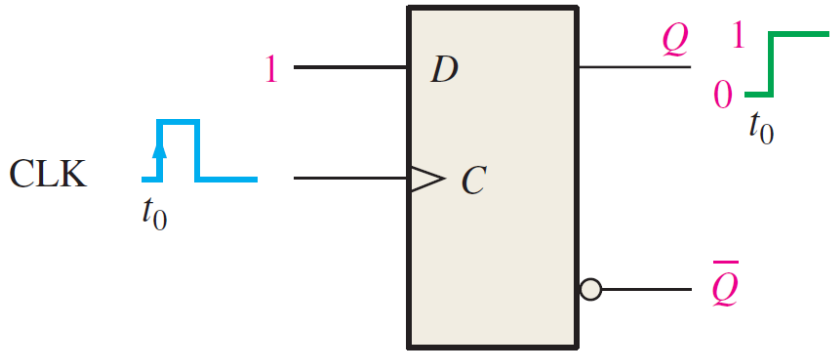
Chapter 6: Sequential Logic

- The output depends not only on the present input but also on the history of the input

Latch



Flip-Flop



Chapter 7: Storage

- Flip-flops
- Registers
- Semiconductor Memories: read-only memory (ROM), random-access memory (RAM)
- Magnetic Memories: hard disk (HDD)
- Optical Memories: CDs, DVDs, and Blu-ray Discs

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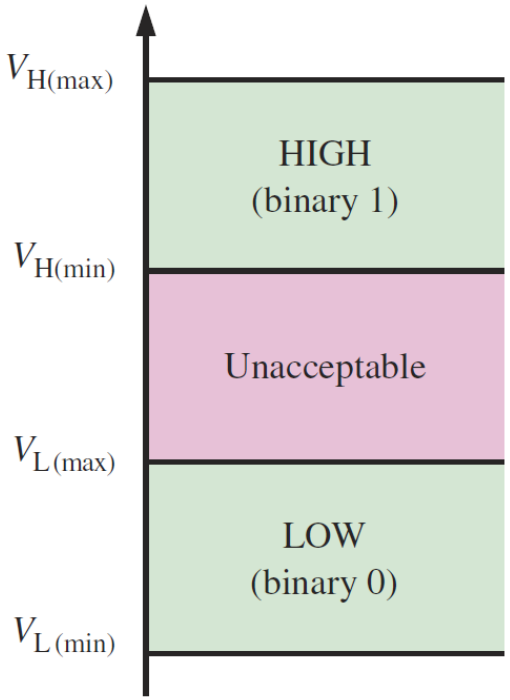
Reading materials

- Chapter 1 of Floyd book

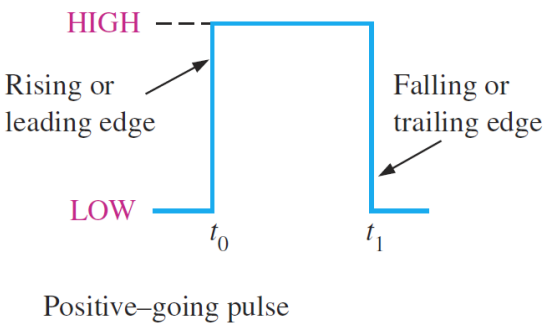
Binary Digits & Logic Levels

- Each of the two digits in the binary system, 1 and 0, is called a bit. In positive logic, 1(0) is represented by the higher(lower) voltage. The representation is opposite in negative logic.
- Groups of bits, called codes, are used to represent numbers, letters, symbols, instructions, and anything else required in a given application.
- The voltages used to represent a 1 and a 0 are called logic levels. A HIGH or LOW can be any voltage between specified minimum and maximum values.
- The voltage values between $V_{L(max)}$ and $V_{H(min)}$ are unacceptable for proper operation.

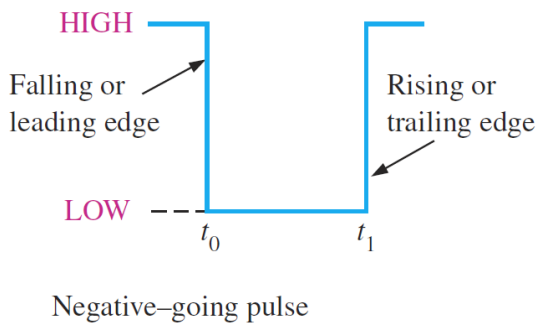


Digital Waveforms

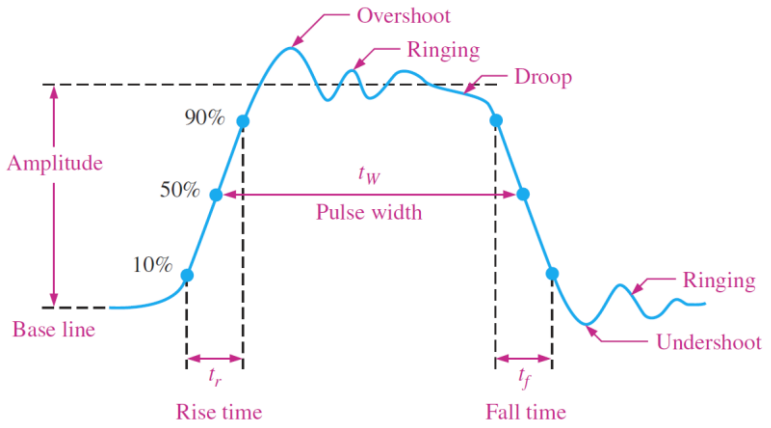
- Digital waveforms consist of voltage levels that are changing back and forth between the HIGH and LOW levels.
- It is common to measure rise time (t_r) from 10% to 90% of the pulse amplitude, similarly for the fall time t_f.
- The pulse width (t_W) is defined as the time interval between the 50% points on the rising and falling edges.



Positive–going pulse



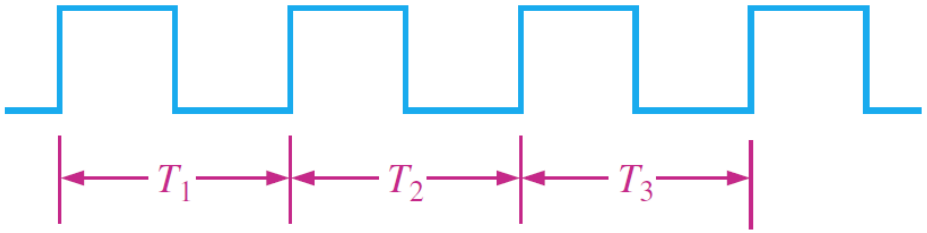
Negative–going pulse



Waveform Characteristics

- Most waveforms can be classified as either periodic or nonperiodic. A periodic pulse waveform is one that repeats itself at a fixed interval, called a period (T). Frequency (f) is the reciprocal of T and is measured in hertz (Hz). A nonperiodic pulse waveform does not repeat itself at fixed intervals.
- Duty cycle is the ratio of the t_W to T.

$$\text{Duty cycle} = \left(\frac{t_W}{T}\right)100\%$$

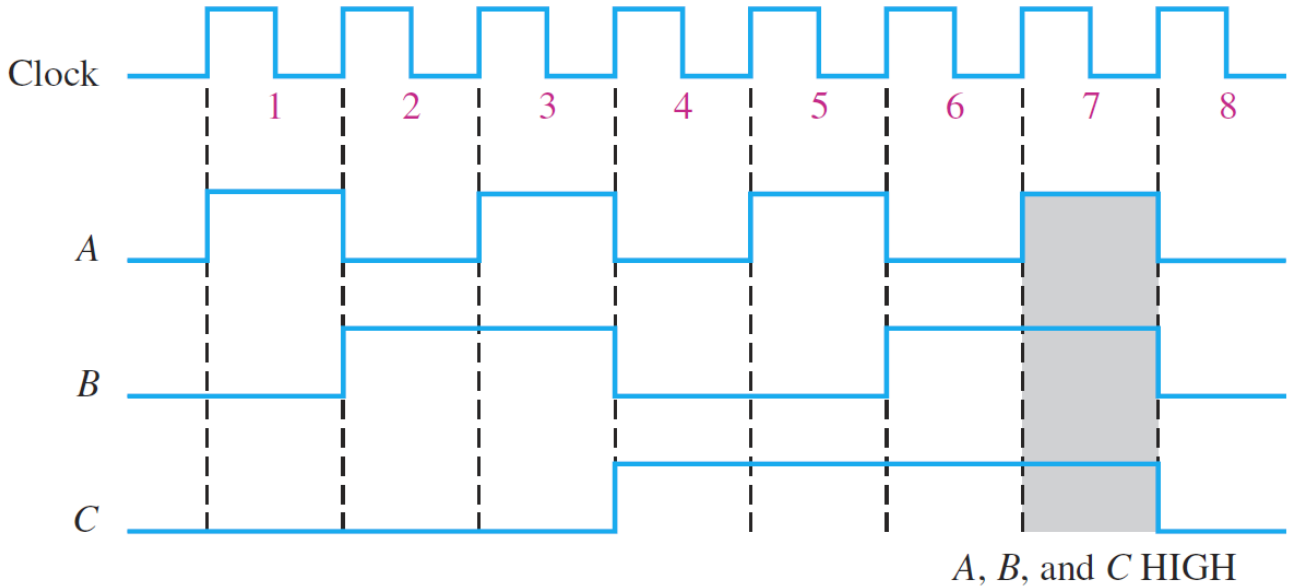


Period $= T_1 = T_2 = T_3 = \ldots = T_n$

Frequency $= \frac{1}{T}$

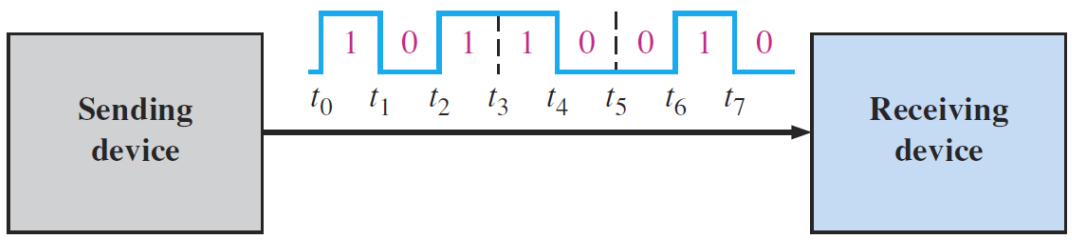
The Clock & Timing Diagrams

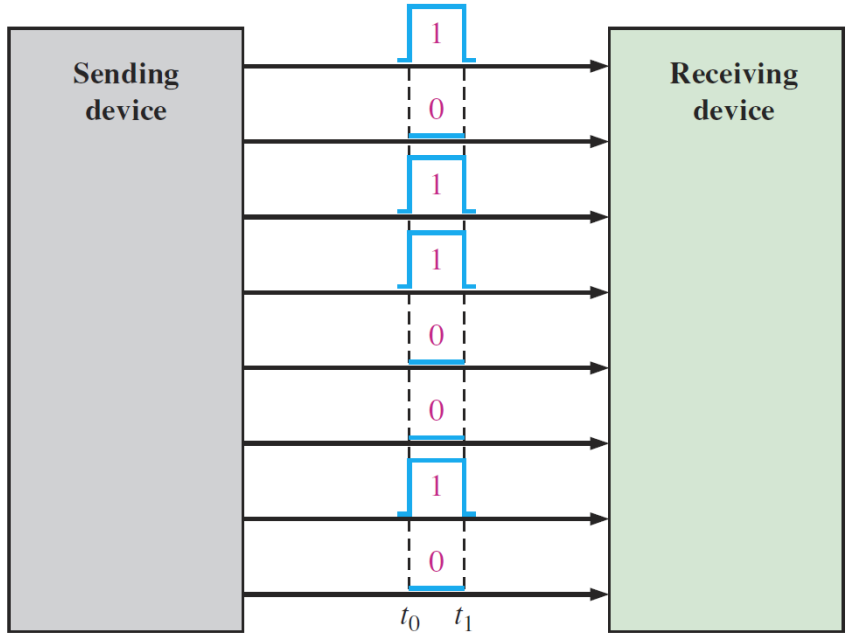
- In digital systems, all waveforms are synchronized with a basic timing waveform called the clock. The clock is a periodic waveform in which *T* equals the time for one bit.
- A timing diagram shows the actual time relationship of two or more waveforms and how each waveform changes in relation to the others.



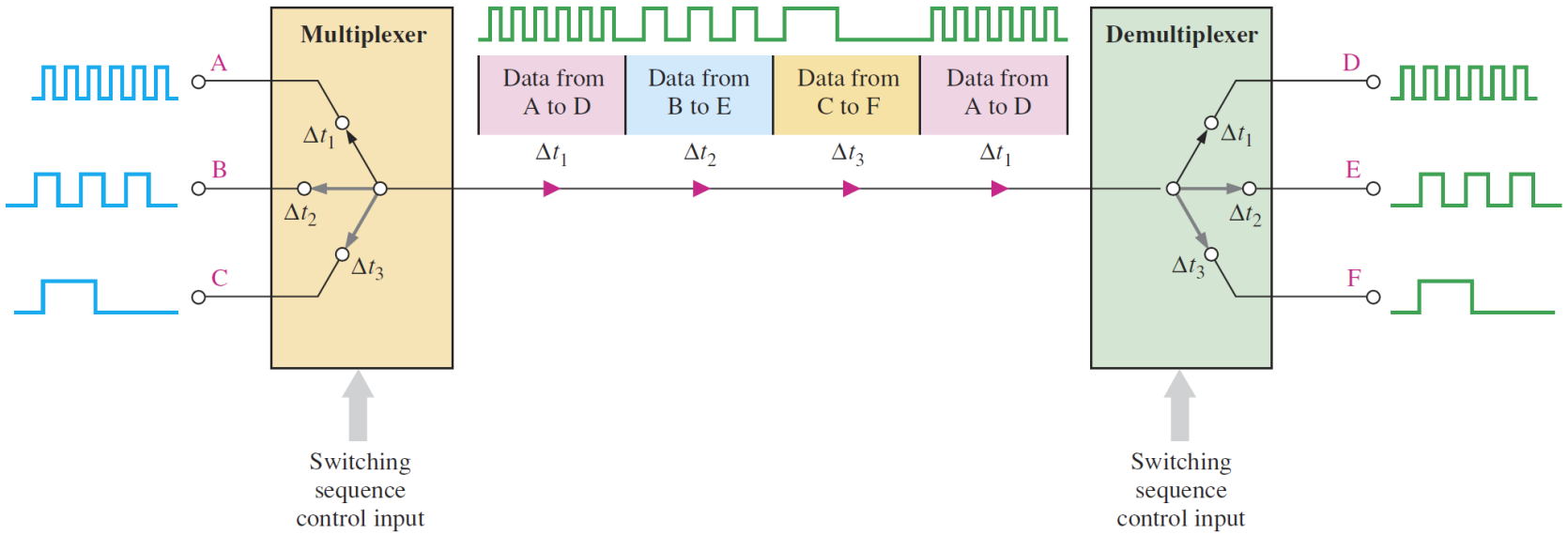
Data Transfer

- Binary data are transferred in either serial or parallel. For serial transfer, only one line is required. However, it takes longer to transfer a given number of bits.



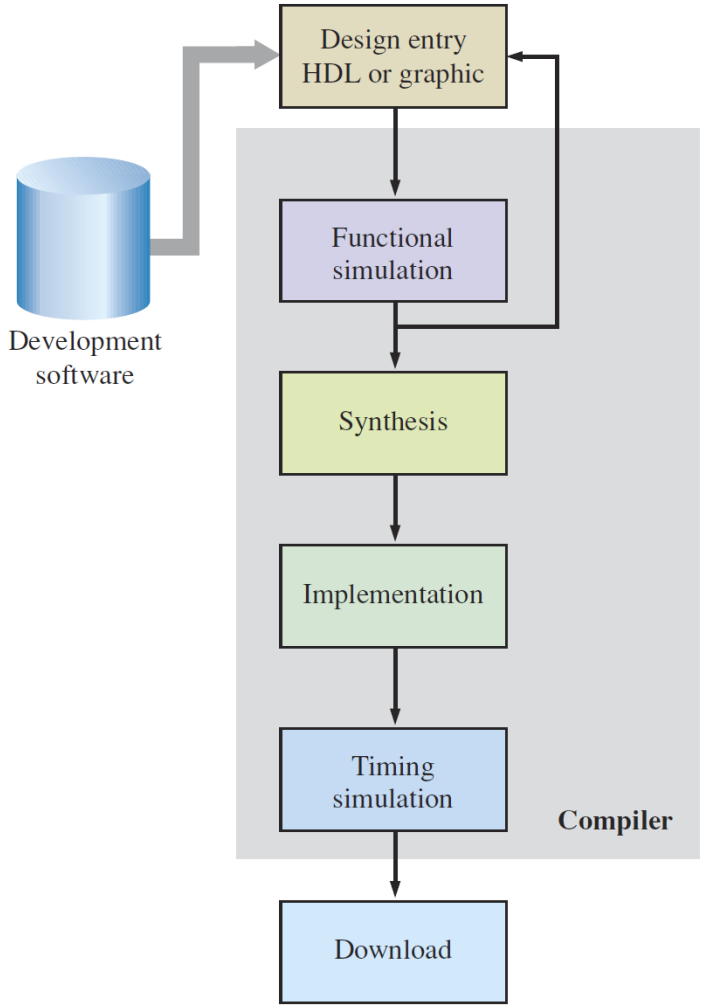


Combinational and Sequential Logic Functions



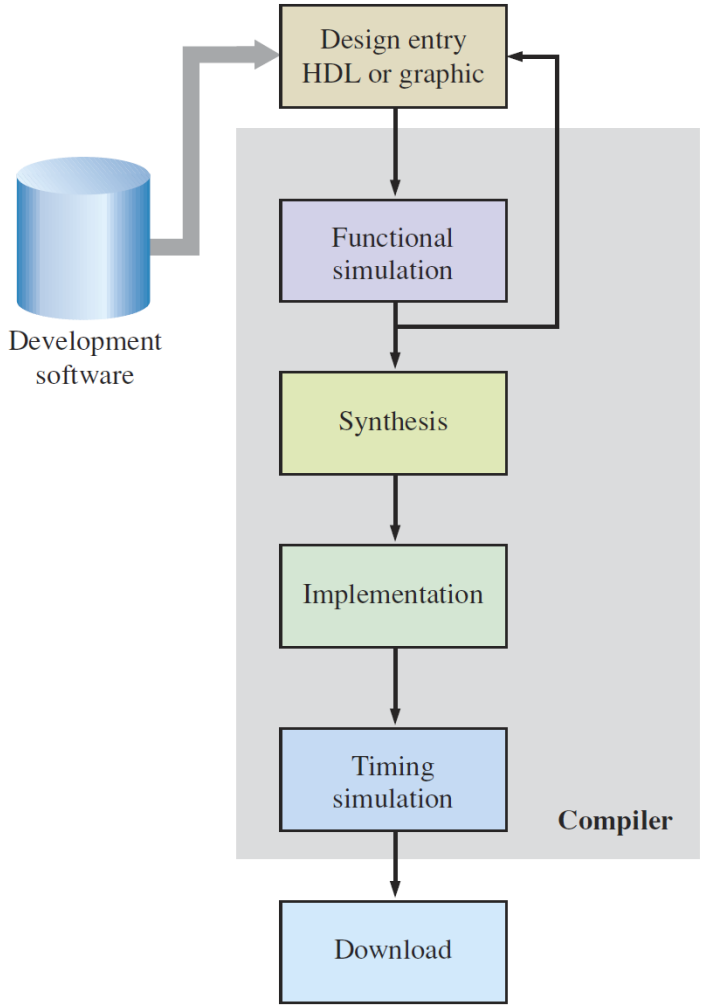
- Multiplexing and demultiplexing are used when data from several sources are to be transmitted over one line to a distant location and redistributed to several destinations

Design Entry



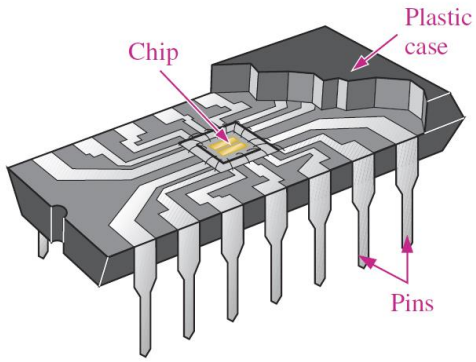
- The circuit must be entered into the design application software using text-based entry, graphic entry (schematic capture), or state diagram description. Text-based entry is accomplished with a hardware description language (HDL) such as VHDL, Verilog.
- Once a design has been entered, it is compiled. A compiler is a program that translates source code into object code in a format that can be downloaded to a target device.

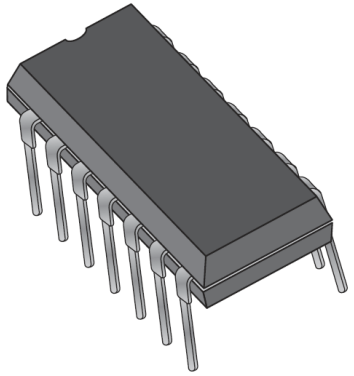
Design Entry



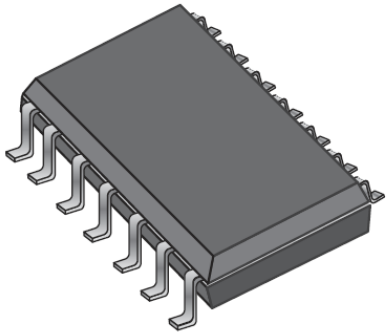
- Functional Simulation: The entered design is simulated by software to confirm that the logic circuit functions as expected.
- Synthesis is where the design is translated into a netlist.
- Implementation is where the logic structures described by the netlist are mapped into the actual device.
- The timing simulation is used to confirm that no design timing problems due to propagation delays.
- Download the design into the hardware.

IC Packages

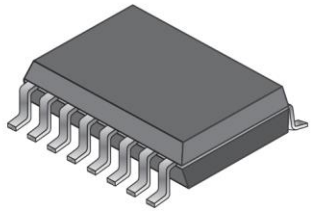




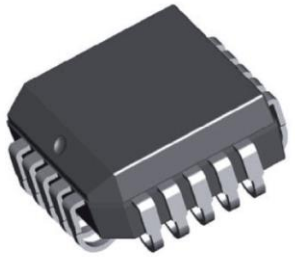
Dual in-line package (DIP)



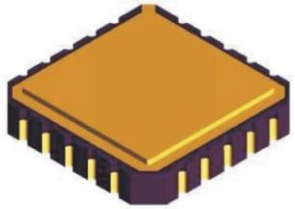
Small-outline IC (SOIC)



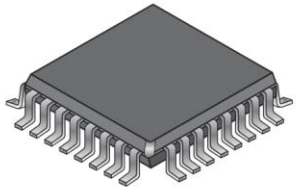
(a) SSOP (153 × 193 mils)



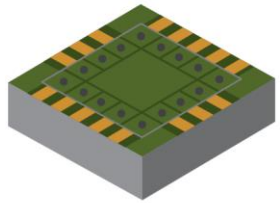
(b) PLCC (350 × 350 mils)



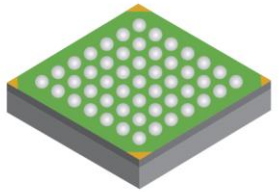
(c) LCC (350 × 350 mils)



(d) LQFP (7 × 7 mm)



(e) Laminate CSP bottom view (3.5 × 3.5 mm)



(f) FBGA bottom view (4 × 4 mm)

- Package pins are used to connect the chip and the outside world.
- IC packages are classified as either through-hole mounted (e.g., DIP) or surface mounted (e.g., SOIC)

Complexity Classifications for ICs

- Small-scale integration (SSI): up to ten equivalent gate circuits per chip.
- Medium-scale integration (MSI): 10 to 100 equivalent gates per chip.
- Large-scale integration (LSI): 100 to 10,000 equivalent gates per chip.
- Very large-scale integration (VLSI): 10,000 to 100,000 equivalent gates per chip.
- Ultra large-scale integration (ULSI): more than 100,000 equivalent gates per chip.

Integrated Circuit Technologies

- A circuit uses MOSFETs is CMOS (complementary MOS).
- A circuit uses bipolar junction transistors is called TTL (transistor-transistor logic).