Student Name: _____

Student Number: _____

School: _____

Year of Entrance: _____

Solution

ShanghaiTech University Final Examination Cover Sheet

Academic Year: 2021 to 2022 Term: Fall

Course-offering School: SIST

Instructor: Hengzhao Yang and Juan Li

Course Name: Digital Circuits

Course Number: EE 115B

Exam Instructions for Students:

1. All examination rules must be strictly observed throughout the entire test, and any form of cheating is prohibited.

2. Other than allowable materials, students taking closed-book tests must place their books, notes, tablets and any other electronic devices in places designated by the examiners.

3. Students taking open-book tests may use allowable materials authorized by the examiners. They must complete the exam independently without discussion with each other or exchange of materials.

For Marker's Use:

Section	1	2	3	4	5	6	7	8	9	10	Total
Marks											
Recheck											

Marker's Signature:
Date:

Rechecker's Signature:
Date:

1. Short questions. (10 points. 3 points for (b) and 1 point each for others.)

(a) Convert $(25)_{10}$ to BCD.

$(2\ 5)_{10} = (0010\ 0101)_{BCD}$

0010 0101

(b) Complete the truth table for the **XNOR** gate (2 points) and draw its circuit symbol (1 point).

Input A	Input B	Output X
0	0	1
0	1	0
1	0	0
1	1	1

(c) Determine the odd parity bit for 1101001.

4 '1's ⇒ '1' for odd parity bit.

(d) What does "VHDL" stand for?

VHSIC (Very High Speed Integrated Circuits)

Hardware Description Language

(e) What does "FPGA" stand for?

Field Programmable Gate Array

(f) (True or False) In VHDL, the CASE statement can only appear in a PROCESS.

True

(g) (True or False) In VHDL, the statements inside a PROCESS are sequential.

True

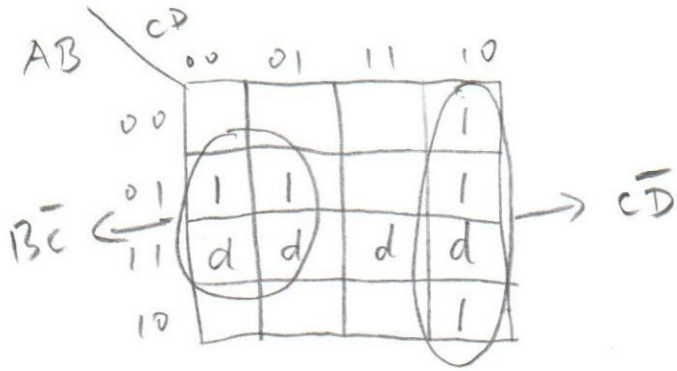
(h) (True or False) The output of the Moore type finite state machine depends on both the state and the present input.

False

2. Develop the minimum SOP and POS expressions for the following function using Karnaugh map. (10 points. 5 points each.)

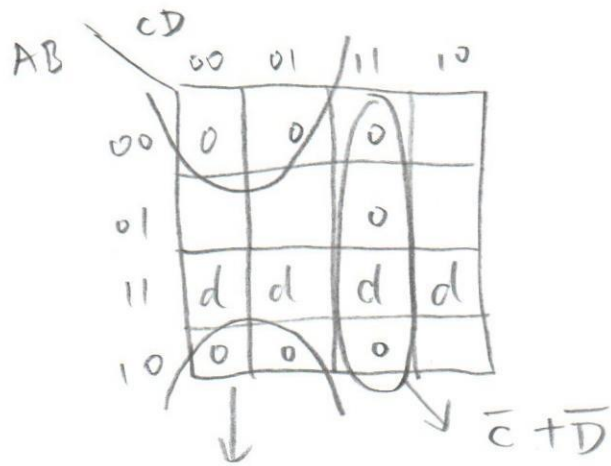
$$\boldsymbol{Y(A,B,C,D) = \sum m(2,4,5,6,10) + D(12,13,14,15)}$$

(1) SOP



$$Y = B\bar{C} + C\bar{D}$$

(2) POS



$$Y = (B+C)(\bar{C}+\bar{D})$$

3. Develop the minimum SOP expression for the following function using the Quine-McCluskey method. (20 points.)

$$Y(A,B,C,D) = \sum m(2,3,7,8,10,11,14)$$

① Minterms

2	3	7	8	10	11	14
0010	0011	0111	1000	1010	1011	1110

② Grouping minterms

table 1

group 1	2	0010	✓
	8	1000	✓
group 2	3	0011	✓
	10	1010	✓
group 3	7	0111	✓
	11	1011	✓
	14	1110	✓

table 2

first-round combinations

2,3	001-	✓
2,10	-010	✓
8,10	10-0	
3,7	0-11	
3,11	-011	✓
10,11	101-	✓
10,14	1-10	

table 3

second-round combinations

2,3,10,11	-01-
2,10,3,11	-01-

End: no further combinations can be done.

This page is intentionally left blank for Problem 3.

PIs:

table 2	8, 10	10 − 0	$A\bar{B}\bar{D}$
	3, 7	0 − 11	$\bar{A}CD$
	10, 14	1 − 10	$AC\bar{D}$
table 3	2, 3, 10, 11	−01−	$\bar{B}C$

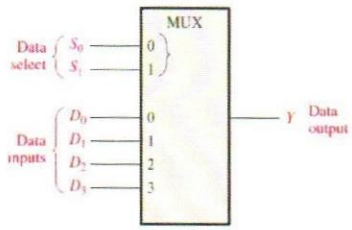
③ PI chart

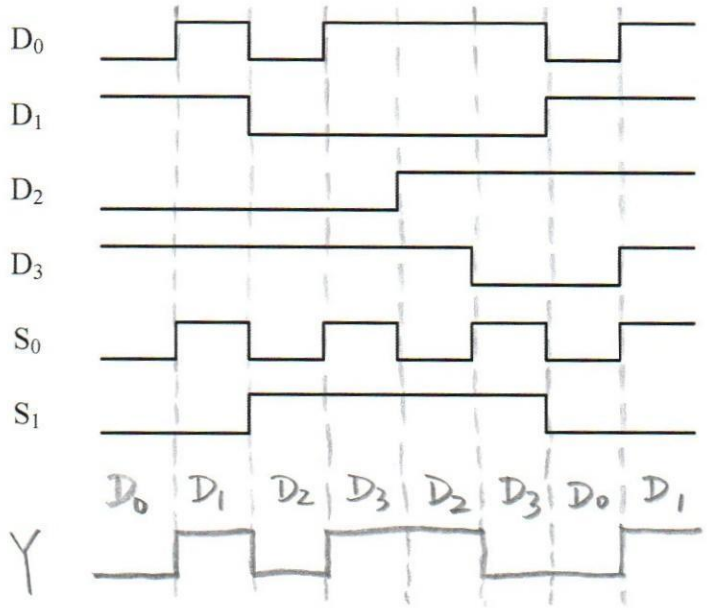
index	PI	2	3	7	8	10	11	14
8, 10	$A\bar{B}\bar{D}$				(X)	X		
3, 7	$\bar{A}CD$		X	(X)				
10, 14	$AC\bar{D}$					X		(X)
2, 3, 10, 11	$\bar{B}C$	(X)	X			X	(X)	

All PIs are EPIs.

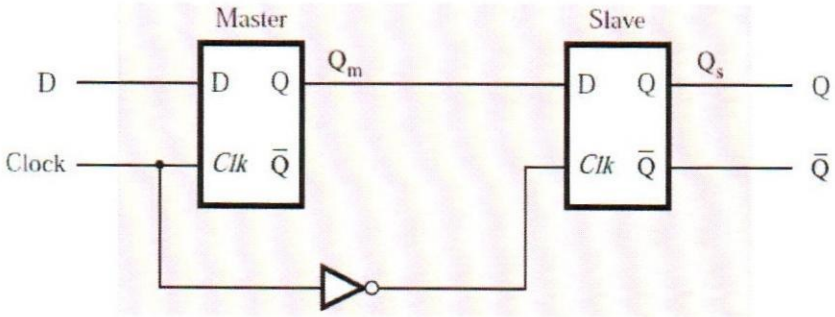
$$Y = \bar{B}C + A\bar{B}\bar{D} + \bar{A}CD + AC\bar{D}$$

4. Draw the output (Y) waveform given the following inputs to the 4-to-1 MUX. (8 points.)





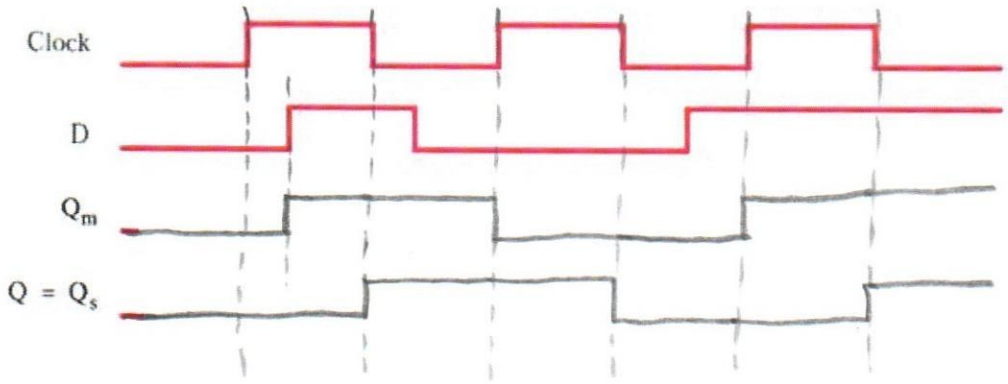
5. Consider the circuit below. (12 points.)



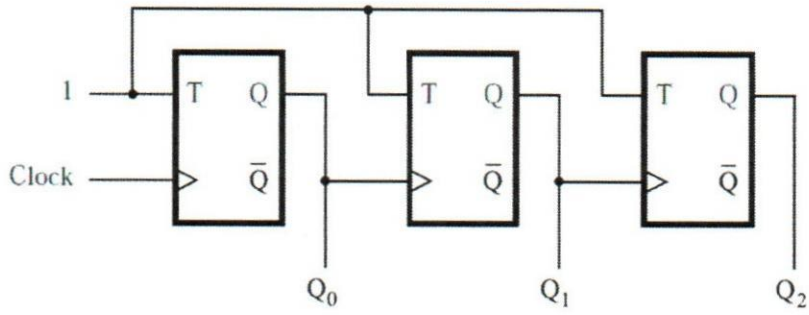
(a) (True or False, 2 points.) The "Master" and "Slave" stages are two gated D latches.

True

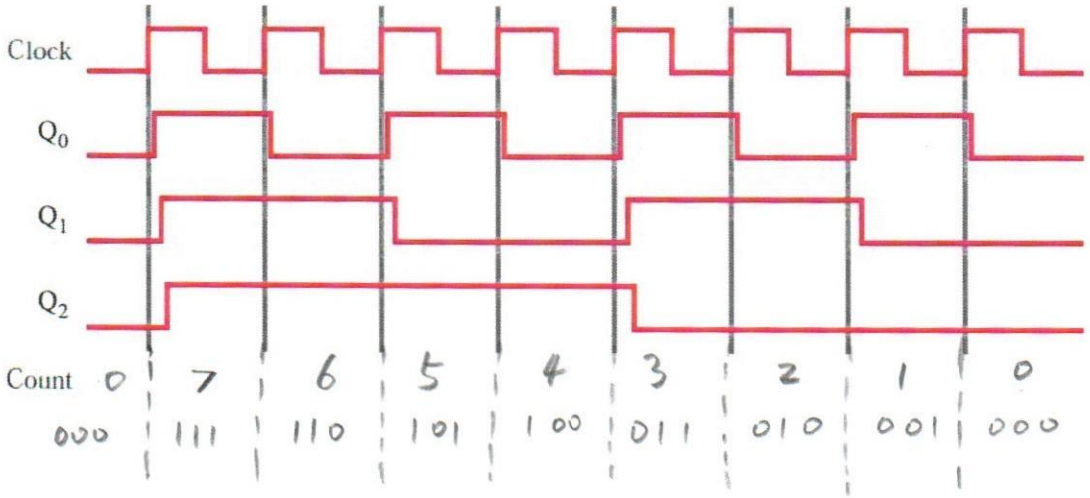
(b) (10 points.) Draw the timing diagram for Qm and Q (Q=Qs). Assume that the initial conditions are Qm=Q=0 as shown in the graph below. Ignore the propagation delays.



6. Consider the counter below. (20 points.)



(a) (16 points.) Analyze its binary sequence and identify its modulus. Assume that the initial states are Q_0=Q_1=Q_2=0. The count is represented by "$Q_2Q_1Q_0$" with Q_2 as the MSB and Q_0 as the LSB.



Sequence : 111, 110, 101, 100, 011, 010, 001, 000.

Modulus : 8.

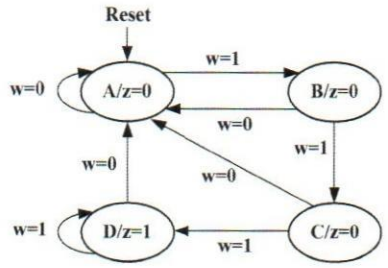
(b) (True or False, 2 points.) This counter is a synchronous counter.

False

(c) (True or False, 2 points.) This counter is an up-counter.

False

7. Consider the state diagram below. The input is "w" and the output is "z". (20 points.)



(a) Convert the state diagram to a state table. (5 points.)

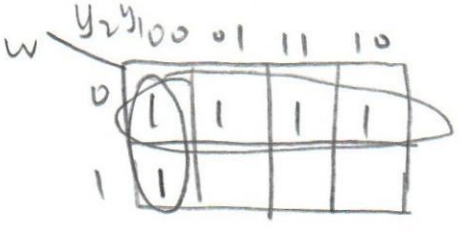
Present State	Next State w=0	Next State w=1	Output z
A	A	B	0
B	A	C	0
C	A	D	0
D	A	D	1

(b) Convert the state table developed in step (a) to a state-assigned table using the following configurations. The present state variables are "y_2y_1". The next state variables are "Y_2Y_1". The state assignment is "11" for A, "00" for B, "01" for C, and "10" for D. (5 points.)

Present State y_2y_1	Next State w=0 Y_2Y_1	Next State w=1 Y_2Y_1	Output z
11	11	00	0
00	11	01	0
01	11	10	0
10	11	10	1

(c) Based on the state-assigned table developed in step (b), determine the minimum SOP expression for the next state variable "Y_1". (10 points.)

w	y_2	y_1	Y_1
0	1	1	1
0	0	0	1
0	0	1	1
0	1	0	1
1	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0



$$Y_1 = \bar{w} + \bar{y}_2\bar{y}_1$$