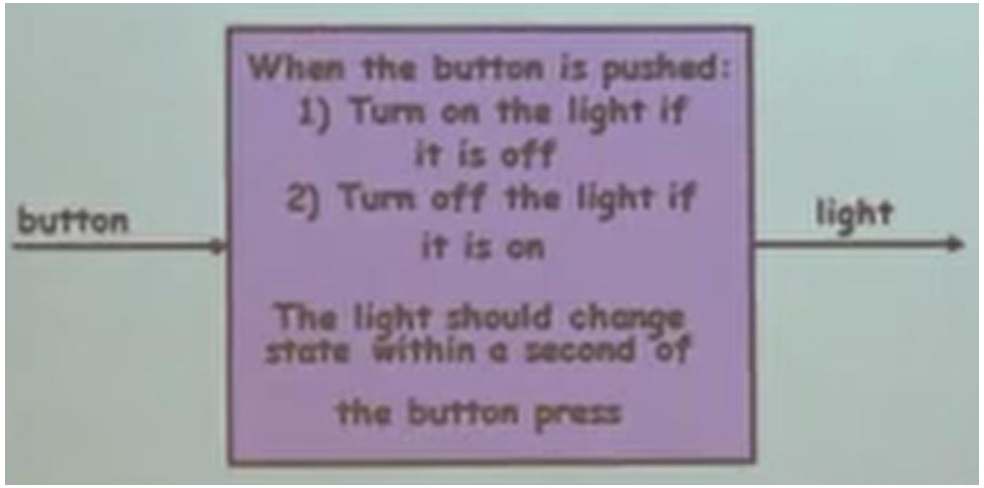
Something We Cannot Build

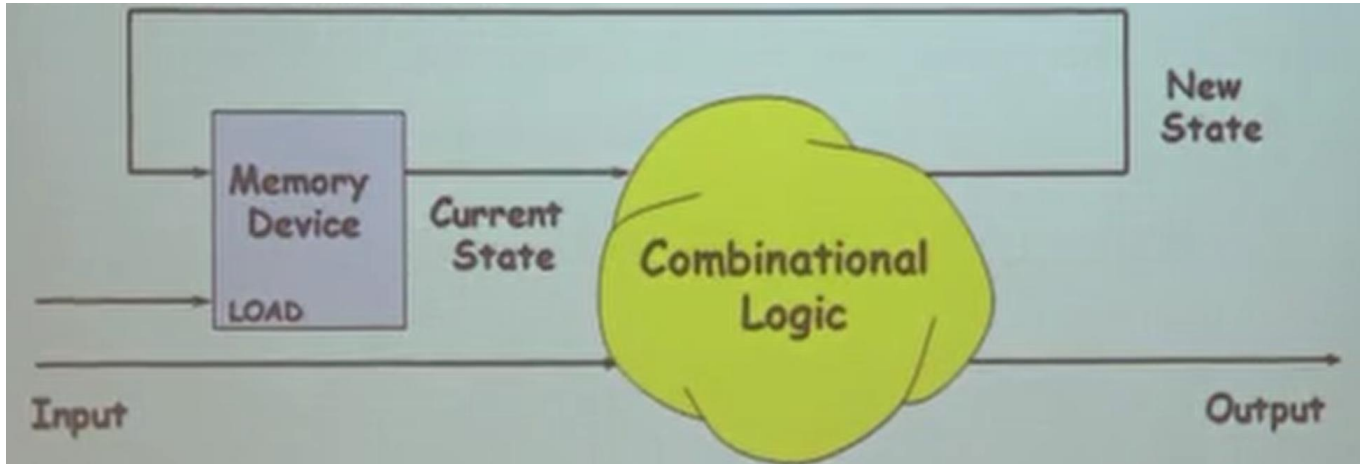


Think about it:

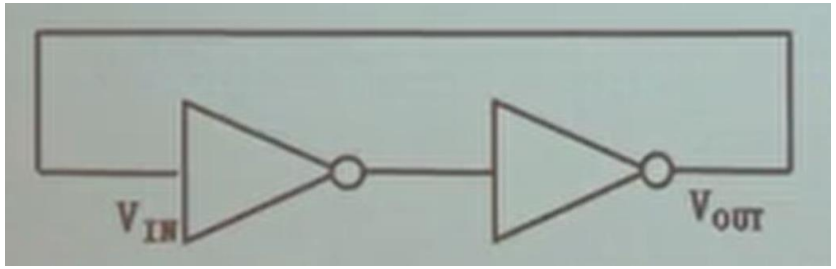
- Can we built the circuit using the combinational logic?
- If not, what is missing here?

Something We Cannot Build

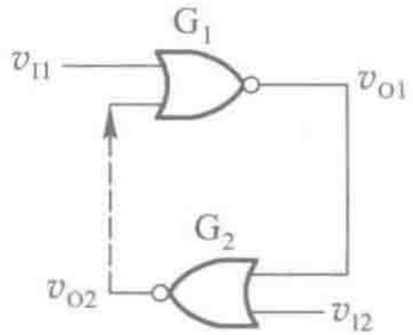
- One needs the storage unit
- The output is triggered by an event instead of a value.



Use feedback to store a bit

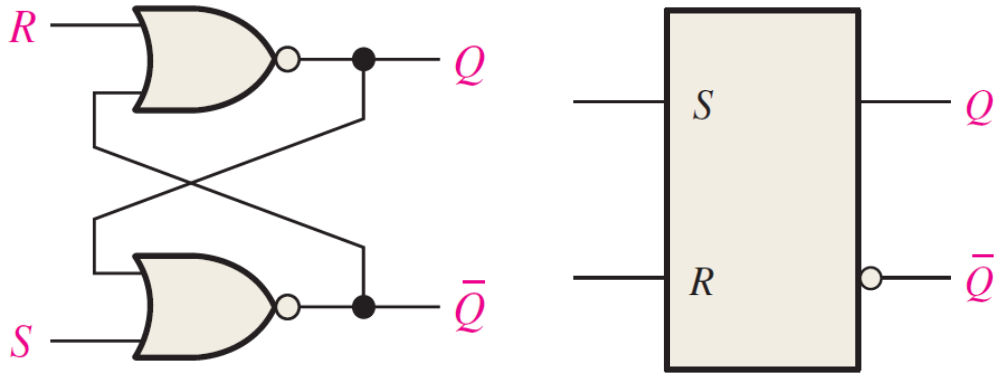


Add control terminals



Question: if we want to maintain the state, what voltage should be applied to v_{11} and v_{12}?

S-R (SET-RESET) Latch



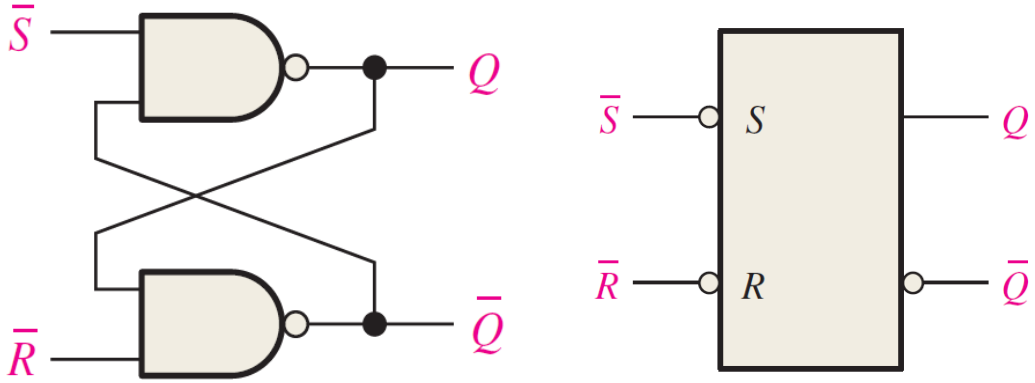
- The output of each gate is connected to an input of the opposite gate to provide a feedback.
- Even the input is removed, the output state is still maintained.
- This is the active high input SR latch

S_D	R_D	Q	Q^*
0	0	0	0
0	0	1	1
1	0	0	1
1	0	1	1
0	1	0	0
0	1	1	0
1	1	0	0①
1	1	1	0①

① The state is undetermined when *S* and *R* are removed simultaneously

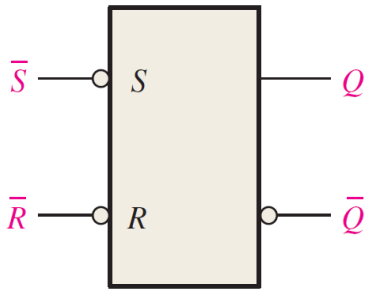
S-R (SET-RESET) Latch

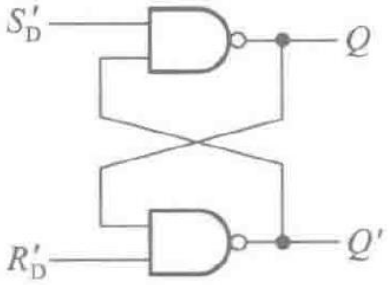
Active low input SR latch

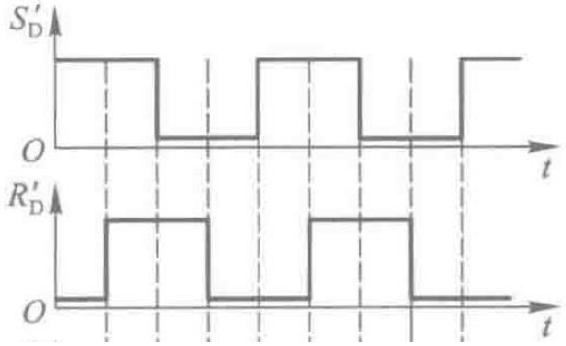


S'_D	R'_D	Q	Q^*
1	1	0	0
1	1	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
0	0	0	1①
0	0	1	1①

S-R (SET-RESET) Latch

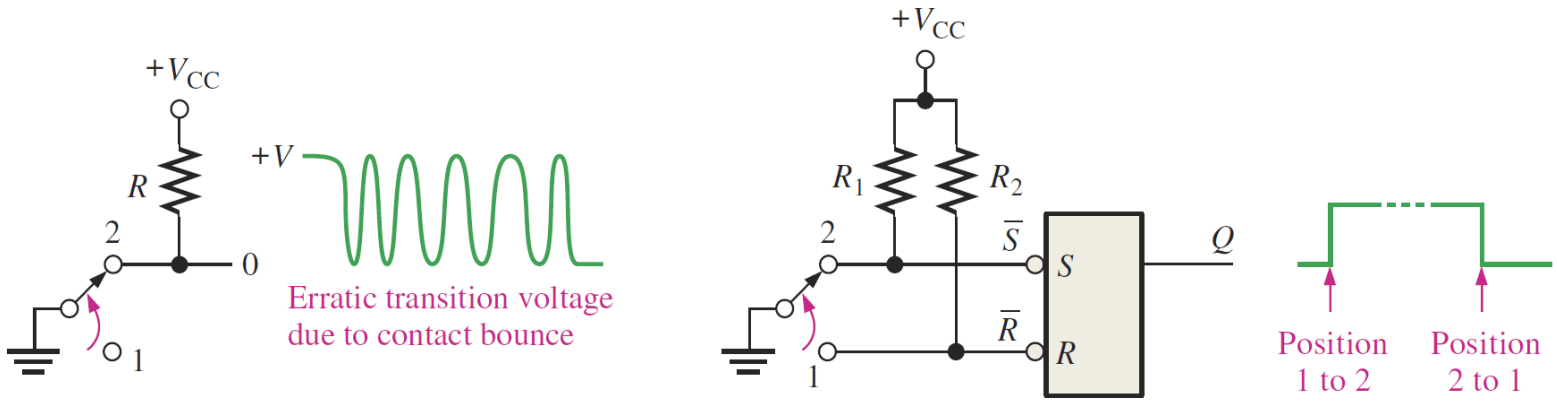






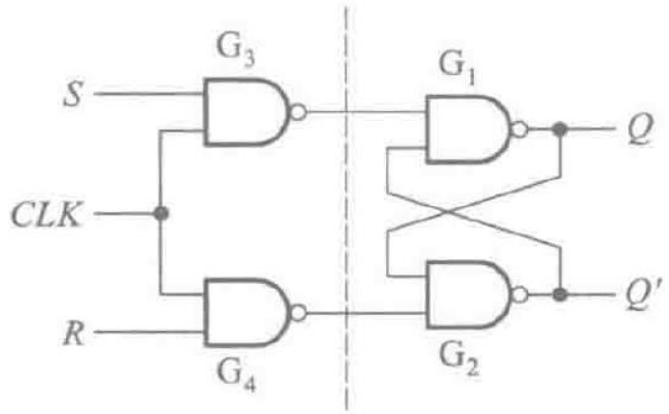
Question: plot the waveform of *Q* and *Q*'

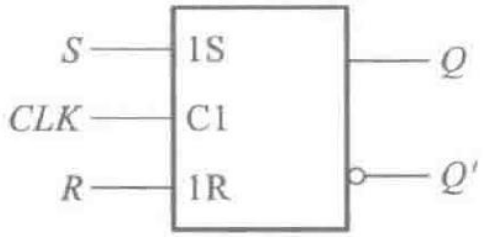
S-R Latch as a Contact-Bounce Eliminator



- The closure of a mechanical switch is accompanied by the contact bounce
- An S-R latch can be used to eliminate the effects of switch bounce.
- The 1 to 2 transition sets the latch. Any further voltage spikes on the S input do not affect the latch.
- Similarly, a clean transition from HIGH to LOW is made for a 2 to 1 transition .

The gated S-R Latch

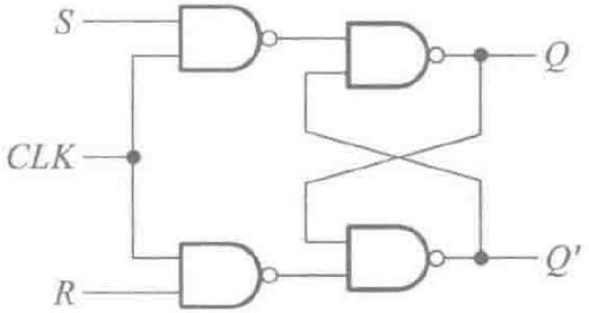


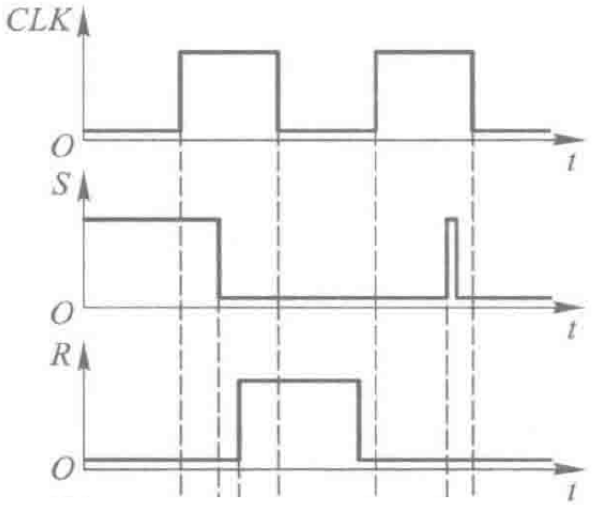


CLK	S	R	Q	Q^*
0	×	×	0	0
0	×	×	1	1
1	0	0	0	0
1	0	0	1	1
1	1	0	0	1
1	1	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	1	0	1①
1	1	1	1	1①

- C1 denotes that *CLK* is a control signal with the numbering 1
- 1S and 1R denotes that *S* and *R* are controlled by C1
- The gated latch is a level-sensitive device

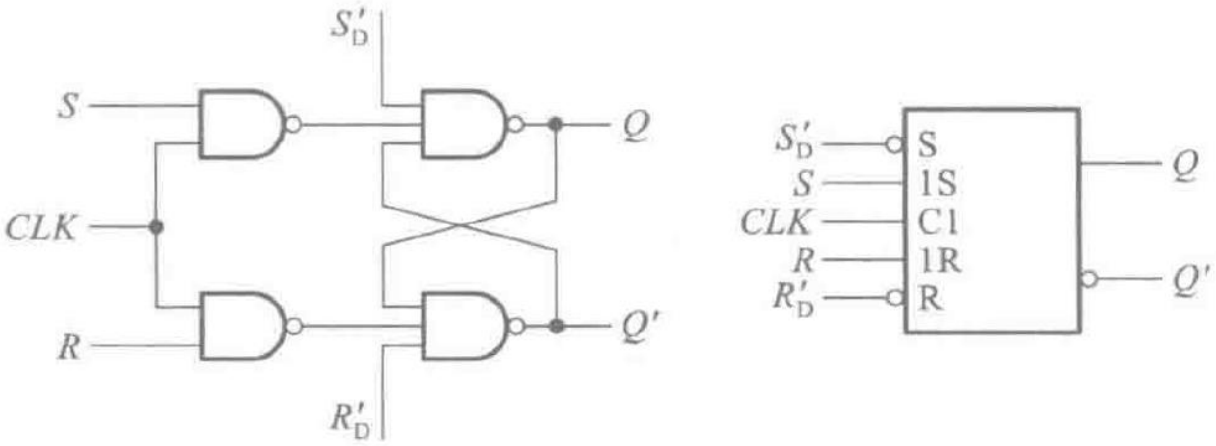
The gated S-R Latch





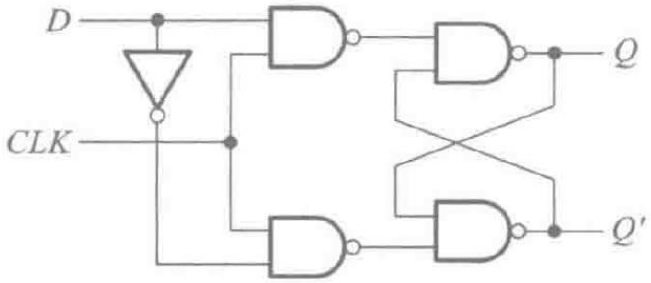
Question: plot the waveform of *Q* and *Q'*, assume the initial *Q* is 0

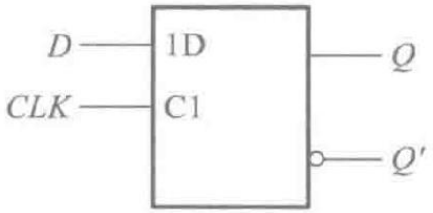
The asynchronous gated S-R Latch



- When S_D' and R_D' are not used for asynchronous set and reset, one should set them to 1
- When they are used, *CLK* should be set to 0

The gated D Latch

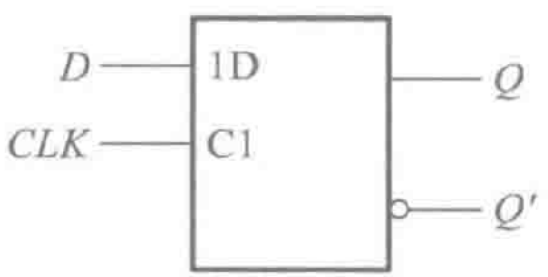


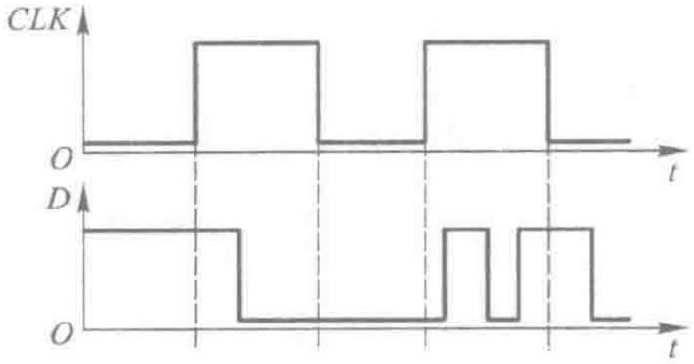


CLK	D	Q	Q^+
0	×	0	0
0	×	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

- Compared to the S-R latch, it lost the keep function

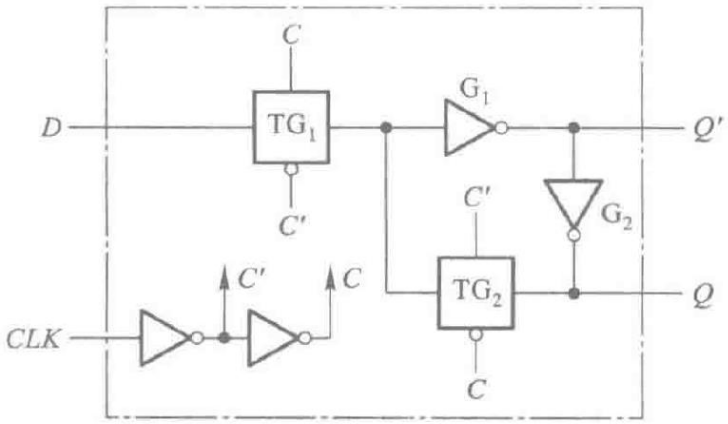
The gated D Latch



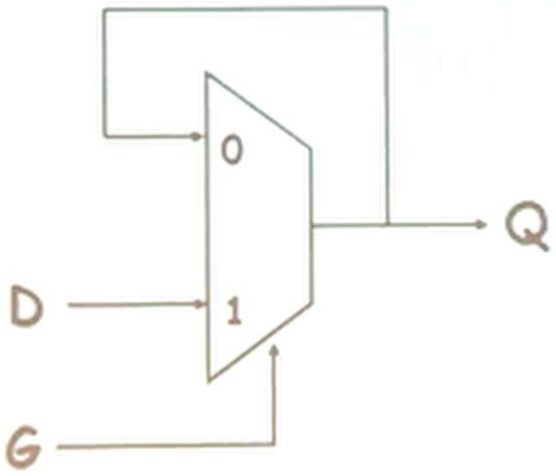


Question: plot the waveform of *Q* and *Q'*, assume the initial *Q* is 0

The gated D Latch



D latch using transmission gate



D latch using MUX