EE 115B: Digital Circuits

VHDL Tutorial 2
Vivado Usage for Beginners

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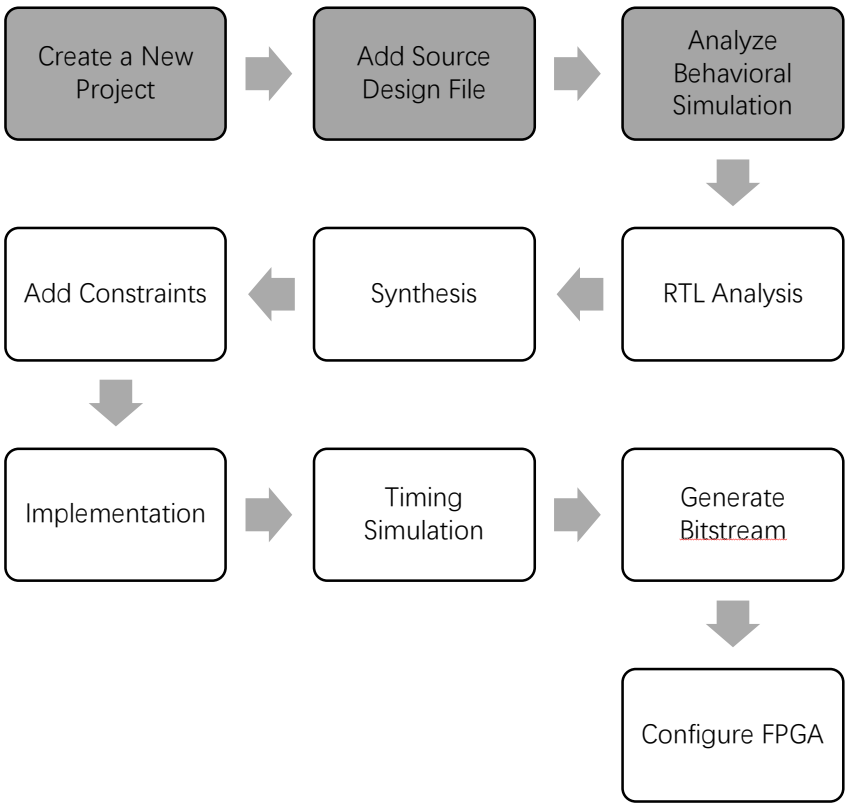
ShanghaiTech University

Introduction

In our lab, we will guide you to create a simple digital design using Xilinx Vivado software. A typical digital design flow consists of creating new projects, adding source design file, analyzing behavioral simulation, RTL analysis, synthesis, adding constraints, implementation, timing simulation，generating bitstream and configuring FPGA. You will go through the typical design flow targeting the Zynq-7000 All Programmable SoC based ZedBoard. The typical design flow is shown below. We focus on the first three steps in this tutorial.

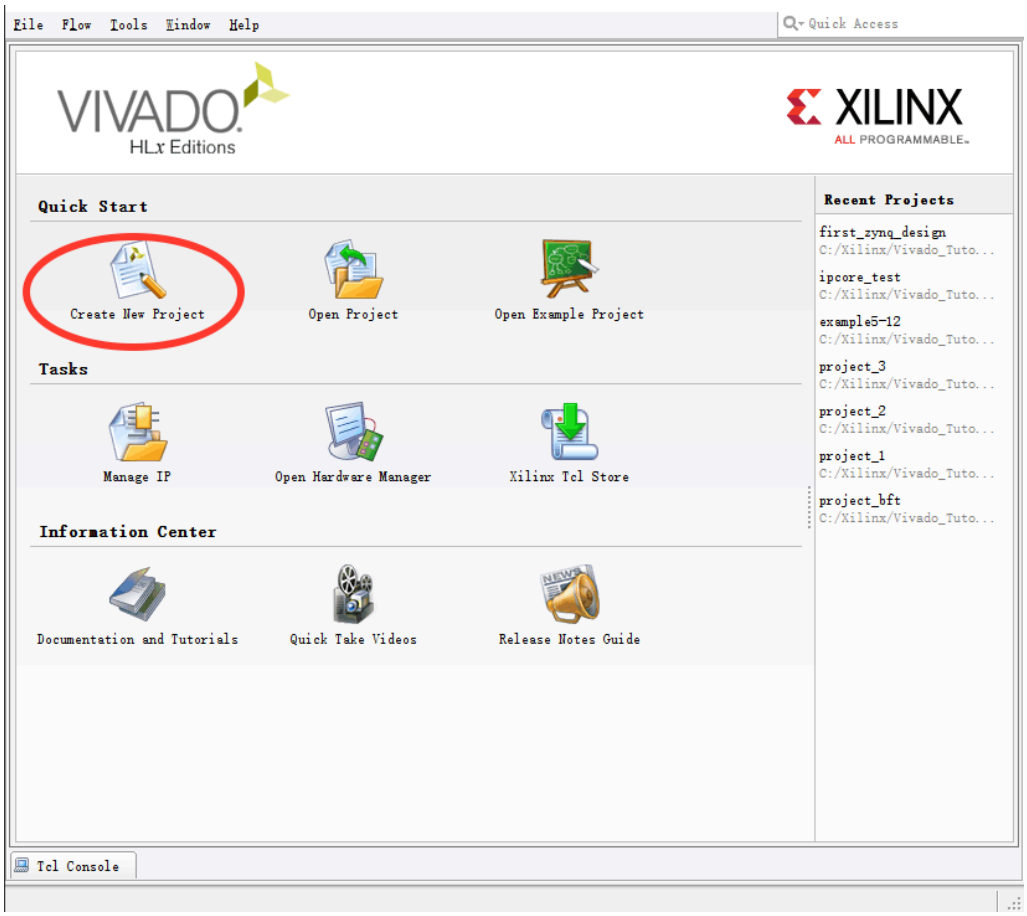


A typical design flow

General Flow for this tutorial

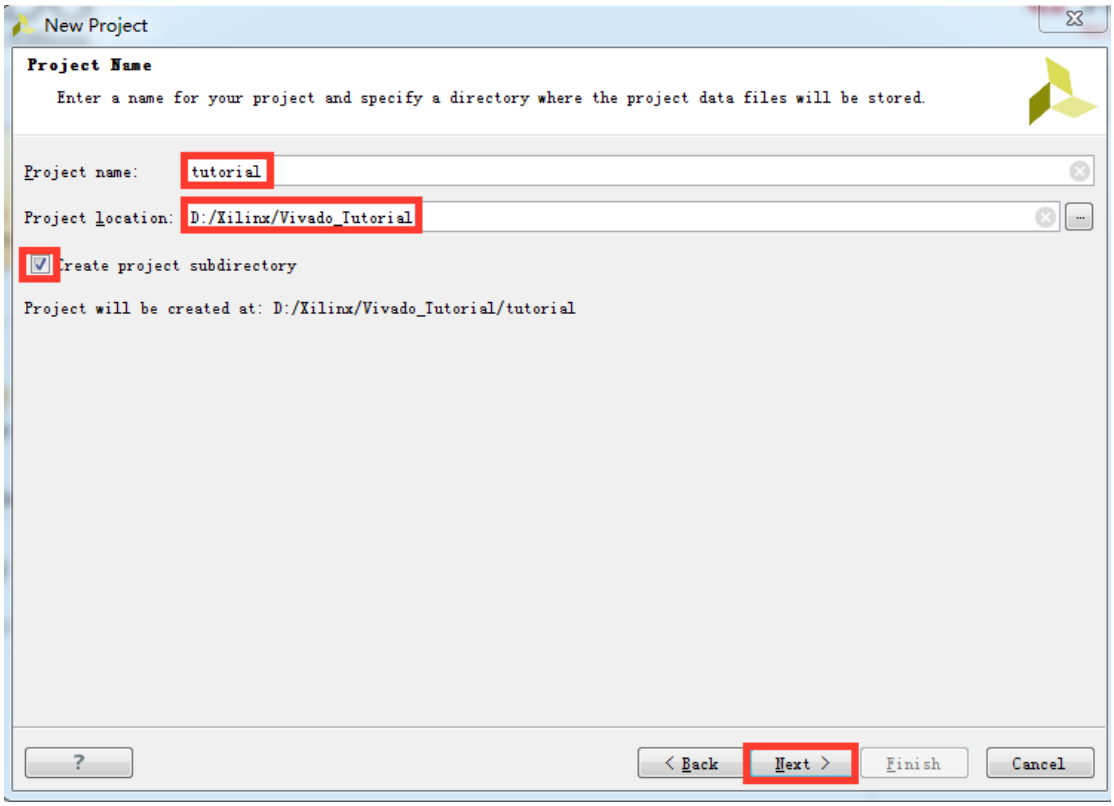
Step 1. Create A New Project

1. Open Vivado by selecting Start > All Programs > Xilinx Design Tools > Vivado 2016.2 >Vivado 2016.2
2. Click **Create New Project** to start the wizard. You will see Create A New Vivado Project dialog box. Click **Next**.

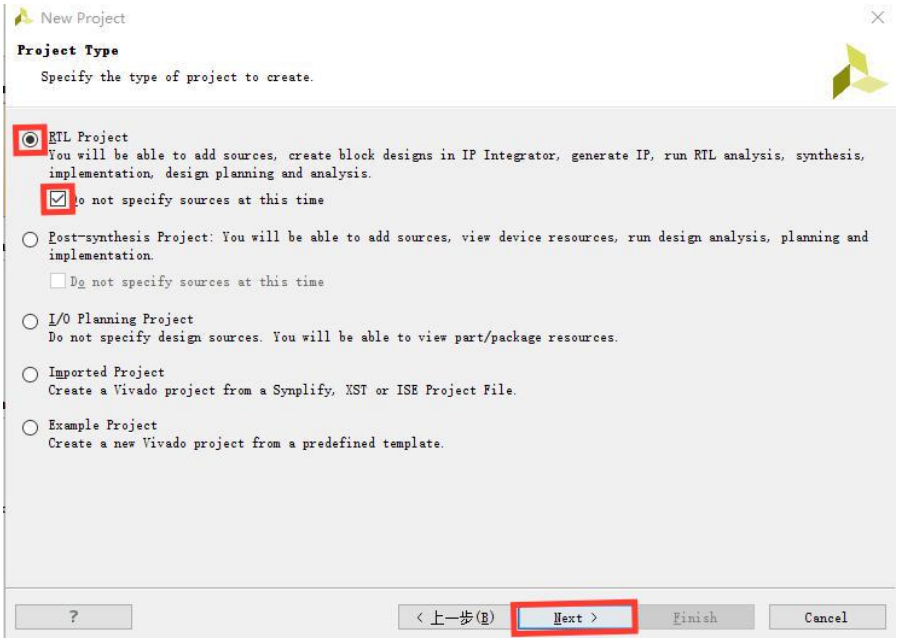



New Project
Create a New Vivado Project
This wizard will guide you through the creation of a new project.
To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.
To continue, click Next.
?
< 上一步(B)
Next >
Finish
Cancel

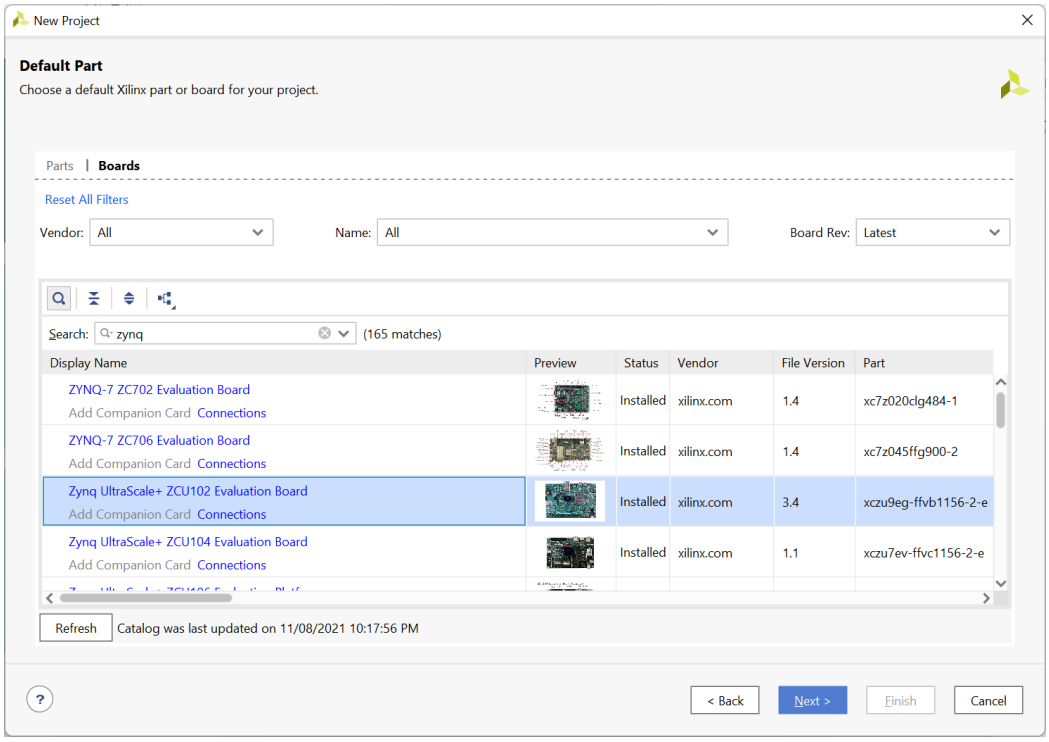
3. Enter **D:/Xilinx/Vivado_Tutorial** in Project location field.
4. Enter **tutorial** in the Project name field. Make sure that the ***Create Project Subdirectory*** box is checked. Click **Next**.



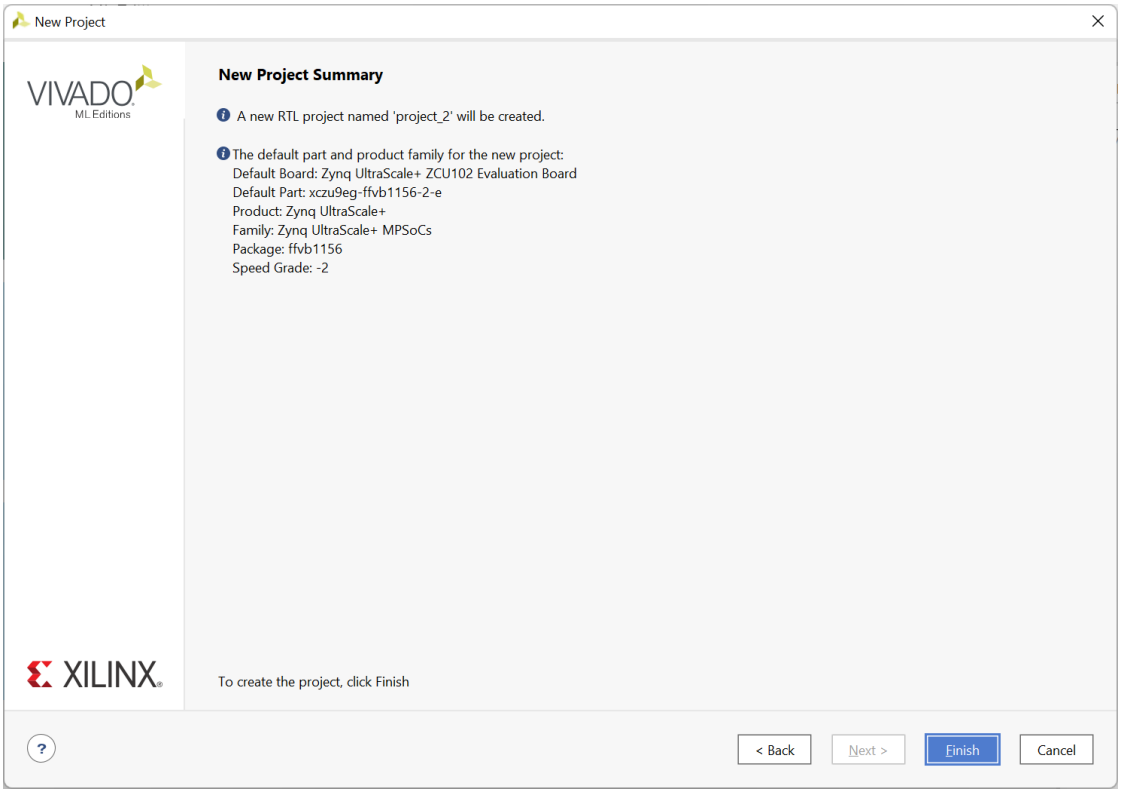
5. Select **RTL Project** option and check the **Do not specify sources at this time** box in the *Project Type* form, and click **Next**.

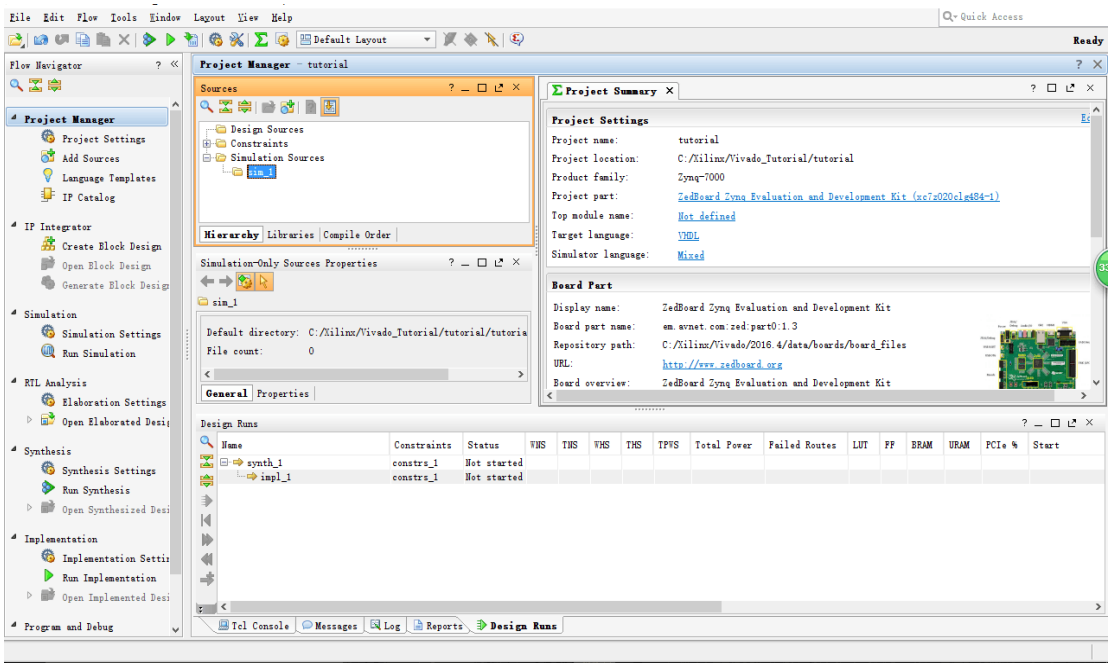


6. Choose **Boards** and select the **Zynq UltraScale+ ZCU102 Evaluation Board**, and click **Next**.



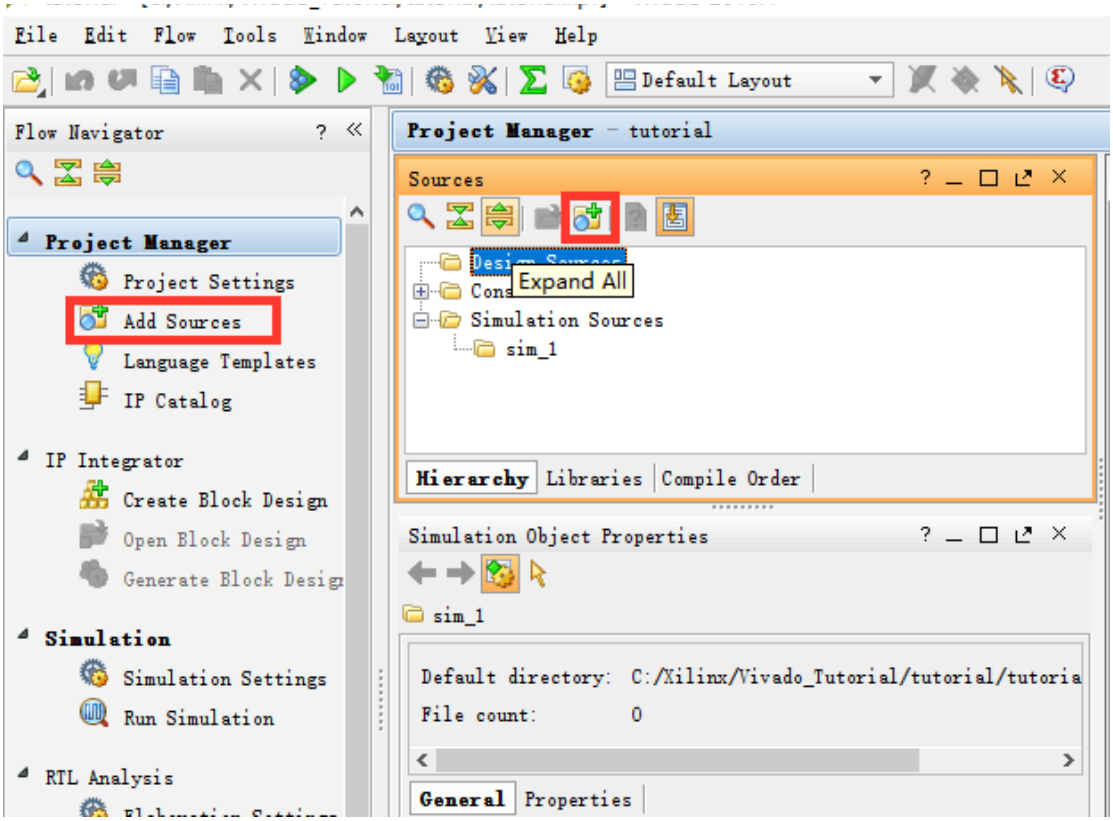
7. You will see **New Project Summary** dialog box. Click **Finish**.



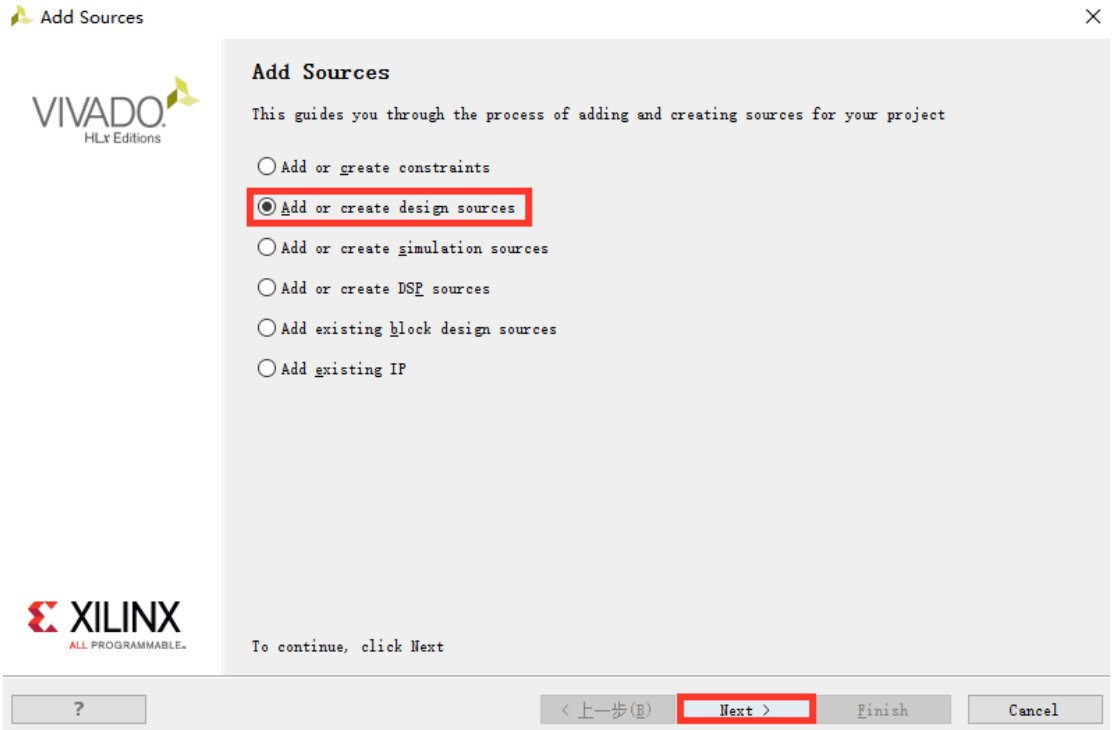

File Edit Flow Tools Window Layout View Help
Default Layout
Ready
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Implementation Settings
Run Implementation
Open Implemented Design
Program and Debug
Project Manager - tutorial
Sources
Design Sources
Constraints
Simulation Sources
sim_1
Hierarchy Libraries Compile Order
Simulation-Only Sources Properties
sim_1
Default directory: C:/Xilinx/Vivado_Tutorial/tutorial/tutoria
File count: 0
General Properties
Project Summary
Project Settings
Project name: tutorial
Project location: C:/Xilinx/Vivado_Tutorial/tutorial
Product family: Zynq-7000
Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clg484-1)
Top module name: Not defined
Target language: VHDL
Simulator language: Mixed
Board Part
Display name: ZedBoard Zynq Evaluation and Development Kit
Board part name: em.avnet.com:zed:part0:1.3
Repository path: C:/Xilinx/Vivado/2016.4/data/boards/board_files
URL: http://www.zedboard.org
Board overview: ZedBoard Zynq Evaluation and Development Kit
Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM PCIe % Start
synth_1 constrs_1 Not started
impl_1 constrs_1 Not started
Tcl Console Messages Log Reports Design Runs

Step 2. Add Source Design File.

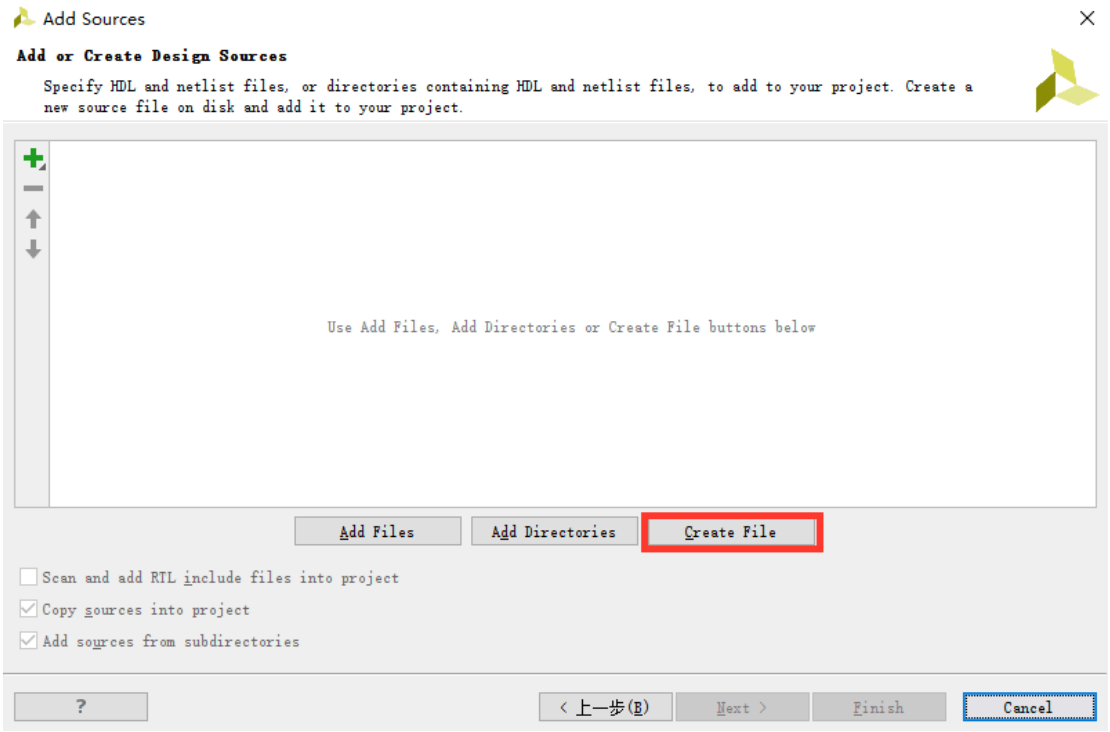
1. Click **Add Sources** under the *Project Manager* tasks of the *Flow Navigator* pane.



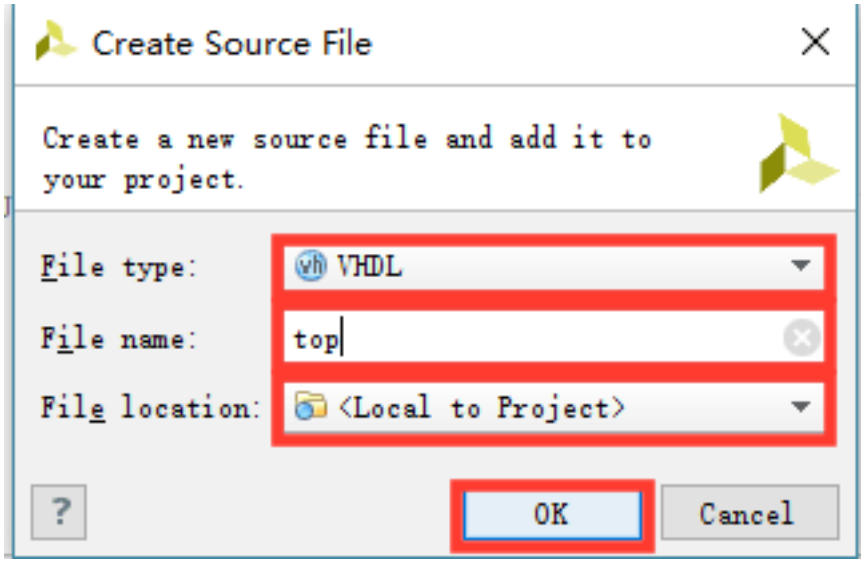
2. Select the **Add or Create Design Sources** option and click **Next**.



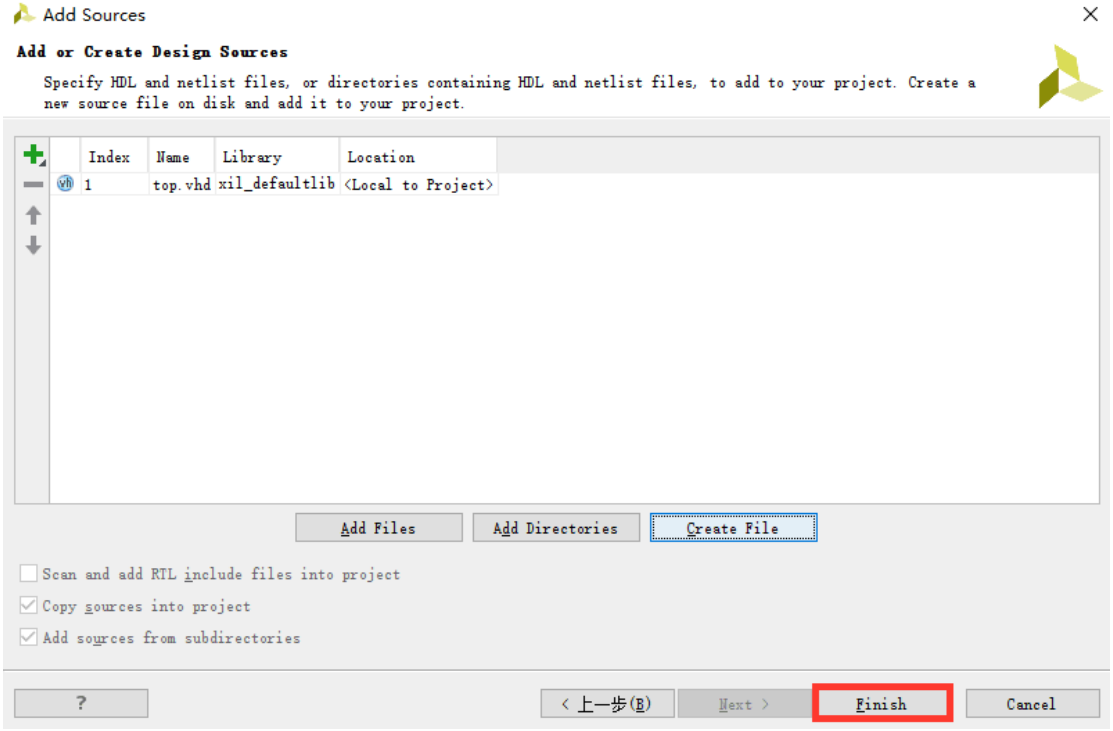
3. In the *Add Sources Files* form, click the **Create Files** button.



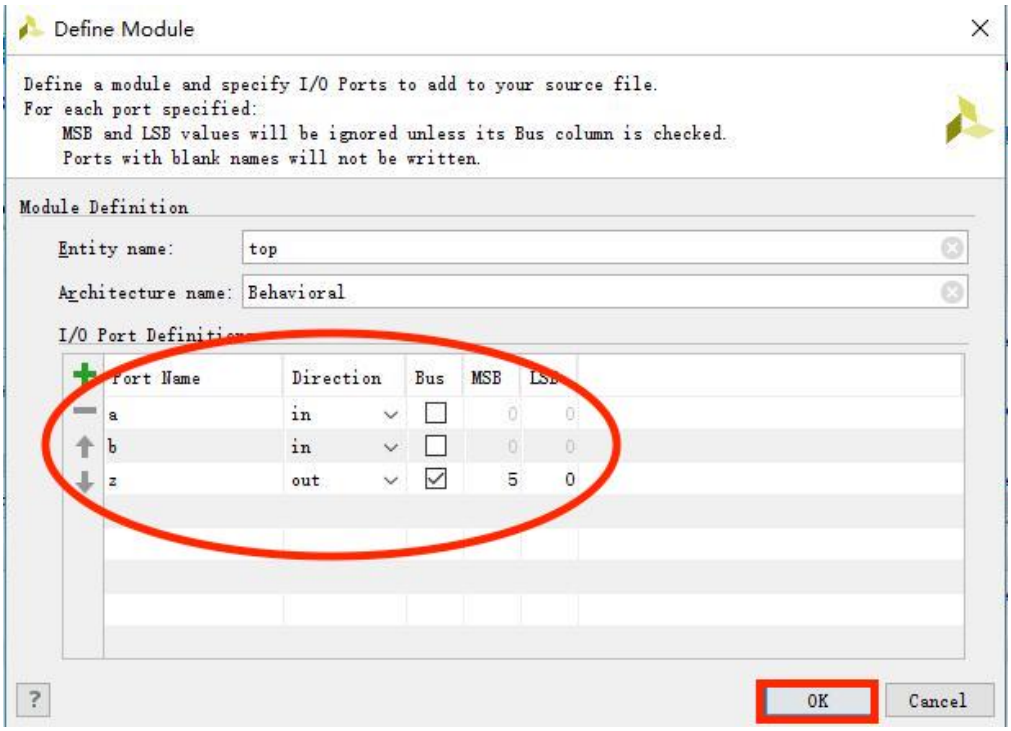
4. Set the *File type* to **VHDL** and input the *File name* such as **top**, and click **OK**.



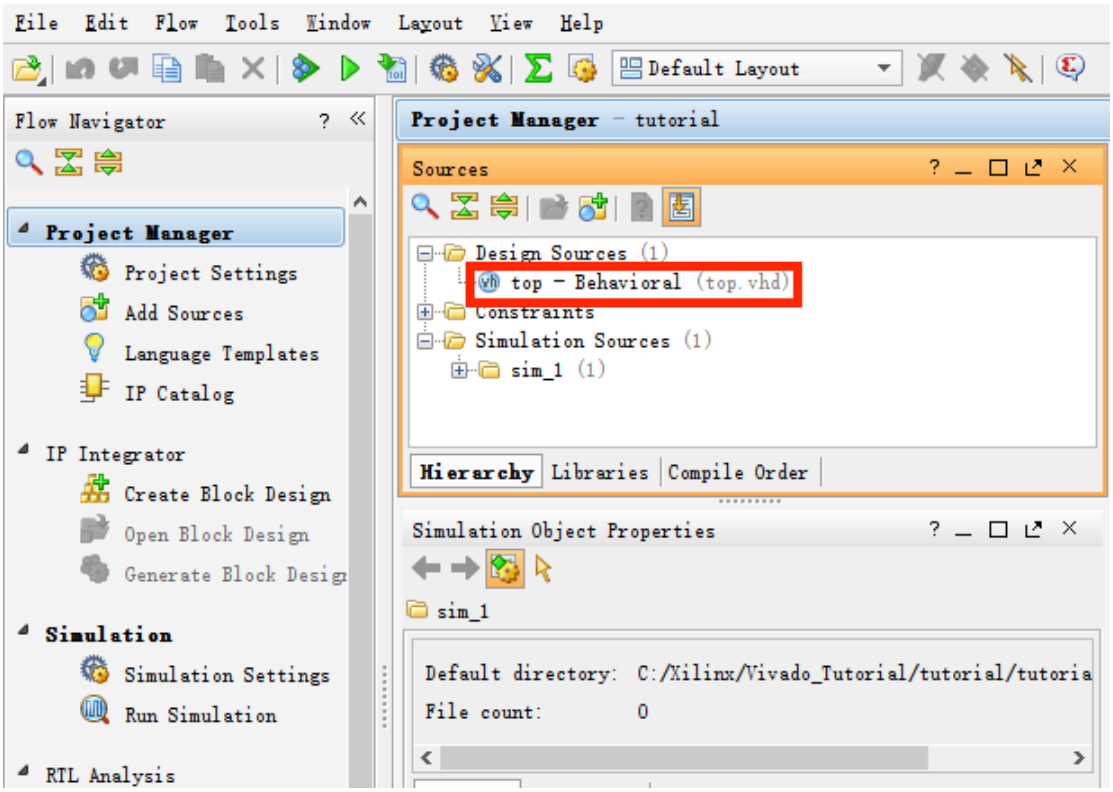
5. Click **Finish**.



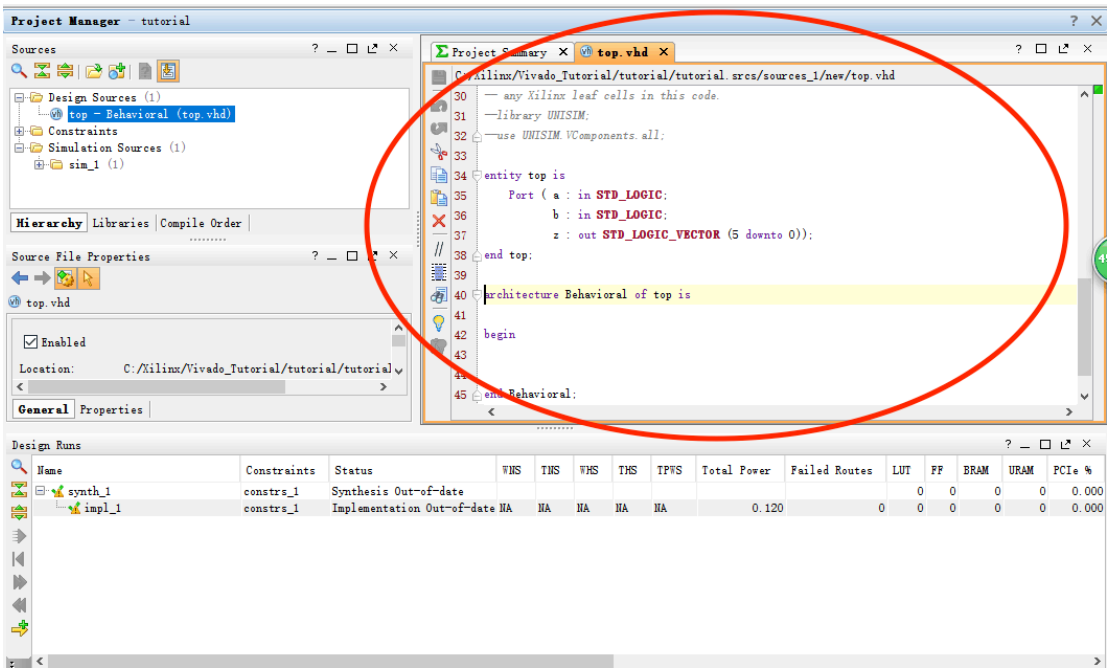
6. In **I/O Port Definition** of the pop-up **Define Module**, enter the design module required port, and set the port, if the port is bus type, check the Bus option, and set the **MSB** and **LSB** based on the bus width. Click **OK** when finished.



7. Double click the new created source file **top - Behavioral** and open it.



8. Now you can type in your own VHDL design code.

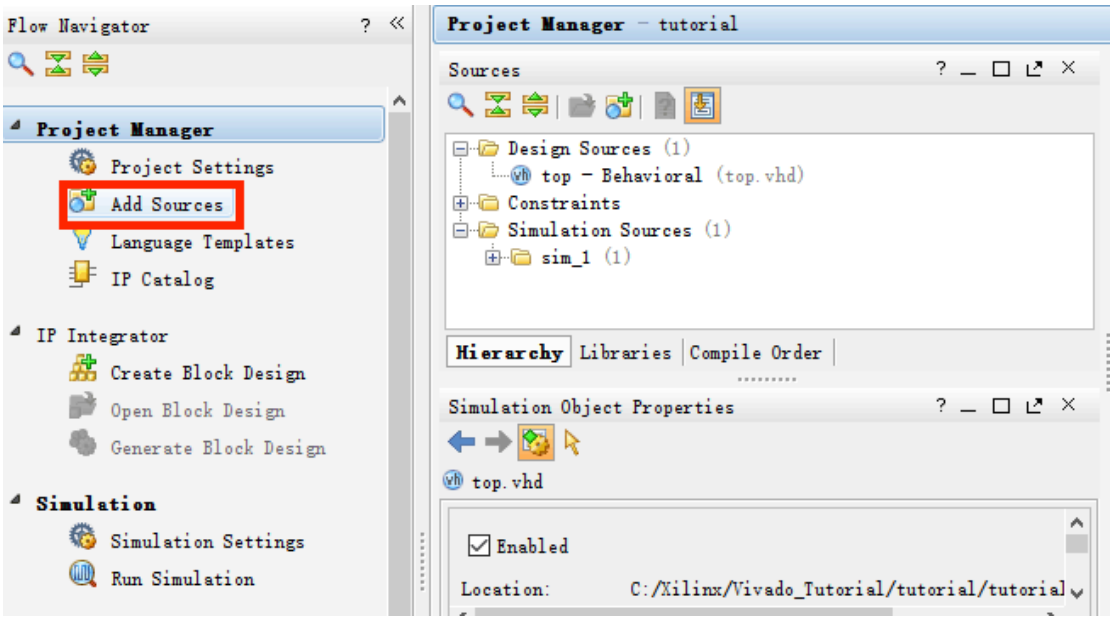


9. Save the file.

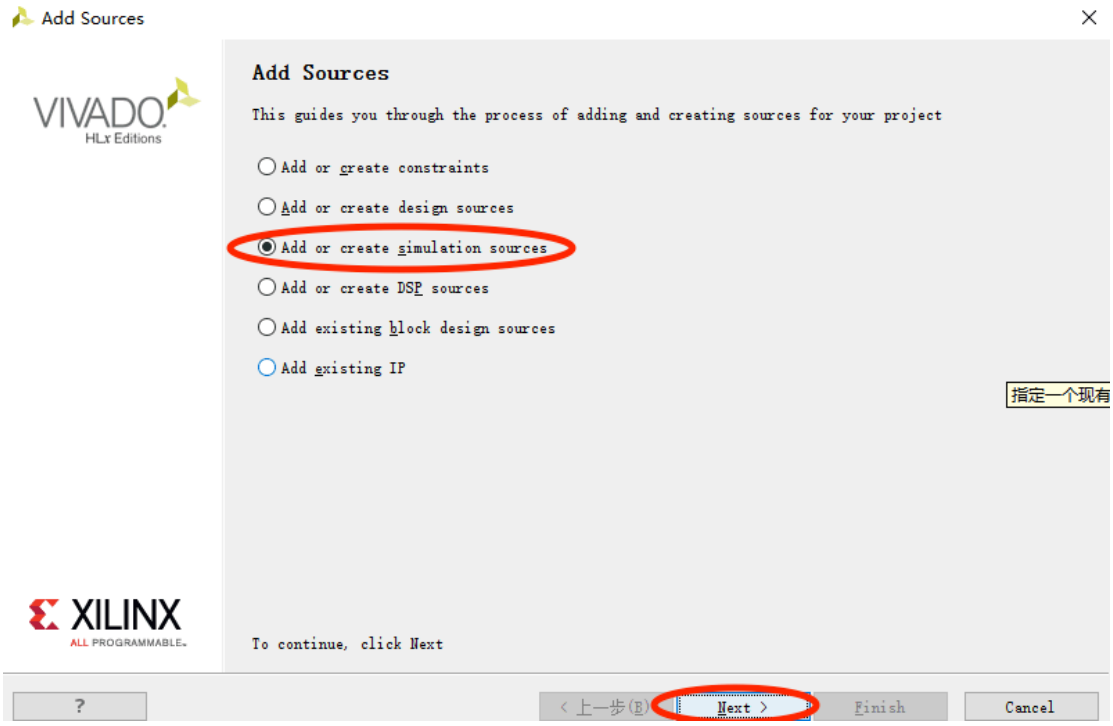
```
--Sample Code.
--top.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity top is
    Port (  a : in STD_LOGIC;
            b : in STD_LOGIC;
            z : out STD_LOGIC_VECTOR (5 downto 0));
end top;
architecture Behavioral of top is
begin
z(0)<=a and b;
z(1)<=a nand b;
z(2)<=a or b;
z(3)<=a nor b;
z(4)<=a xor b;
z(5)<=a xnor b;
end Behavioral;
```

Step 3. Behavioral Simulation

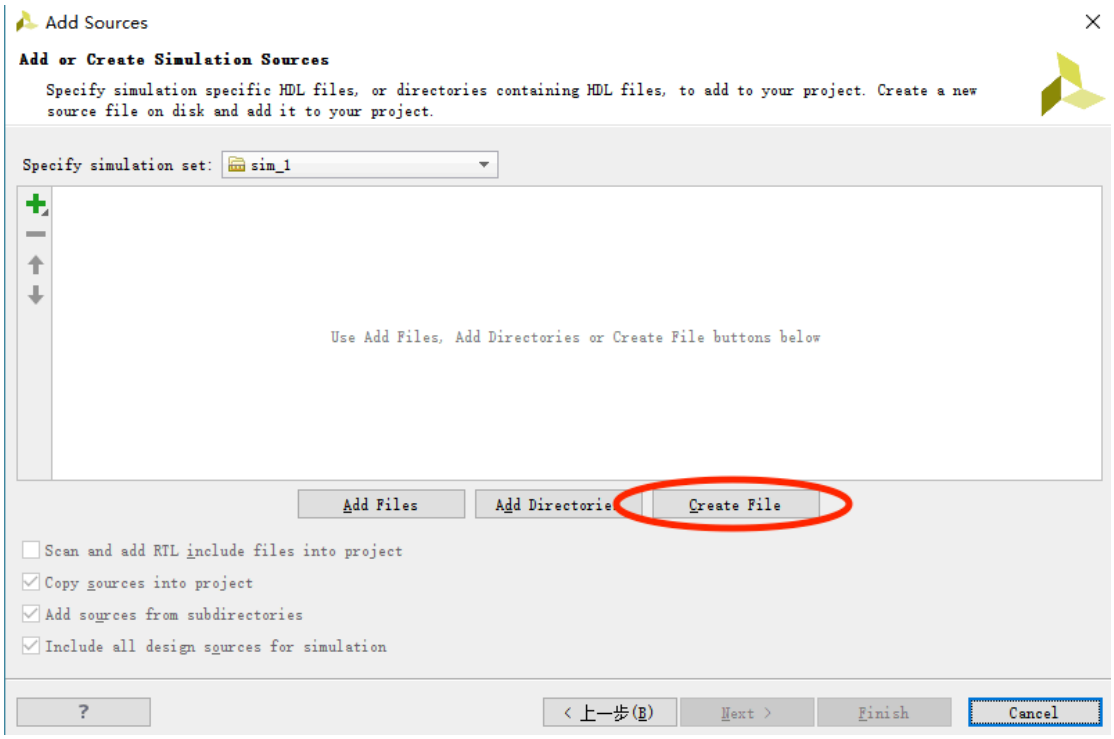
1. Click **Add Sources** under the *Project Manager* tasks of the *Flow Navigator* pane.



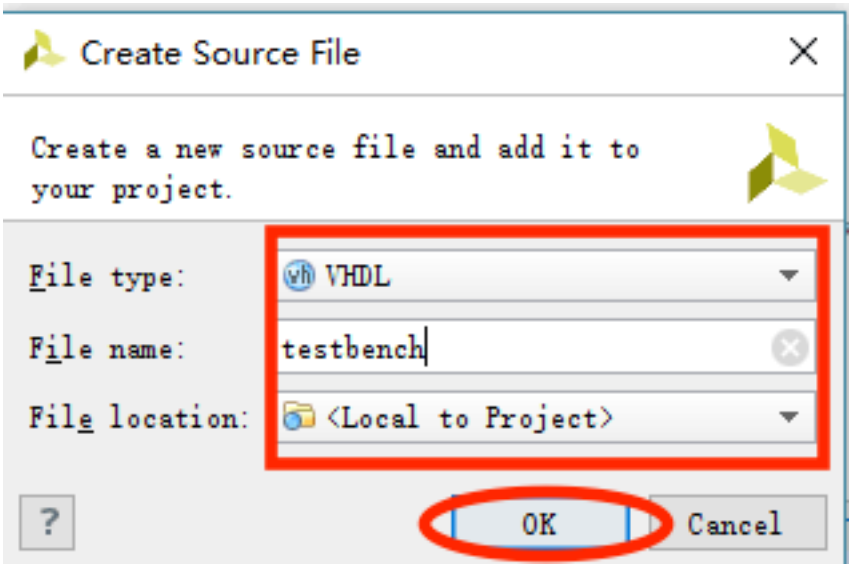
2. Select the *Add or Create Simulation Sources* option and click **Next**.



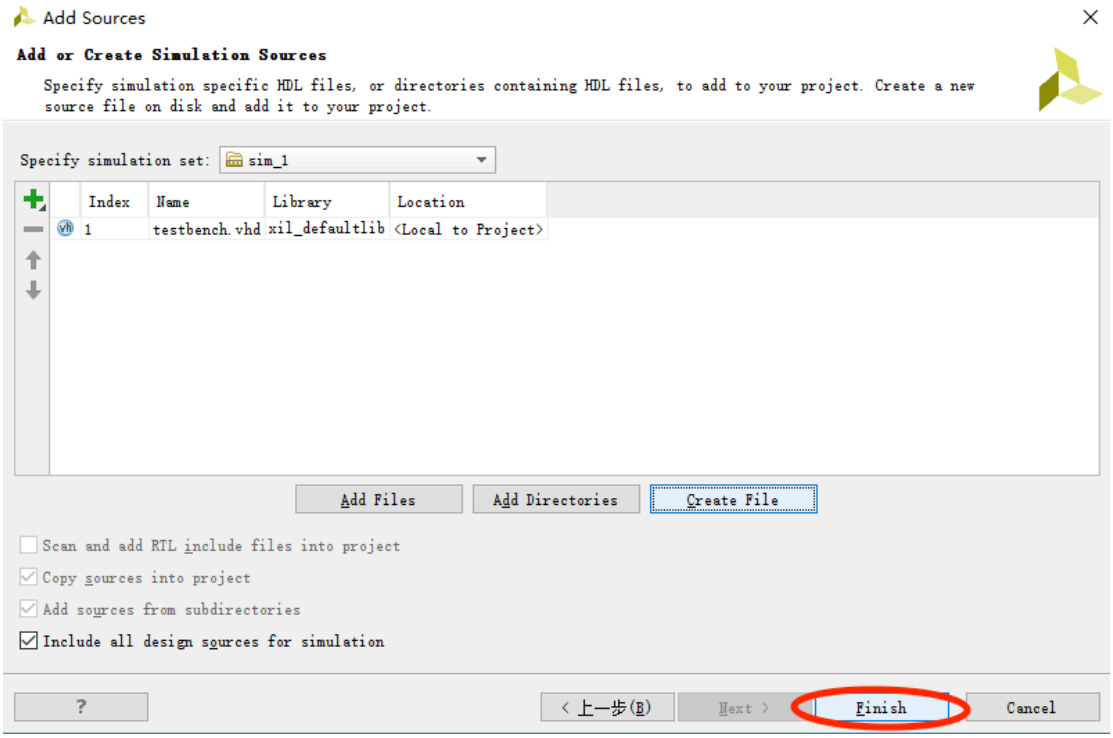
3. In the *Add Sources Files* form, click the **Create File** button.



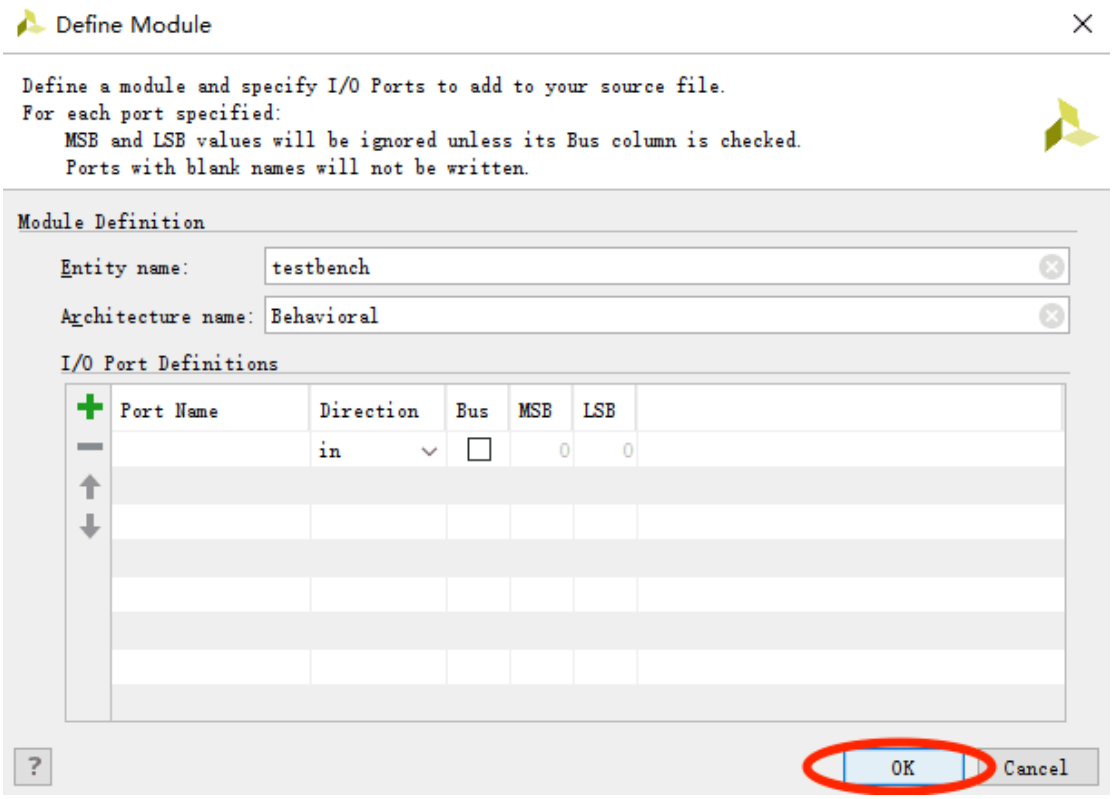
4. Set the *File type* to **VHDL** and input the *File name*, and click **OK**.



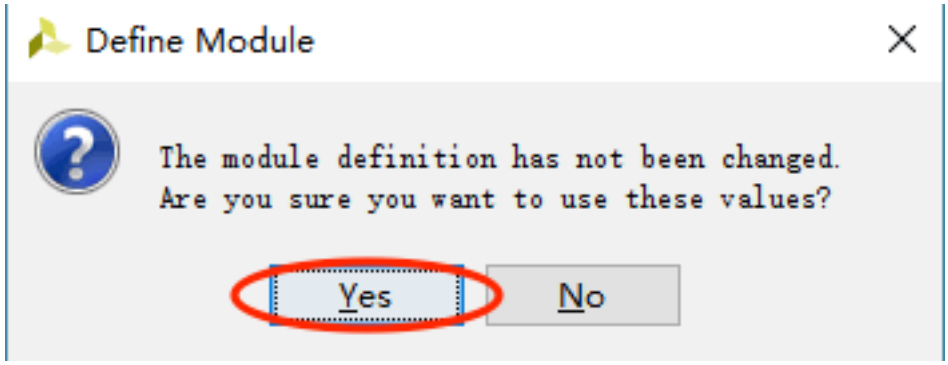
5. Click **Finish**.



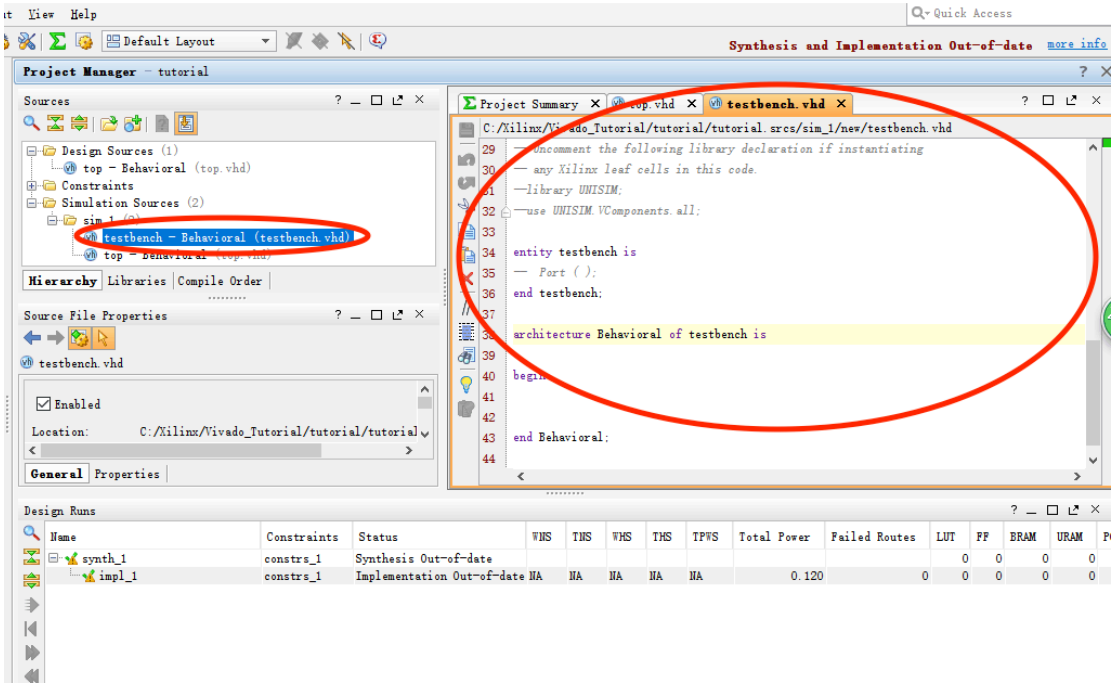
6. Click **OK**.



7. Click **Yes**.



8. Double click the new created source file **testbench - Behavioral** and open it. Then you can type in the test code.

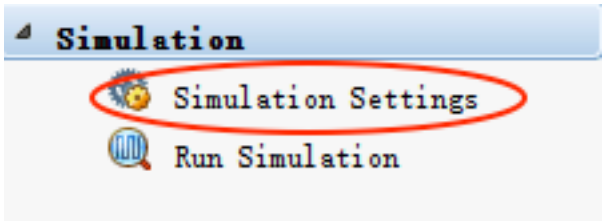


9. Save the file.

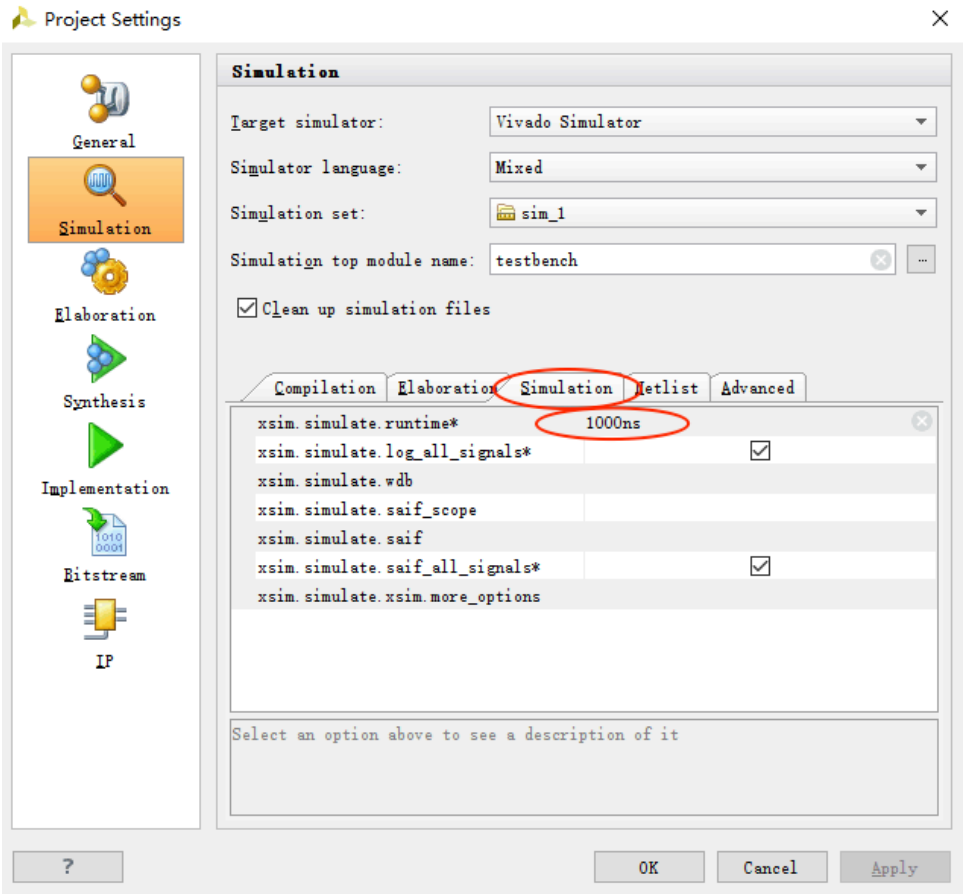
```
--Sample Code.
--testbench.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity testbench is
end testbench;

architecture Behavioral of testbench is
component top
   Port( a : in STD_LOGIC;
         b : in STD_LOGIC;
         z : out STD_LOGIC_VECTOR (5 downto 0)
         );
end component;
signal a : std_logic:='0';
signal b : std_logic:='0';
signal z : std_logic_vector(5 downto 0);
begin
uut : top port map(
                        a=>a,
                        b=>b,
                        z=>z
                          );
process
begin
    a<='0';
    b<='0';
    wait for 200 ns;
    a<='0';
    b<='1';
    wait for 200 ns;
    a<='1';
    b<='0';
```

```
    wait for 200 ns;
    a<='1';
    b<='1';
    wait for 200 ns;
end process;
end Behavioral;
```

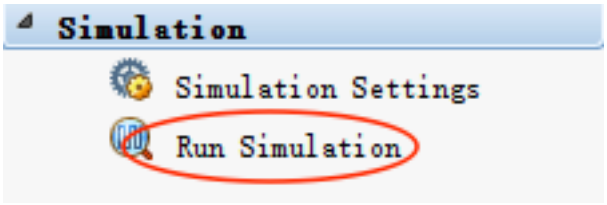
10. Select **Simulation Settings** under the *Project Manager* tasks of the *Flow Navigator* pane. A **Project Settings** form will appear showing the **Simulation** properties form.



11. Select the **Simulation** tab, and set the **Simulation Run Time** value to 1000 ns and click **OK**.



12. Click on **Run Simulation** > **Run Behavioral Simulation** under the Project Manager tasks of the *Flow Navigator* pane.



13. The testbench and source files will be compiled and the Vivado simulator will run (assuming no errors). You will see a simulator output similar to the one shown below.