ShanghaiTech University

EE 115B: Digital Circuits

Fall 2021

Midterm Exam, November 23, 2021

Solution

My signature below indicates that I understand and have complied with the Academic Integrity Policy of ShanghaiTech University. I have neither received nor given any unauthorized aid.

Print Name: [illegible] Signature: [illegible]

1. Short questions. (28 points. 2 points each.)
   1) Convert $(17.25)_{10}$ to binary.

$17 \div 2 = 8$ remainder 1; $8 \div 2 = 4$ remainder 0; $4 \div 2 = 2$ remainder 0; $2 \div 2 = 1$ remainder 0; $1 \div 2 = 0$ remainder 1

$0.25 \times 2 = 0.5$ → 0; $0.5 \times 2 = 1.0$ → 1

$$(17.25)_{10} = (10001.01)_2$$

   2) Convert $(101.11)_2$ to decimal.

$$(101.11)_2 = 1\times 2^2 + 0\times 2^1 + 1\times 2^0 + 1\times 2^{-1} + 1\times 2^{-2}$$
$$= (5.75)_{10}$$

   3) Convert $(2E.A)_{16}$ to octal.

2 → 0010, E → 1110, . , A → 1010

00101110 . 1010 → 5 6 . 5

$$(2E.A)_{16} = (56.5)_8$$

   4) Convert $(000110010010)_{BCD}$ to decimal.

0001 → 1, 1001 → 9, 0010 → 2

$$(000110010010)_{BCD} = (192)_{10}$$

5) Determine the even parity bit for 11010.

Three 1's ⇒ Even parity bit is '1'.

6) (True or False) The XOR gate is also called the equivalence gate.

False

7) (True or False) The POS form of a logic function is written with minterms.

False

8) (True or False) If the value of a logic variable is 0, it appears in the complemented form in a maxterm.

False

9) What does "VHDL" stand for?

VHSIC (Very High Speed Integrated Circuits)
Hardware Description Language

10) What does "FPGA" stand for?

Field Programmable Gate Array

11) (True or False) The VHDL code is case sensitive.

False

12) (True or False) A signal has three possible values: 0, 1, and Z. It is fine to use BIT as the type of this signal.

False

13) Given the following VHDL code, determine the value of A(6 downto 3).

```
signal A: std_logic_vector (7 downto 0);
A <= "11001010";
```

A(6 downto 3)= 1001

14) Given the following VHDL code, write the logic function for F.

```
F <= A and B or C and D;
```

F= (AB+C)D

2. Derive the standard SOP and POS expressions for the following function. Write the results in two forms: (a) explicit expressions with minterms/maxterms (e.g., Y=ABC) and (b) compact expressions with indexes of minterms/maxterms (e.g., Y=∑m(7) for Y=ABC). (12 points. 3 points each.)

$$\boldsymbol{Y(A,B,C) = (A + \bar{C})(\bar{A} + B)}$$

$Y = (A+\bar{C})(\bar{A}+B)$

$= (A+\bar{C}+B\bar{B})(\bar{A}+B+C\bar{C})$

PoS explicit $= (A+B+\bar{C})(A+\bar{B}+\bar{C})(\bar{A}+B+C)(\bar{A}+B+\bar{C})$

$= M_1 M_3 M_4 M_5$

PoS compact $= \Pi M(1,3,4,5)$

Sop compact $= \Sigma m(0,2,6,7)$

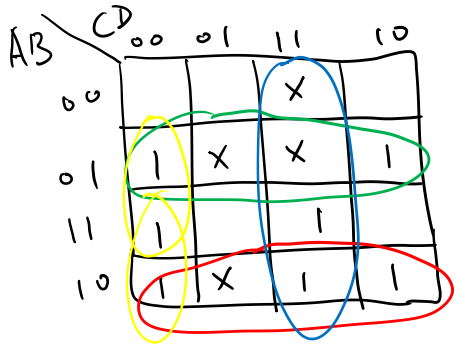
$= m_0 + m_2 + m_6 + m_7$

Sop explicit $= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + AB\bar{C} + ABC$

3. Develop the minimum SOP and POS expressions for the following function using Karnaugh map. (20 points. 10 points each.)

$$Y(A,B,C,D) = \sum m(4,6,8,10,11,12,15) + D(3,5,7,9)$$

> SOP



Red: $A\bar{B}$

Green: $\bar{A}B$

Blue: CD

} EPIs

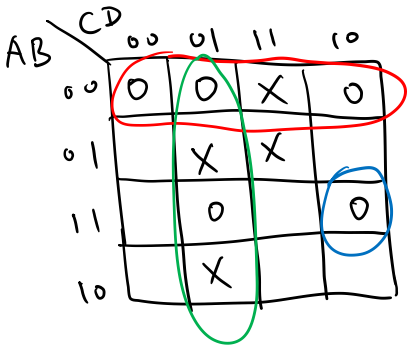
Yellow: $B\bar{C}\bar{D}$ or $A\bar{C}\bar{D}$ } PIs

$$Y = A\bar{B} + \bar{A}B + CD + B\bar{C}\bar{D}$$

or

$$Y = A\bar{B} + \bar{A}B + CD + A\bar{C}\bar{D}$$

> POS



Red: $A+B$

Green: $C+\bar{D}$

Blue: $\bar{A}+\bar{B}+\bar{C}+D$

} EPIs

$$Y = (A+B)(C+\bar{D})(\bar{A}+\bar{B}+\bar{C}+D)$$

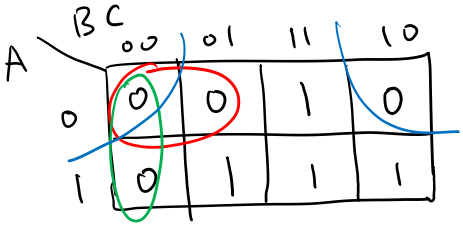
4. Convert the following AND-OR expression to NAND, AND-OR-Invert (AOI), and NOR expressions. (12 points. 4 points each.)

$$\boldsymbol{Y(A,B,C) = AB + BC + AC}$$

> NAND

$$Y = AB + Bc + Ac = \overline{\overline{AB + Bc + Ac}} = \overline{\overline{AB} \cdot \overline{Bc} \cdot \overline{Ac}}$$

> AOI



Red : $\bar{A}\bar{B}$

Green : $\bar{B}\bar{C}$

Blue : $\bar{A}\bar{C}$

$$Y = \overline{\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}}$$

> NOR

$$Y = \overline{\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}}$$

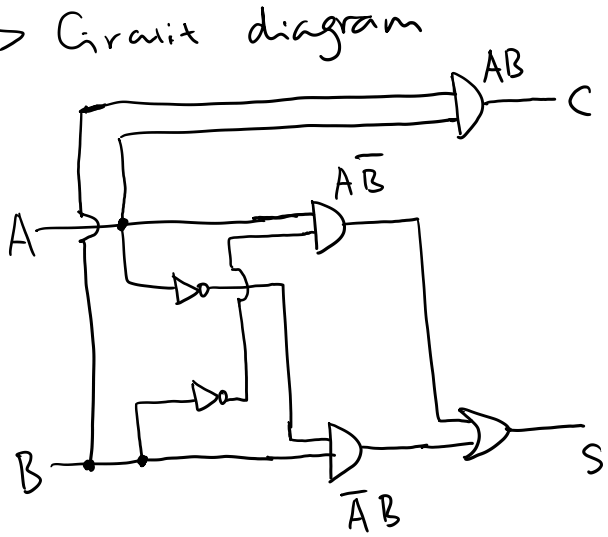
$$= \overline{\overline{A+B} + \overline{B+C} + \overline{A+C}}$$

5. Design a 1-bit half-adder using AND, OR, and NOT gates. The inputs are A and B. The outputs are S and C: S is the sum and C is the carry out. You need to (a) build the truth table, (b) write the logic expressions for S and C, and (c) draw the circuit diagram. (12 points. 4 points each.)

> Truth table

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

> Circuit diagram



$S = \bar{A}B + A\bar{B}$

$C = AB$

6. Plot the output (Y_0 through Y_7) waveforms given the following inputs to the 3-8 decoder (also a DEMUX) 74LS138. The enable inputs G_{2A} and G_{2B} are set as LOW all the time. (16 points. 2 points each.)